(Rev. 4.1)

MITSUBISHI LSIs

M5M467805/465805AJ,ATP -5,-6,-5S,-6S

EDO (HYPER PAGE MODE) 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 8388608-word by 8-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.
The use of double-layer aluminum process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M467805XX-5,5S	50	13	25	13	84	300
M5M467805XX-6,6S	60	15	30	15	104	250
M5M465805XX-5,5S	50	13	25	13	84	390
M5M465805XX-6,6S	60	15	30	15	104	325

XX=AJ,ATP

- **Standard 32 pin SOJ, 32 pin TSOP**
- **Single 3.3 ± 0.3V supply**
- **Low stand-by power dissipation**
  - **1.08mW (Max) - - - - - - - - - - - - - - LVCMOS input level**
- **Low operating power dissipation**
  - **M5M467805xx-5 - - - - - - - - - - - - - 360.0mW (Max)**
  - **M5M467805xx-6 - - - - - - - - - - - - - 324.0mW (Max)**
  - **M5M465805xx-5 - - - - - - - - - - - - - 468.0mW (Max)**
  - **M5M465805xx-6 - - - - - - - - - - - - - 432.0mW (Max)**
- **Self refresh capability***
  - **Self refresh current - - - - - - - - - - 400μA(Max)**
- **Hyper-page mode , Read-modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities**
- **Early-write mode , $\overline{OE}$ and $\overline{W}$ to control output buffer impedance**
- **All inputs, outputs LVTTL compatible and low capacitance**

*** : Applicable to self refresh version(M5M467/5805AJ,ATP -5S,-6S : option) only**

ADDRESS

Part No.	Row Add	Col Add	Refresh	Refresh Cycle Normal	Refresh Cycle S-version
M5M467805A	A0-A12	A0-A9	$\overline{RAS}$ Only Ref,Normal R/W	8192/64ms	8192/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465805A	A0-A11	A0-A10	$\overline{RAS}$ Only Ref,Normal R/W CBR Ref,Hidden Ref	4096/64ms	4096/128ms

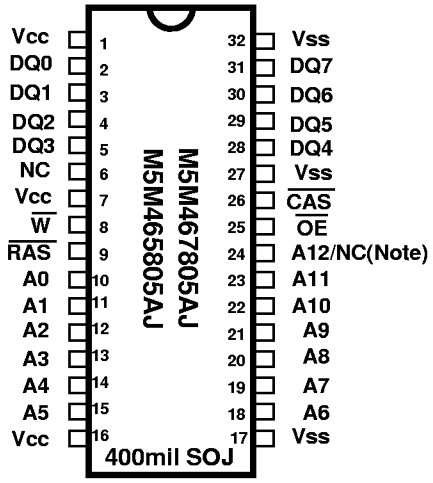
APPLICATION

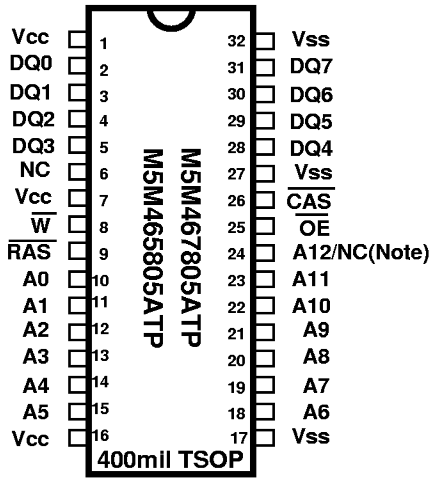
Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin Name	Function
A_0-A_{12}	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

PIN CONFIGURATION (TOP VIEW)





Note : A12...M5M467805A , NC...M5M465805A
NC : NO CONNECTION

FUNCTION

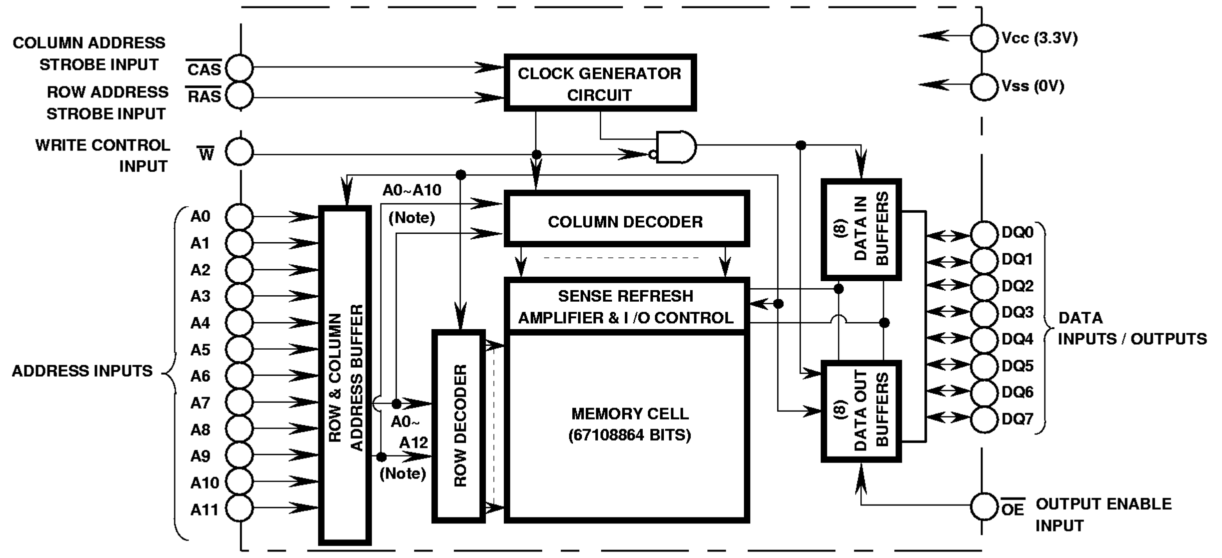
The M5M467805/465805AJ,ATP provide,in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g. , hyper page mode, $\overline{CAS}$ before $\overline{RAS}$ refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	NO	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	NO	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	NO	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



Note : Refer to Page 1 (ADDRESS)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
VI	Input voltage		-0.5 ~ Vcc+0.5	V
V0	Output voltage		-0.5 ~ Vcc+0.5	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C , unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

[M5M467805A]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ Vcc	-10		10	µA
I_I	Input current		0V ≤ VIN ≤ Vcc+0.3V, Other inputs pins=0V	-10		10	µA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M467805-5,5S	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling t_{RC}=t_{WC}=min. output open			100	mA
		M5M467805-6,6S				90	
I_{CC2}	Supply current from Vcc , stand-by	M5M467805-5,5S -6,6S	$\overline{\text{RAS}}$= $\overline{\text{CAS}}$ =V_{IH}, output open			1	mA
		M5M467805-5,6	$\overline{\text{RAS}}$=$\overline{\text{CAS}}$=$\overline{\text{WE}}$ ≥Vcc -0.2V,output open			0.5	
		M5M467805-5S,6S				0.3	
I_{CC4}(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M467805-5,5S	RAS=V_{IL}, CAS cycling t_{PC}=min. output open			100	mA
		M5M467805-6,6S				90	
I_{CC6}(AV)	Average supply current from Vcc $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode (Note 3,5)	M5M467805-5,5S	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling t_{RC}=min. output open			130	mA
		M5M467805-6,6S				120	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV) , Icc4 (AV) and Icc6 (AV)are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{\text{RAS}}$=V_{IL} and $\overline{\text{CAS}}$=V_{IH}.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

[M5M465805A]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ Vcc	-10		10	µA
I_I	Input current		0V ≤ VIN ≤ Vcc+0.3V, Other inputs pins=0V	-10		10	µA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M465805-5,5S	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling t_{RC}=t_{WC}=min. output open			130	mA
		M5M465805-6,6S				120	
I_{CC2}	Supply current from Vcc , stand-by	M5M465805-5,5S -6,6S	$\overline{\text{RAS}}$= $\overline{\text{CAS}}$ =V_{IH}, output open			1	mA
		M5M465805-5,6	$\overline{\text{RAS}}$=$\overline{\text{CAS}}$=$\overline{\text{WE}}$ ≥Vcc -0.2V,output open			0.5	
		M5M465805-5S,6S				0.3	
I_{CC4}(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M465805-5,5S	$\overline{\text{RAS}}$=V_{IL}, $\overline{\text{CAS}}$ cycling t_{PC}=min. output open			100	mA
		M5M465805-6,6S				90	
I_{CC6}(AV)	Average supply current from Vcc $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode (Note 3,5)	M5M465805-5,5S	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling t_{RC}=min. output open			130	mA
		M5M465805-6,6S				120	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV) , Icc4 (AV) and Icc6 (AV)are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{\text{RAS}}$=VIL and $\overline{\text{CAS}}$=VIH.

CAPACITANCE (Ta=0 ~ 70°C , Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance,address inputs	V_I=Vss f=1MHz Vi=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{\text{OE}}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{\text{RAS}}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{\text{CAS}}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS

(Ta=0 ~70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter	Limits				Unit
		M5M46X805-5,5S		M5M46X805-6,6S		
		Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7,8)		13		15	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7,9)		50		60	ns
t_{AA}	Column address access time (Note 7,10)		25		30	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 7,11)		28		33	ns
t_{OEA}	Access time from $\overline{OE}$ (Note 7)		13		15	ns
t_{OHC}	Output hold time from $\overline{CAS}$	5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$ (Note 13)	5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low (Note 7)	5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (Note 12)		13		15	ns
t_{WEZ}	Output disable time after $\overline{WE}$ high (Note 12)		13		15	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 12,13)		13		15	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high (Note 12,13)		13		15	ns

Note 6: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-2mA) / VOL=0.4V(IOL=2mA) loads and 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ(max)}$,$t_{WEZ(max)}$,$t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq \pm 10\mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~70 °C, Vcc=3.3 ±0.3V, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter		Limits				Unit
			M5M46X805-5,5S		M5M46X805-6,6S		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time			64		64	ms
t_{REF}	Refresh cycle time (S-version only)			128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note16)	14	37	14	45	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		8		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note17)	10	25	12	30	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note18)	0	10	0	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		8		10		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note19)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note19)	0		0		ns
t_{RDD}	Delay time, $\overline{RAS}$ high to data	(Note20)	13		15		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note20)	13		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note20)	13		15		ns
t_{WED}	Delay time, $\overline{WE}$ low to data	(Note20)	13		15		ns
t_T	Transition time	(Note21)	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T=2ns.
15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.
17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
19: Either t_{DZC} or t_{DZO} must be satisfied.
20: Either t_{RDD} or t_{CDD} or t_{ODD} or t_{WED} must be satisfied.
21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M46X805-5,5S		M5M46X805-6,6S		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		84		104		ns
t_{RAS}	$\overline{RAS}$ low pulse width		50	10000	60	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		8	10000	10	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		35		40		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		25		30		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time		13		18		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M46X805-5,5S		M5M46X805-6,6S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	84		104		ns
t_{RAS}	RAS low pulse width	50	10000	60	10000	ns
t_{CAS}	CAS low pulse width	8	10000	10	10000	ns
t_{CSH}	CAS hold time after RAS low	35		40		ns
t_{RSH}	RAS hold time after CAS low	13		15		ns
t_{WCS}	Write setup time before CAS low (Note 24)	0		0		ns
t_{WCH}	Write hold time after CAS low	8		10		ns
t_{CWL}	CAS hold time after W low	8		10		ns
t_{RWL}	RAS hold time after W low	8		10		ns
t_{WP}	Write pulse width	8		10		ns
t_{DS}	Data setup time before CAS low or W low	0		0		ns
t_{DH}	Data hold time after CAS low or W low	8		10		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M46X805-5,5S		M5M46X805-6,6S		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note23)	109		133		ns
t_{RAS}	RAS low pulse width	75	10000	89	10000	ns
t_{CAS}	CAS low pulse width	38	10000	44	10000	ns
t_{CSH}	CAS hold time after RAS low	70		82		ns
t_{RSH}	RAS hold time after CAS low	38		44		ns
t_{RCS}	Read setup time before CAS low	0		0		ns
t_{CWD}	Delay time, CAS low to W low (Note24)	28		32		ns
t_{RWD}	Delay time, RAS low to W low (Note24)	65		77		ns
t_{AWD}	Delay time, address to W low (Note24)	40		47		ns
t_{OEH}	OE hold time after W low	13		15		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD},t_{RWD} and t_{AWD} and,t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD\ (min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for Hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied, the DQ (at access time and until CAS or OE goes back to V_{IH}) is indeterminate.

Hyper page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by OE or W) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M46X805-5,5S		M5M46X805-6,6S		
		Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	20		25		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time	55		66		ns
t_{DOH}	Output hold time from CAS low	5		5		ns
t_{RAS}	RAS low pulse width for read write cycle (Note26)	65	100000	77	100000	ns
t_{CP}	CAS high pulse width (Note27)	8	13	10	16	ns
t_{CPRH}	RAS hold time after CAS precharge	28		33		ns
t_{CPWD}	Delay time, CAS precharge to W low (Note24)	43		50		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until CAS access	7		7		ns
t_{OEPE}	OE Pulse Width (Hi-Z control)	7		7		ns
t_{WPE}	W Pulse Width (Hi-Z control)	7		7		ns
t_{HCWD}	Delay time, CAS low to W low after read	28		32		ns
t_{HAWD}	Delay time, Address to W low after read	40		47		ns
t_{HPWD}	Delay time, CAS precharge to W low after read	43		50		ns
t_{HCOD}	Delay time, CAS low to OE high after read	13		15		ns
t_{HAOD}	Delay time, Address to OE high after read	25		30		ns
t_{HPOD}	Delay time, CAS precharge to OE high after read	28		33		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of CAS input are performed.
27: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP} \geq t_{CP(max)}$, access time is controlled exclusively by tCAC.

CAS before RAS Refresh Cycle (Note 28)

Symbol	Parameter	Limits				Unit
		M5M46X805-5,5S		M5M46X805-6,6S		
		Min	Max	Min	Max	
t_{CSR}	CAS setup time before RAS low	5		5		ns
t_{CHR}	CAS hold time after RAS low	10		10		ns
t_{RSR}	Read setup time before RAS low	10		10		ns
t_{RHR}	Read hold time after RAS low	10		10		ns

Note 28: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S . The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC9\ (AV)}$*	Average supply current from Vcc Self - Refresh cycle (note 6)	M5M467/5805-5S,6S	$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2V $\overline{OE}$= $\overline{W}$ =A0~A12(A11)=Vcc-0.2V or 0.2V output =Vcc-0.2V,0.2V or OPEN			400	µA

TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M46X805-5S		M5M46X805-6S		
		Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		µS
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of CBR distributed refresh

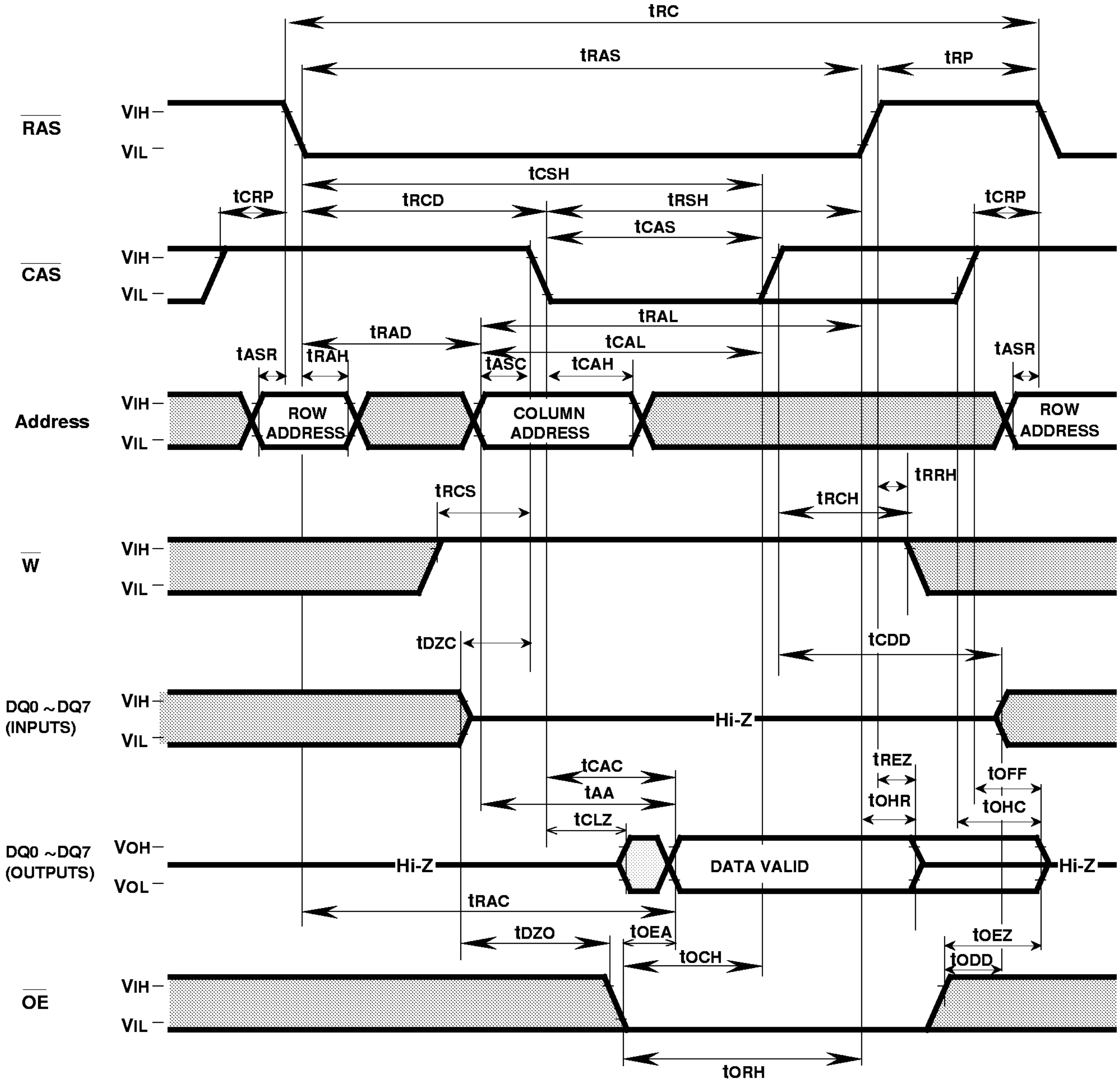
The last / first full refresh cycles must be made within tNS / tSN before / after self refresh , on the condition of tNS ≤ 128 ms and tSN ≤ 128 ms.

(2) In case of burst refresh

The last / first full refresh cycles must be made within tNS / tSN before / after self refresh , on the condition of tNS ≤ 16 ms and tSN ≤ 16 ms.

Timing Diagrams (Note 29)

Read Cycle

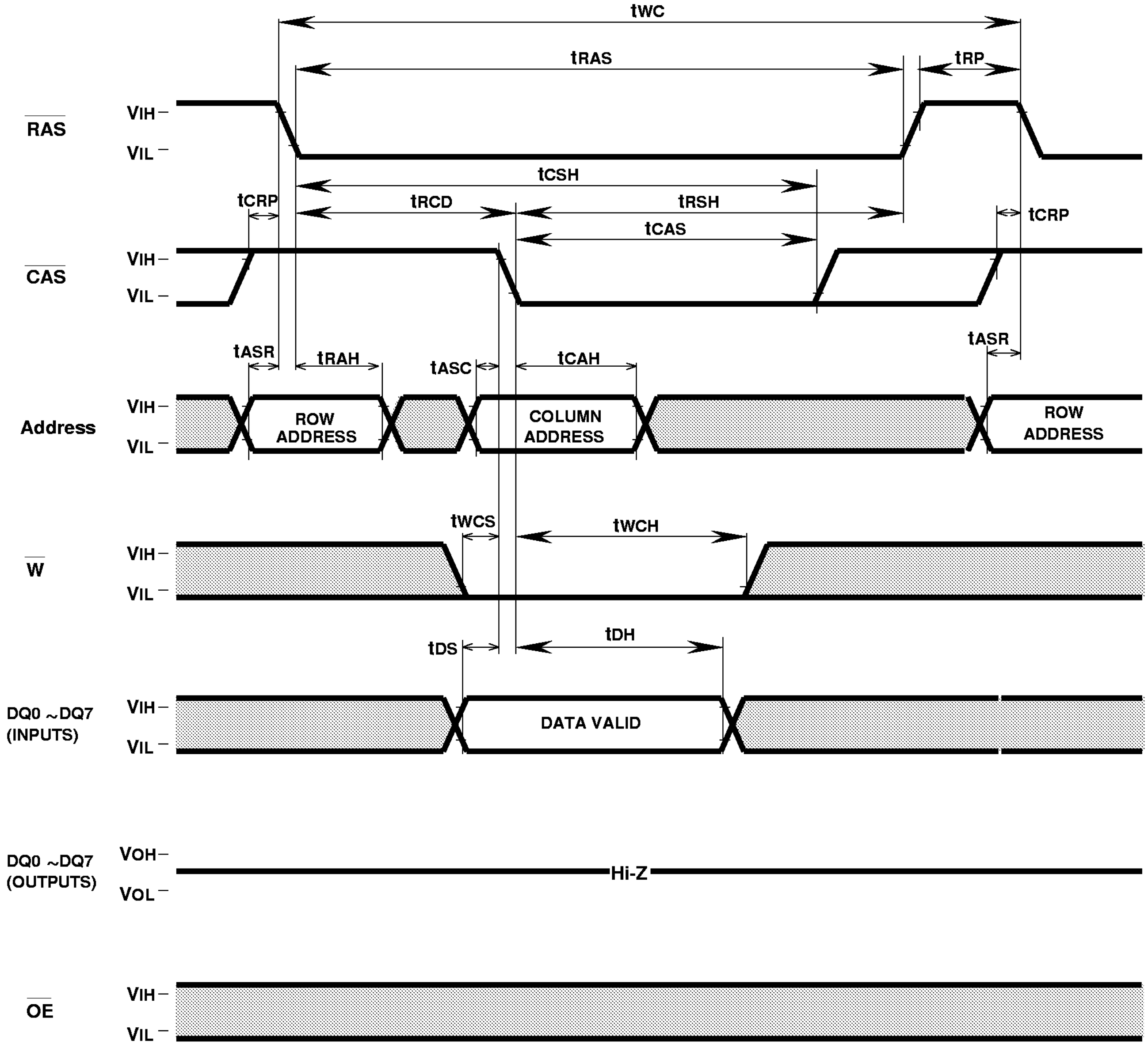


Note 29

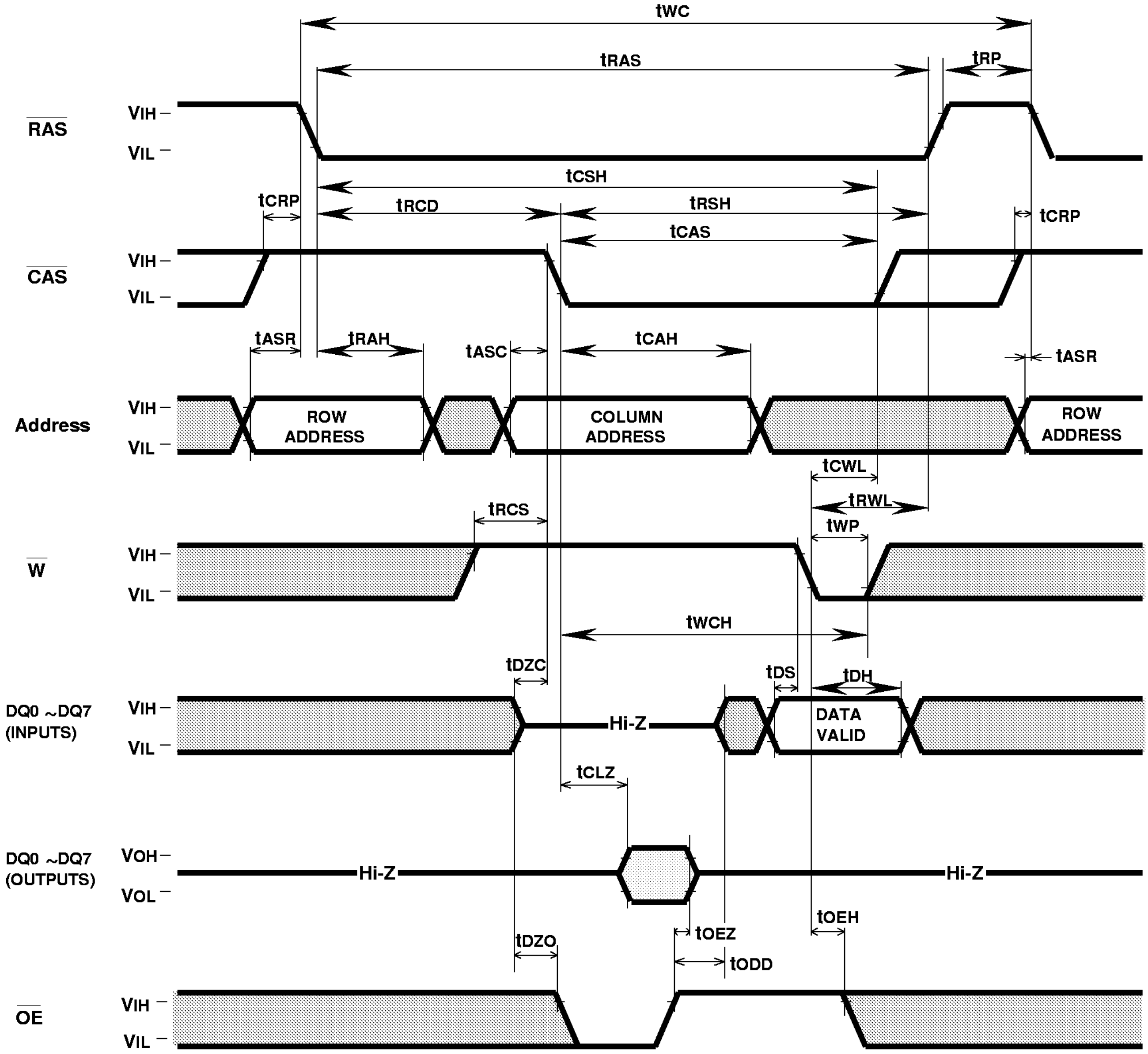
▨ Indicates the don't care input.
$V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$

░ Indicates the invalid output.

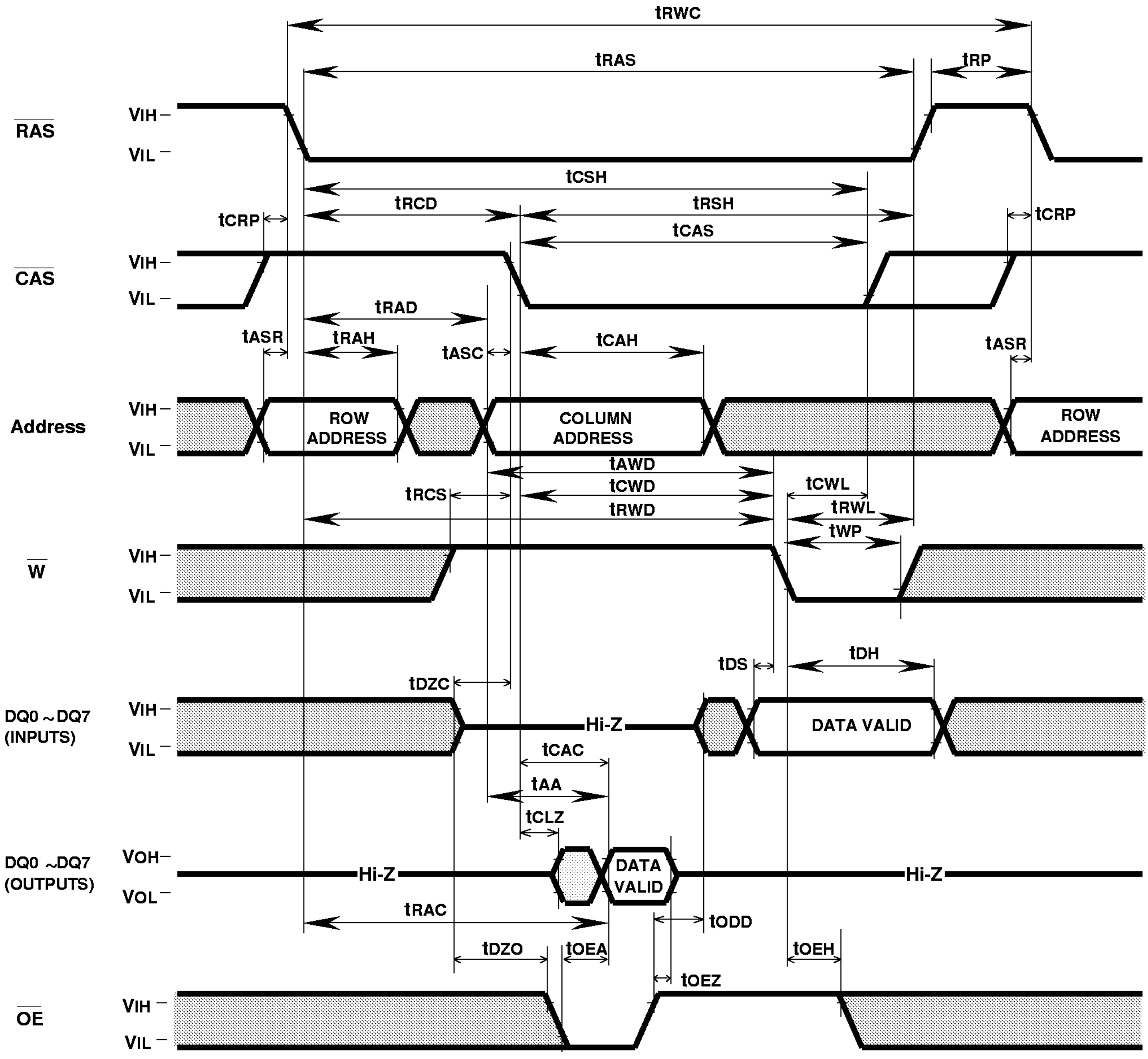
Early Write Cycle



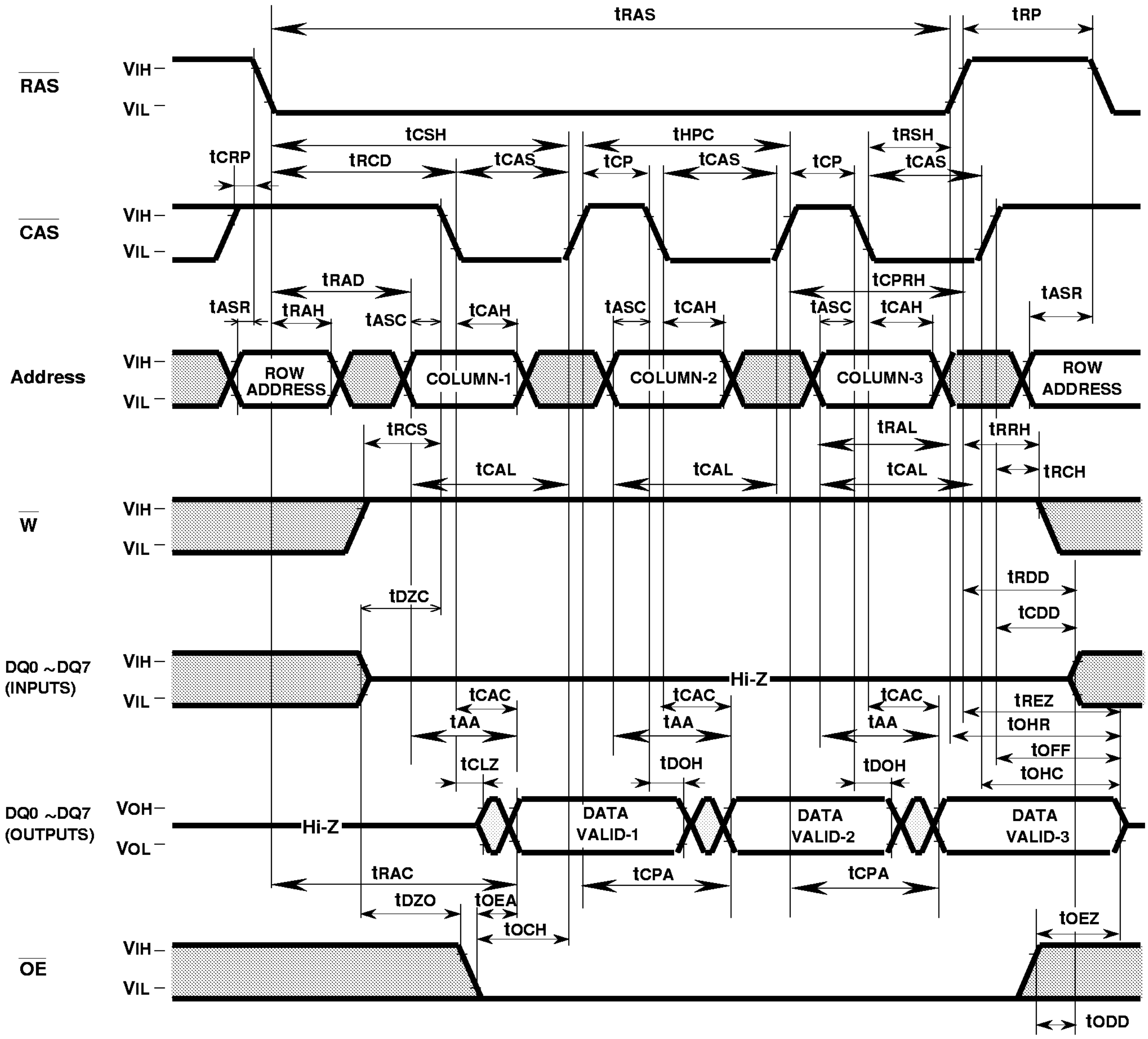
Delayed Write Cycle



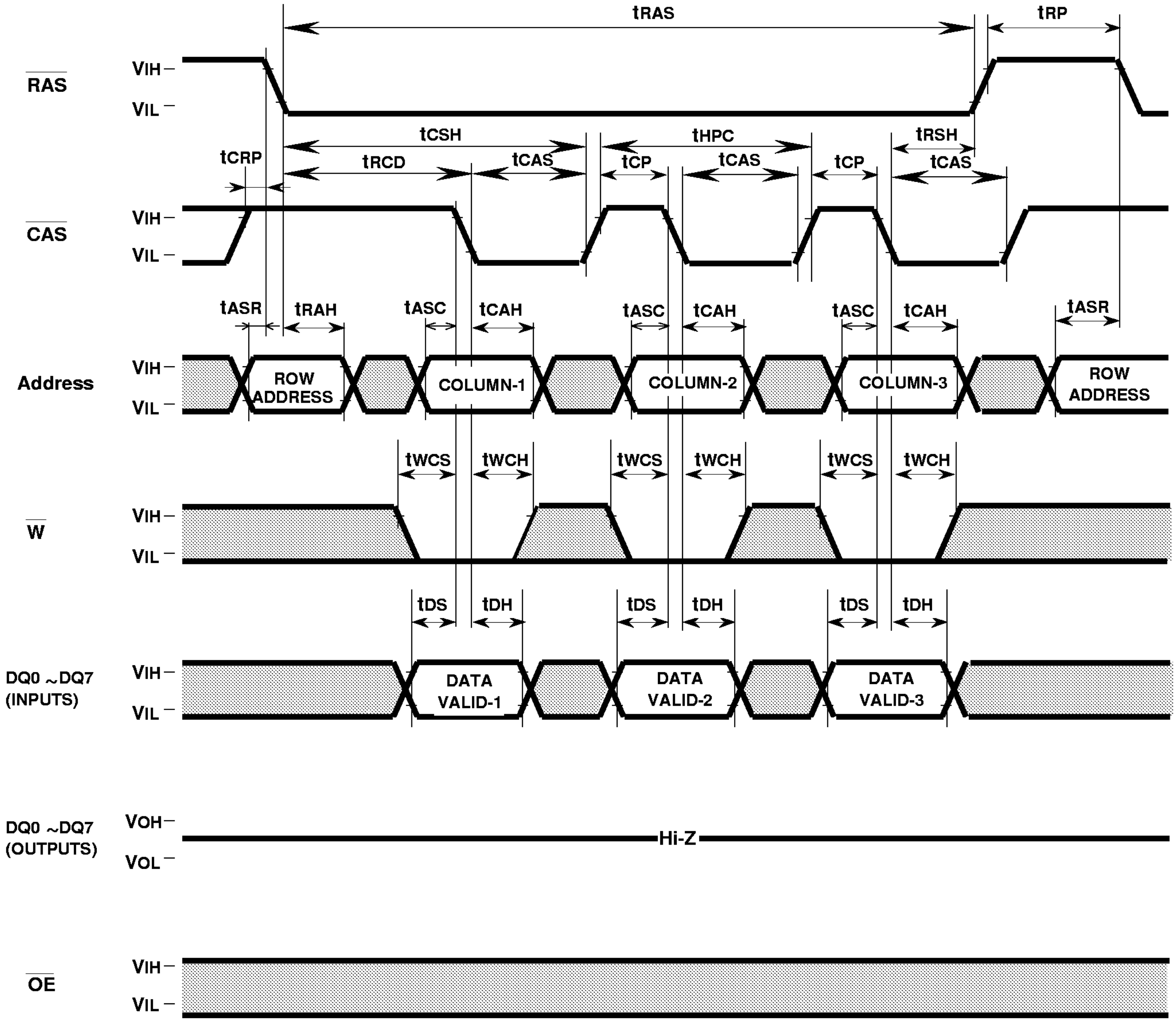
Read-Write, Read-Modify-Write Cycle



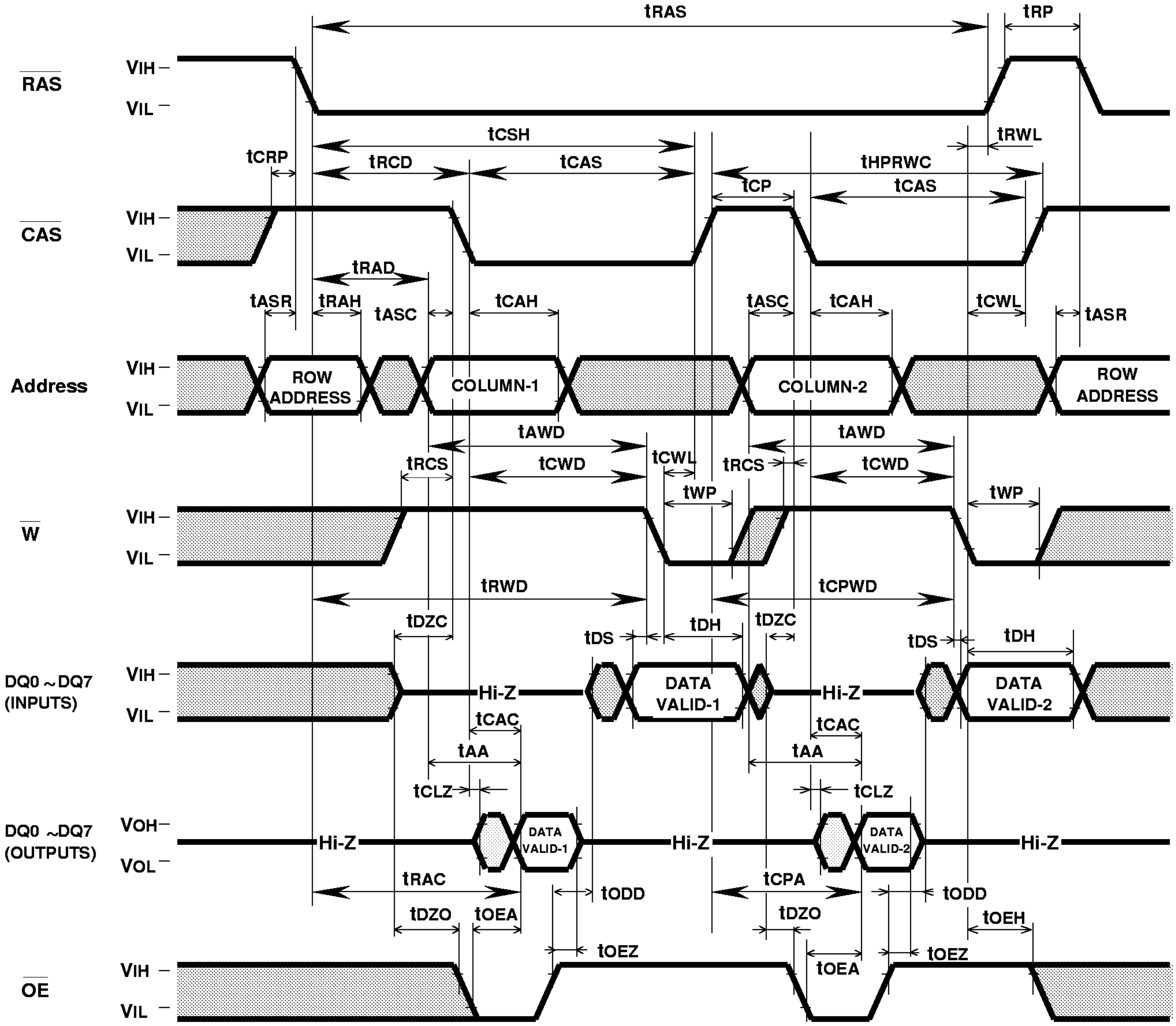
Hyper Page Mode Read Cycle



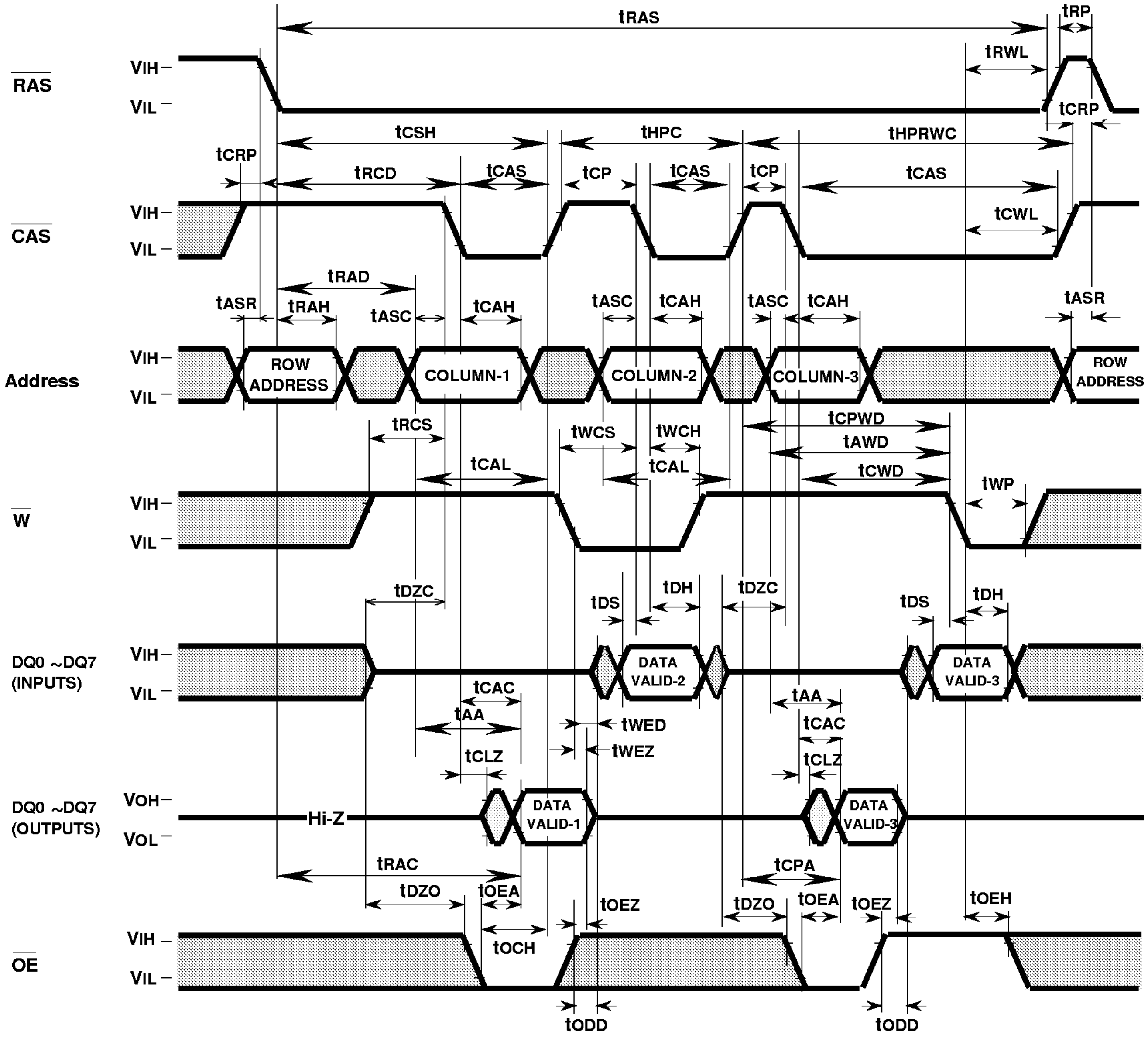
Hyper Page Mode Early Write Cycle



Hyper Page Mode Read-Write,Read-Modify-Write Cycle

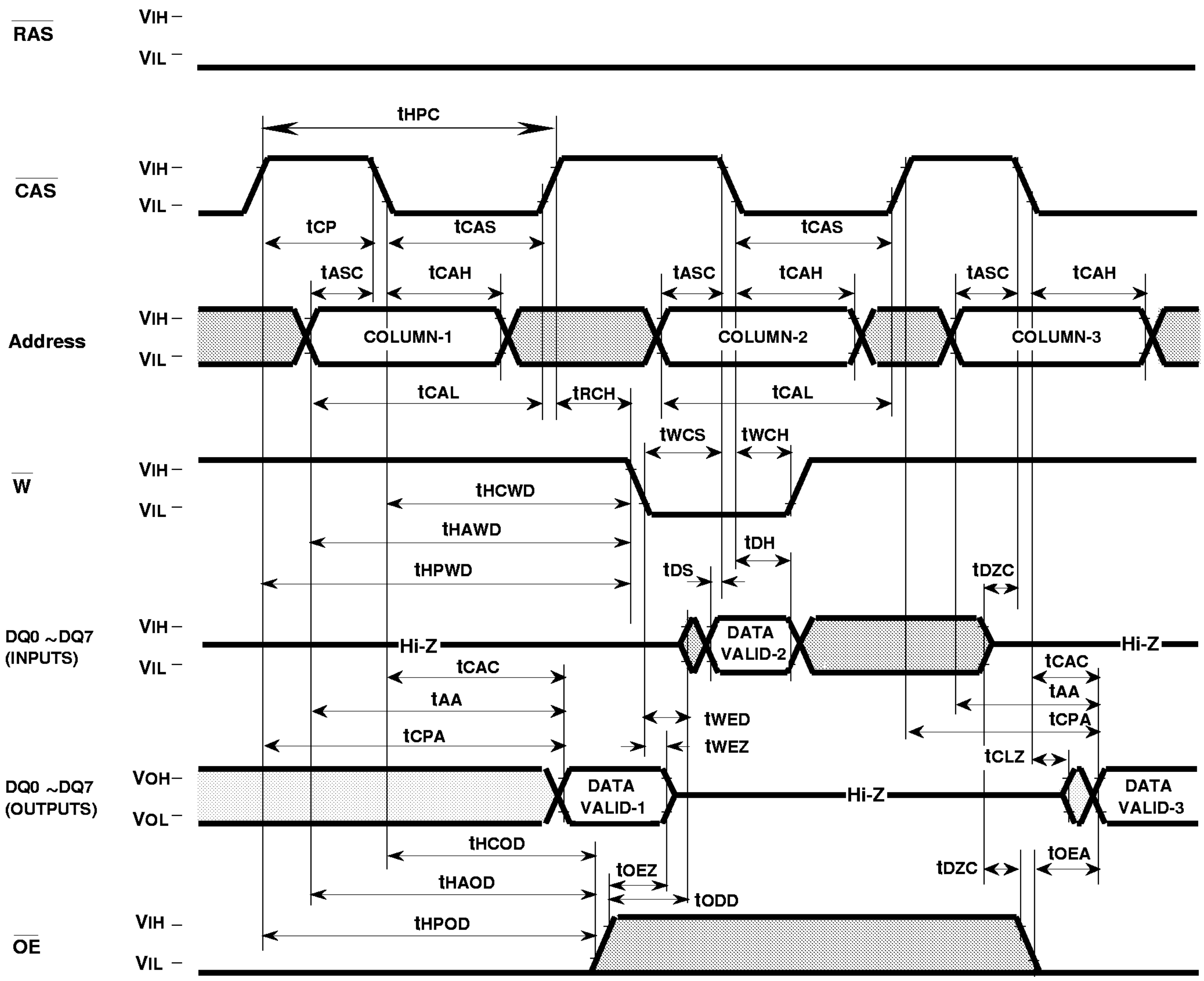


Hyper Page Mode Mix Cycle (1)



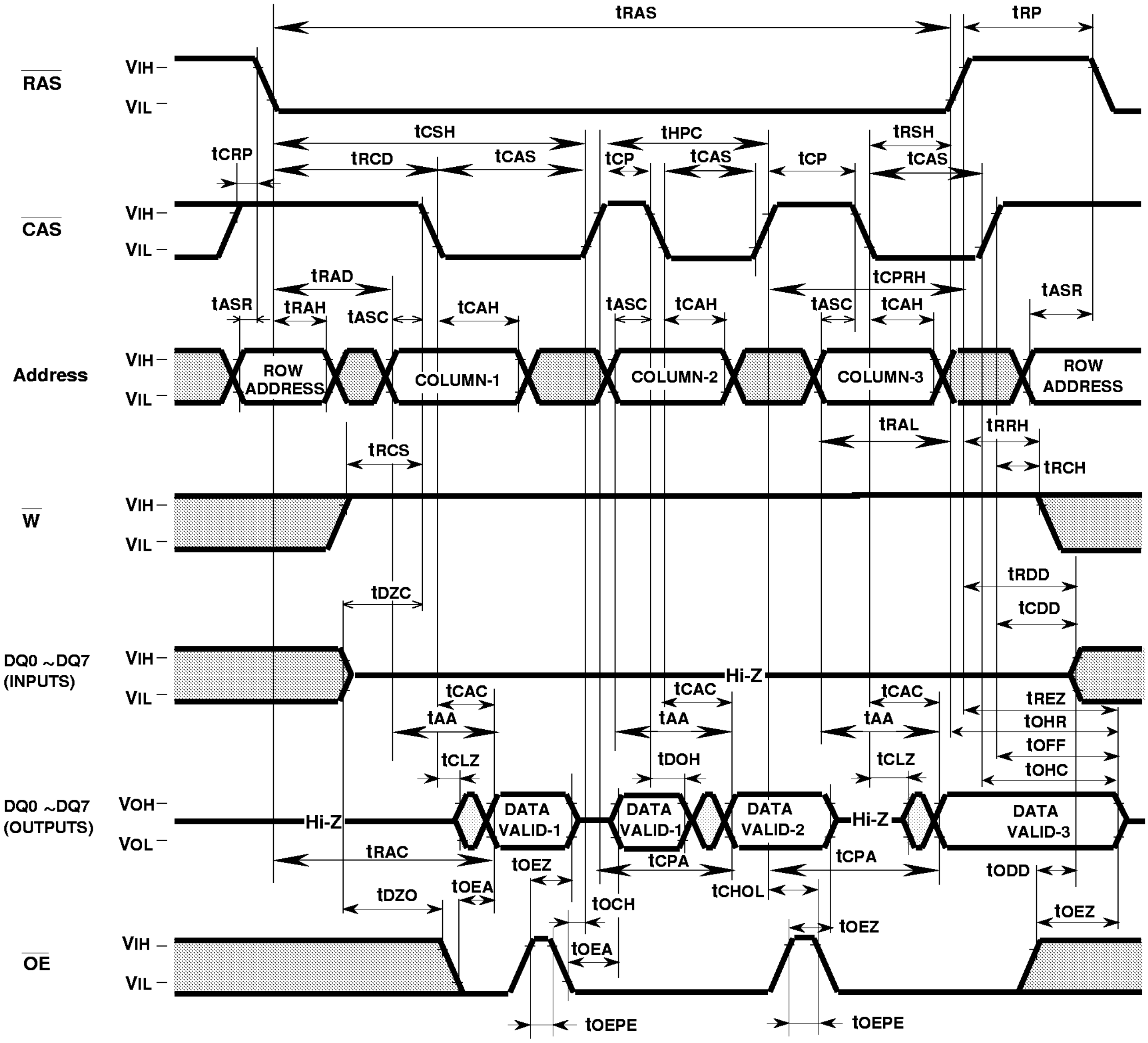
Note 30: $\overline{\text{OE}}$=L; $\overline{\text{WE}}$ Hi-Z control
$\overline{\text{OE}}$=H; $\overline{\text{OE}}$ Hi-Z control

Hyper Page Mode Mix Cycle (2)

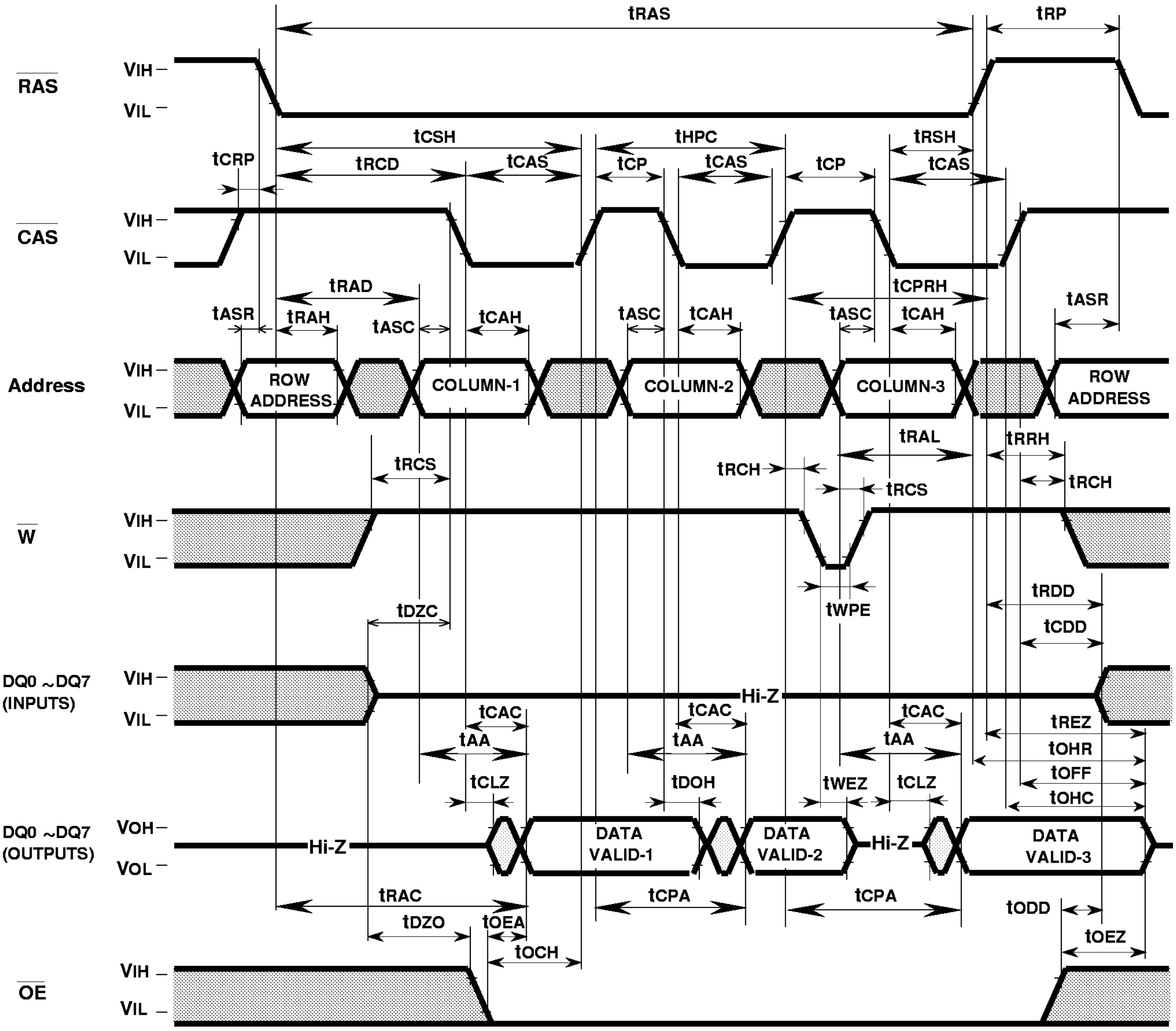


Note 30: $\overline{\text{OE}}$=L; $\overline{\text{WE}}$ Hi-Z control
$\overline{\text{OE}}$=H; $\overline{\text{OE}}$ Hi-Z control

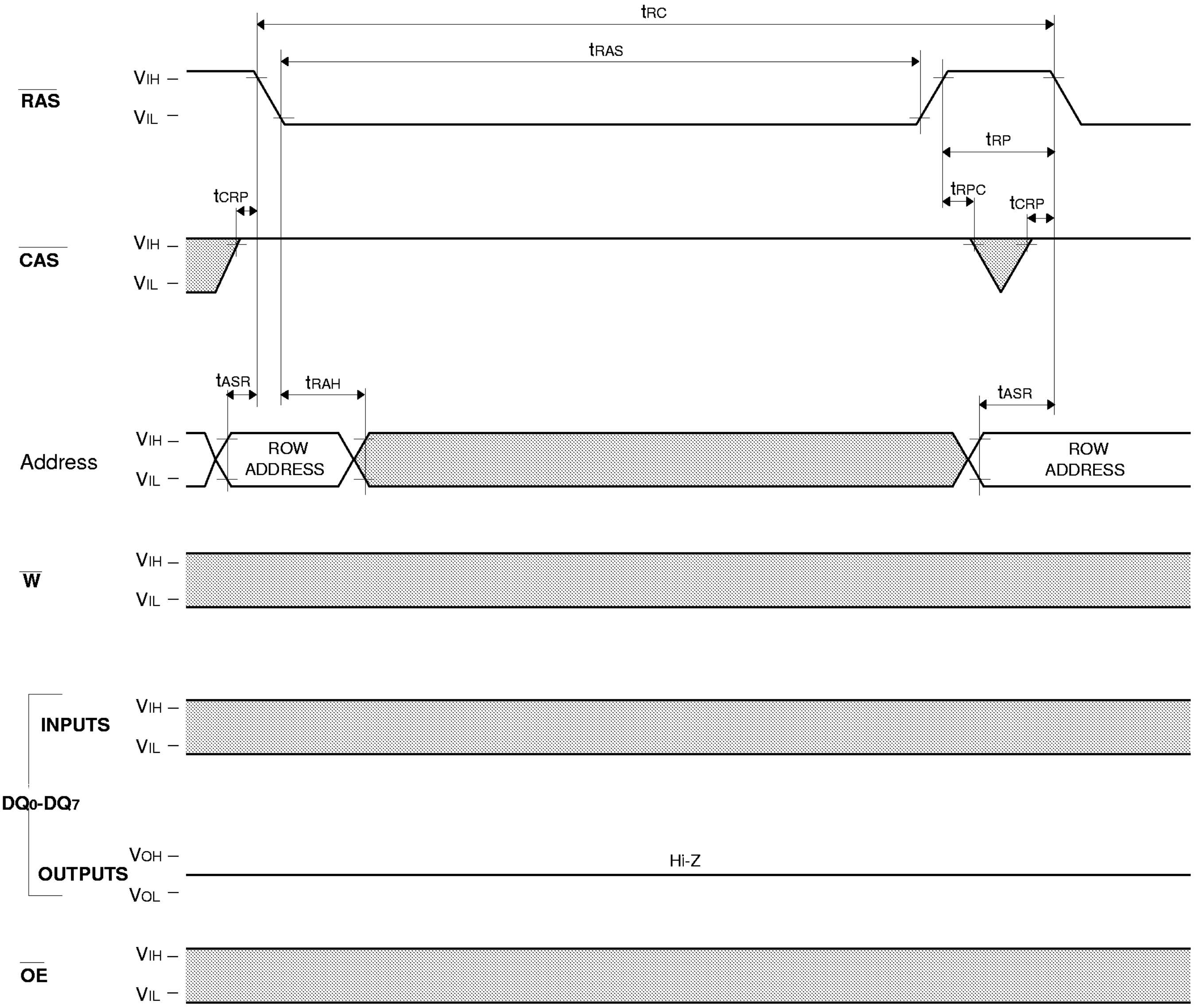
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



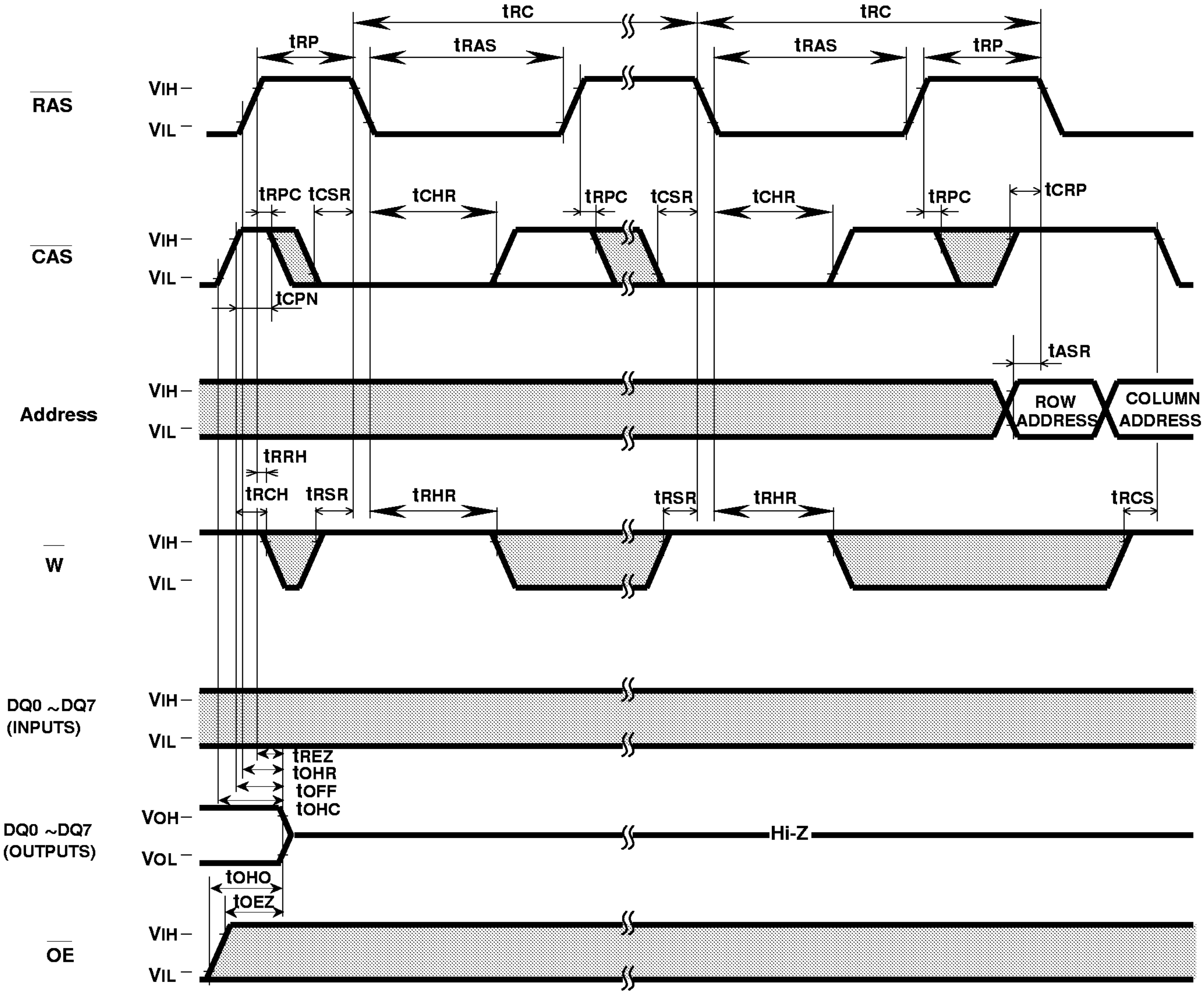
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



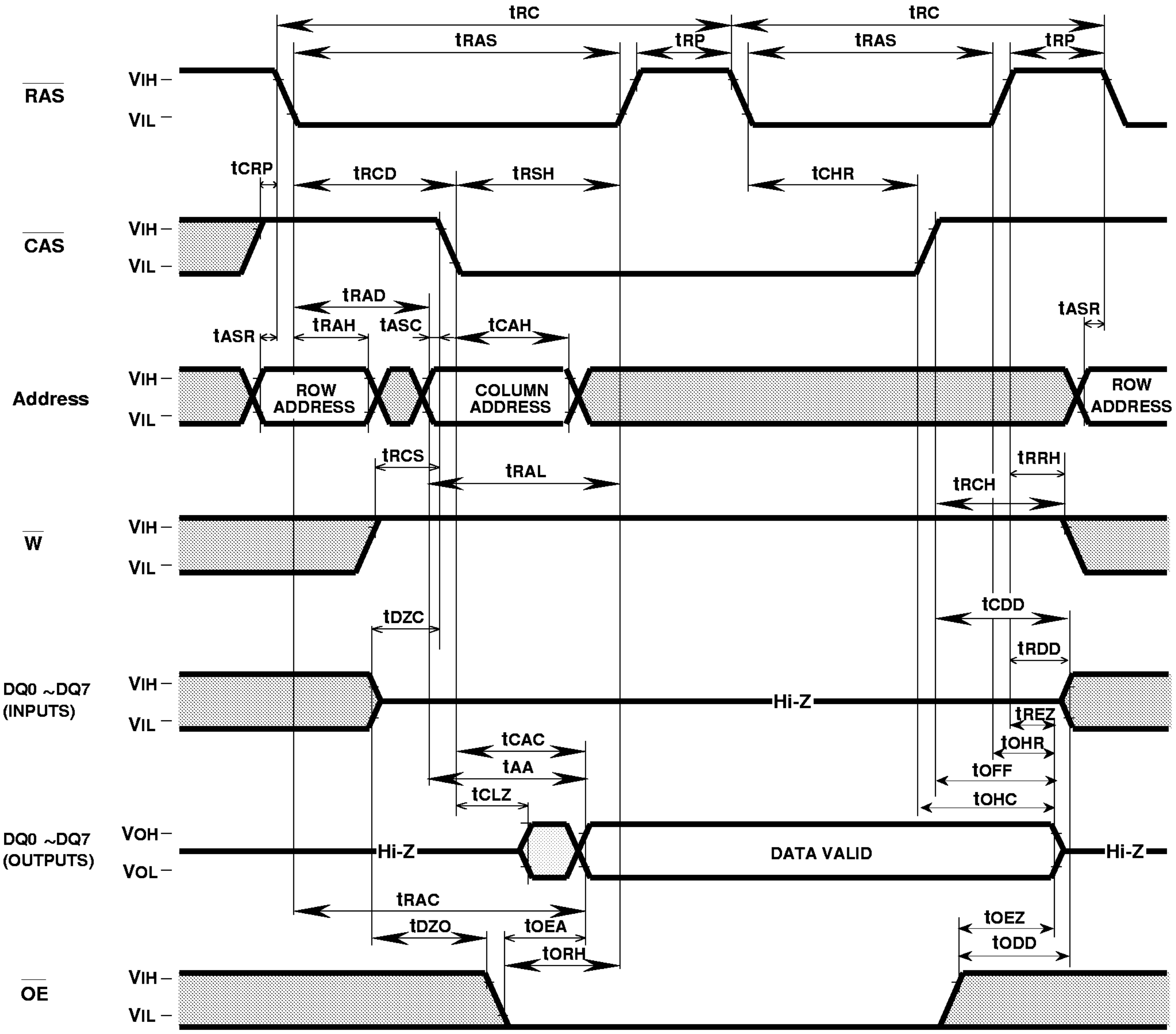
RAS-only Refresh Cycle



$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

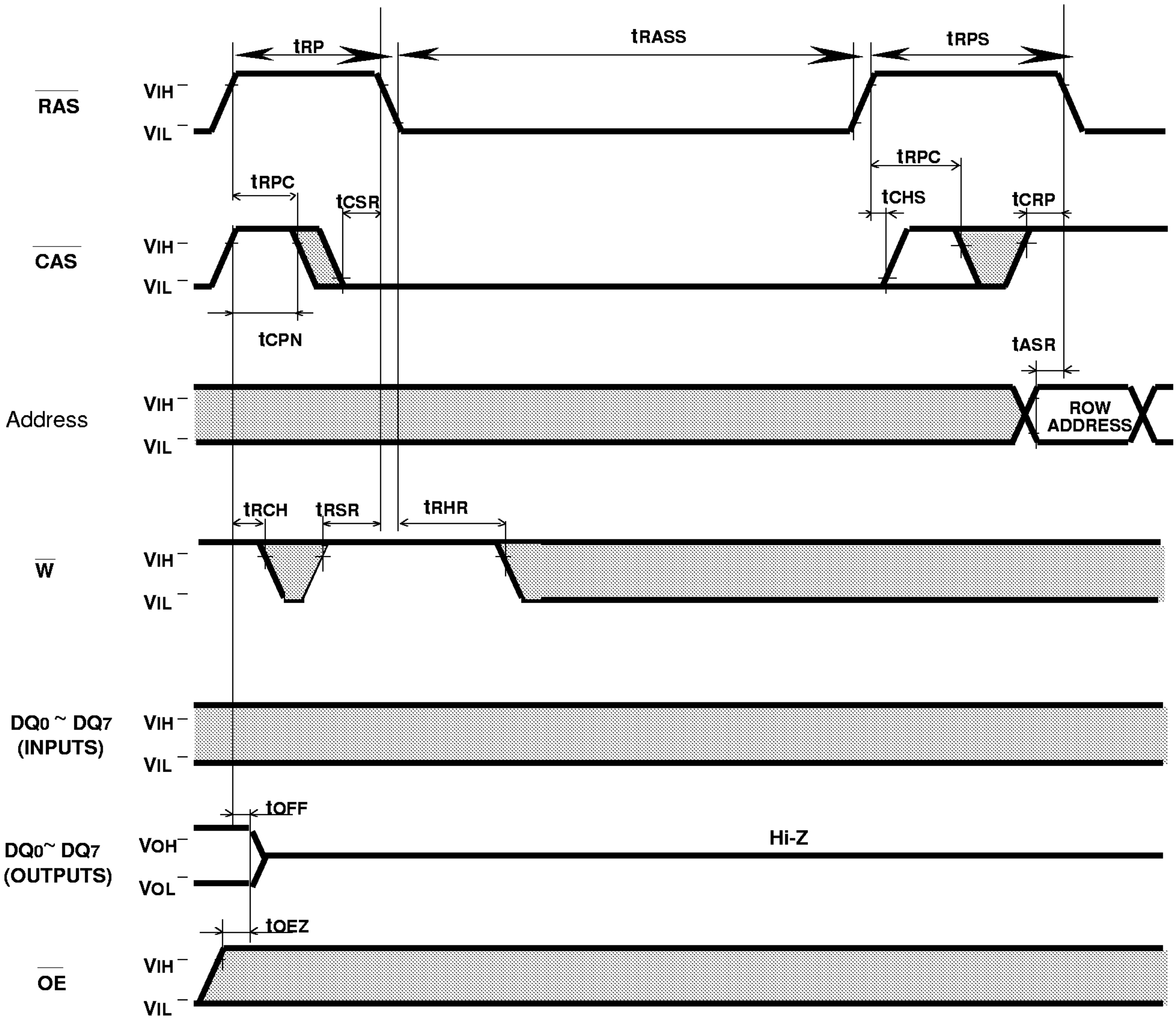


Hidden Refresh Cycle (Read) (Note 31)



Note 31: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle



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