

Features

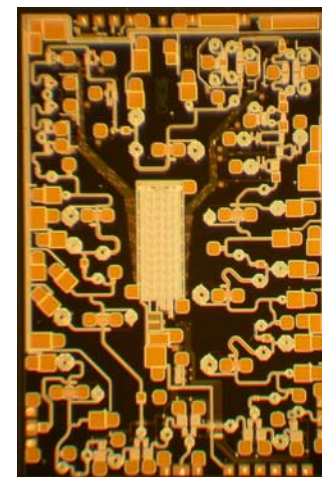
- ◆ **Highly Integrated MMIC**
 - ◊ Dual Path, Transmit/Receive Operation
 - ◊ 6-Bit Phase Shifter and 6-Bit Attenuator
 - ◊ Tx Gain = 28 dB; Rx Gain = 21 dB
 - ◊ Serial Control Data Input
- ◆ **50 Ω Input and Output Impedance**
- ◆ **Proven Manufacturability and Reliability**
 - ◊ No Airbridges
 - ◊ Polyimide Scratch Protection
 - ◊ No Hydrogen Poisoning Susceptibility

Description

The MAMFGM0001-DIE000 is a 3-port, dual path transmit/ receive control MMIC. The on-chip serial-to-parallel converter enables the independent control of the 6-bit phase shifter and 6-bit attenuator and minimizes the required inputs. This product is fully matched to 50 ohms on both the input and output.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG) Process, each device is 100% RF tested on-wafer to ensure performance compliance.

M/A-COM's MSAG process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



Primary Applications

- ◆ Radar Systems
- ◆ Commercial Avionics

Maximum Operating Conditions¹

Parameter	Symbol	Absolute Maximum	Units
Tx Input Power	Tx P _{IN}	2	dBm
Rx Input Power	Rx P _{IN}	5	dBm
Drain Supply Voltage	V _{DD}	12.0	V
Gate Supply Voltage	V _{GG}	-6.0	V
Quiescent Drain Current (No RF)	I _{DQ}	500	mA
Quiescent DC Power Dissipated (No RF)	P _{DISS}	2.5	W
Logic Supply Voltage	V _{EE}	-6.0	V
Junction Temperature	T _J	170	°C
Storage Temperature	T _{STG}	-55 to +150	°C

1. Operation beyond these limits may result in permanent damage to the part.

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Visit www.macom.com for additional data sheets and product information.

Control Chip, X-Band T/R
7.0—12.0 GHz

MAMFGM0001-DIE
Rev C
Preliminary Datasheet

Recommended Operating Conditions²

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V _{DD}	4.8	5.0	5.2	V
Gate Supply Voltage	V _{GG}	-5.2	-5.0	-4.8	V
Digital Supply Voltage	V _{EE}	-5.2	-5.0	-4.8	V
Input Logic High Voltage	V _{IH}	3.0	5.0	5.0	V
Input Logic Low Voltage	V _{IL}	0.0	0.0	0.4	V
Clock Frequency	F _{CLK}		20		MHz
Thermal Resistance	Θ _{JC}		25.6		°C/W
MMIC Base Temperature	T _B			Note 3	°C

2. Operation outside of these ranges may reduce product reliability.

3. Maximum MMIC Base Temperature = 170°C — Θ_{JC} * V_{DD} * I_{DQ}

Electrical Characteristics: T_B = 25°C⁴, Z₀ = 50Ω, V_D = 5V, V_G = -5V, V_{EE} = -5V

Parameter	Symbol	Typical (@ 9.5 GHz)	Units
Bandwidth	f	7.0-12.0	GHz
Transmit Gain	G _n	28	dB
Receive Gain	G _n	21	dB
Input VSWR, Common Port, Transmit	VSWR	1.5:1	
Output VSWR, Tx Out Port, Transmit	VSWR	1.7:1	
Input VSWR, Rx In Port, Receive	VSWR	1.6:1	
Output VSWR, Common Port, Receive	VSWR	1.4:1	
Transmit P1dB	P1dB	22	dBm
Receive P1dB	P1dB	18	dBm
Receive Third Order Intercept, Output	OTOI	26	dBm
Receive Noise Figure	NF	10.5	dB
Attenuator Range (6 bits, 64 states)		0 to 31.5	dB
0.5 dB Bit, Relative Gain, LSB		-0.5	dB
1 dB Bit, Relative Gain		-1.0	dB
2 dB Bit, Relative Gain		-2.0	dB
4 dB Bit, Relative Gain		-4.0	dB
8 dB Bit, Relative Gain		-8.0	dB
16 dB Bit, Relative Gain, MSB		-16.0	dB
Phase Shifter Range (6 bits, 64 states)		0 to 354	°
5.6 ° Bit, Relative Phase, LSB		-5.6	°
11.2° Bit, Relative Phase		-11.2	°
22.5° Bit, Relative Phase		-22.5	°
45° Bit, Relative Phase		-45	°
90° Bit, Relative Phase		-90	°
180° Bit, Relative Phase, MSB		-180	°
Gate Supply Current	I _{GG}	10	mA
Drain Supply Current	I _{DD}	400	mA
Logic Supply Current	I _{EE}	50	mA

4. T_B = MMIC Base Temperature

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MAMFGM0001-DIE

Rev C

Preliminary Datasheet

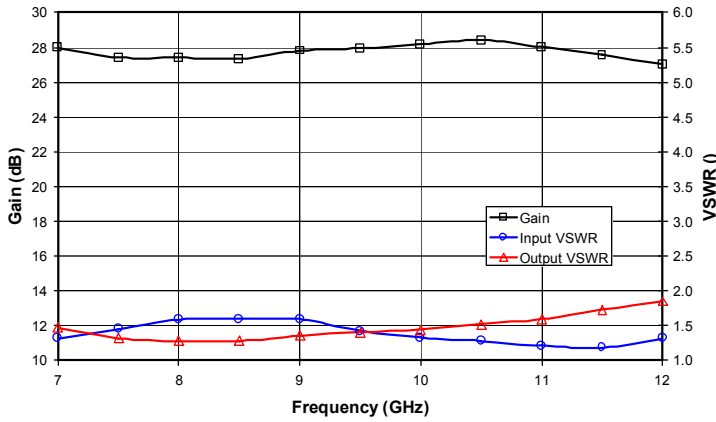


Figure 1. Transmit S-Parameters

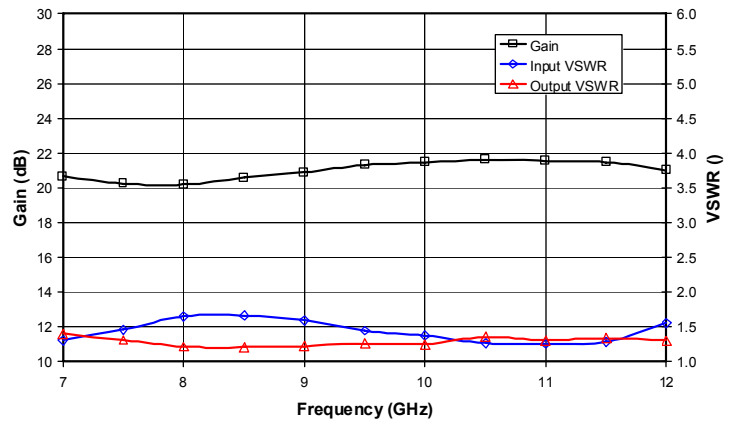


Figure 2. Receive S-Parameters

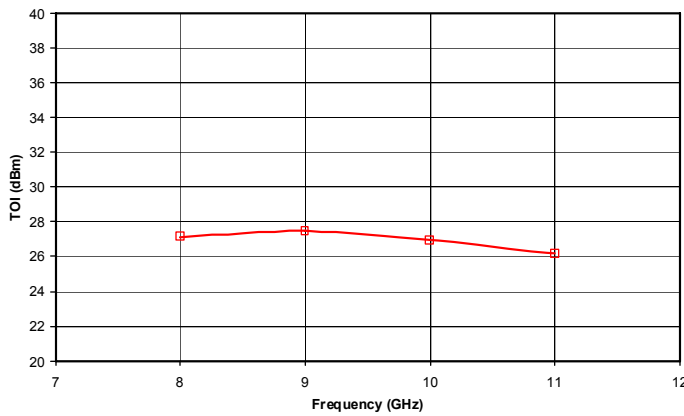


Figure 3. Receive Output TOI

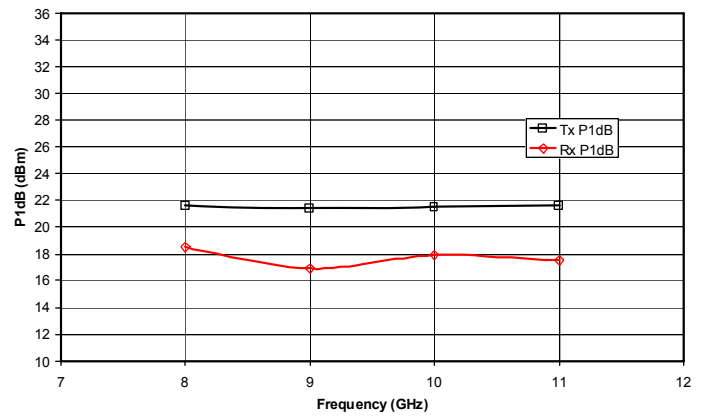


Figure 4. Transmit and Receive P1dB

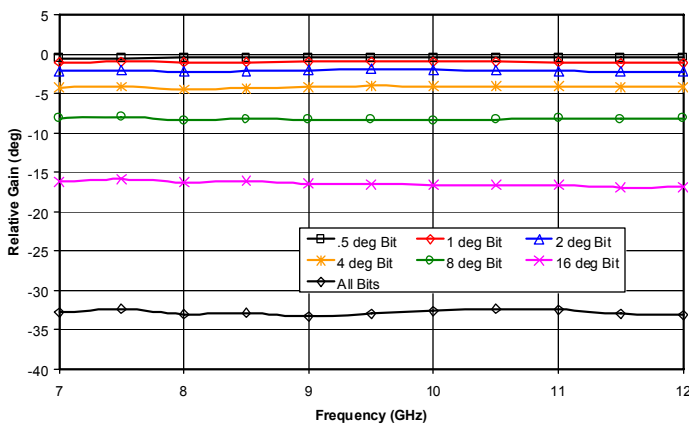


Figure 5. Relative Gain of Major Attenuator States

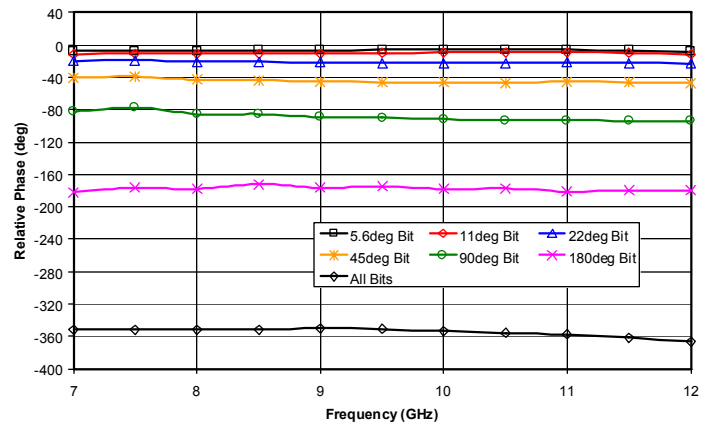


Figure 6. Relative Phase of Major Phase Shifter States

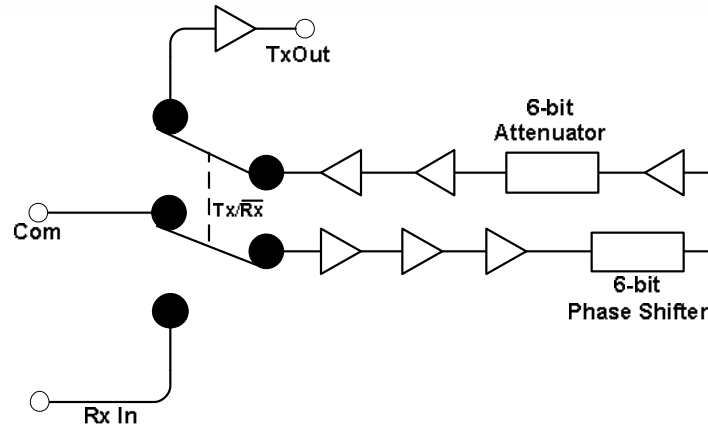


Figure 7. Block Diagram of Transmit/Receive Control MMIC

Truth Table and Data Sequence

X-Band T/R MMIC Control Function		
INPUT SIGNAL	LOGIC LEVEL	FUNCTION
CK (Clock)	Falling Edge	Shifts the data, DI
DI (Data In)	High/Low	Phase and Attn Setting
LD (Load)	Falling Edge	Loads the data from D24 Shift Register
SL and TR (Select & T/R Control)	Low	Selects odd bits (Transmit) and Transmit Path
SL and TR (Select & T/R Control)	High	Selects even bits (Receive) and Receive Path
Logic Level	Logic High	Logic 1: 3.0 to 5V
	Logic Low	Logic 0: 0 to 0.4V
Attn and Phase States	Logic Low	Phase and Attn in Ref. State
	Logic High	Phase and Attn Shift Negative
LSB data enters first and MSB enters last. LSB data travels all 24 shift registers.		

Serial-to-Parallel Converter I/Os						
Input Data to SPC	TR "Low" – TX TR "High" – RX	Phase and Attn		Input Data to SPC	TR "Low" – TX TR "High" – RX	Phase and Attn
D1-LSB	Transmit	5.6°-bit PS		D13	Transmit	0.5 dB-bit Attn
D2	Receive			D13	Receive	
D3	Transmit	11 °-bit PS		D15	Transmit	1 dB-bit Attn
D4	Receive			D16	Receive	
D5	Transmit	22 °-bit PS		D17	Transmit	2 dB-bit Attn
D6	Receive			D18	Receive	
D7	Transmit	45 °-bit PS		D19	Transmit	4 dB-bit Attn
D8	Receive			D20	Receive	
D9	Transmit	90 °-bit PS		D21	Transmit	8 dB-bit Attn
D10	Receive			D22	Receive	
D11	Transmit	180 °-bit PS		D23	Transmit	16 dB-bit Attn
D12	Receive			D24	Receive	

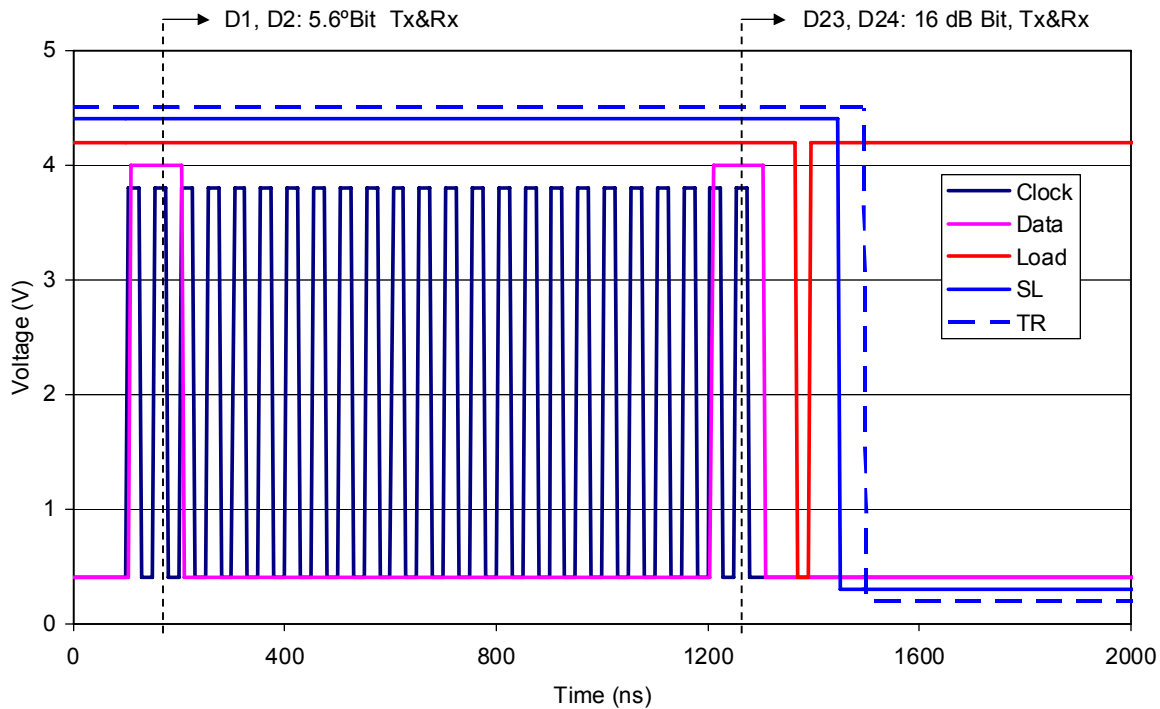


Figure 8. Timing Diagram, Data Sequence

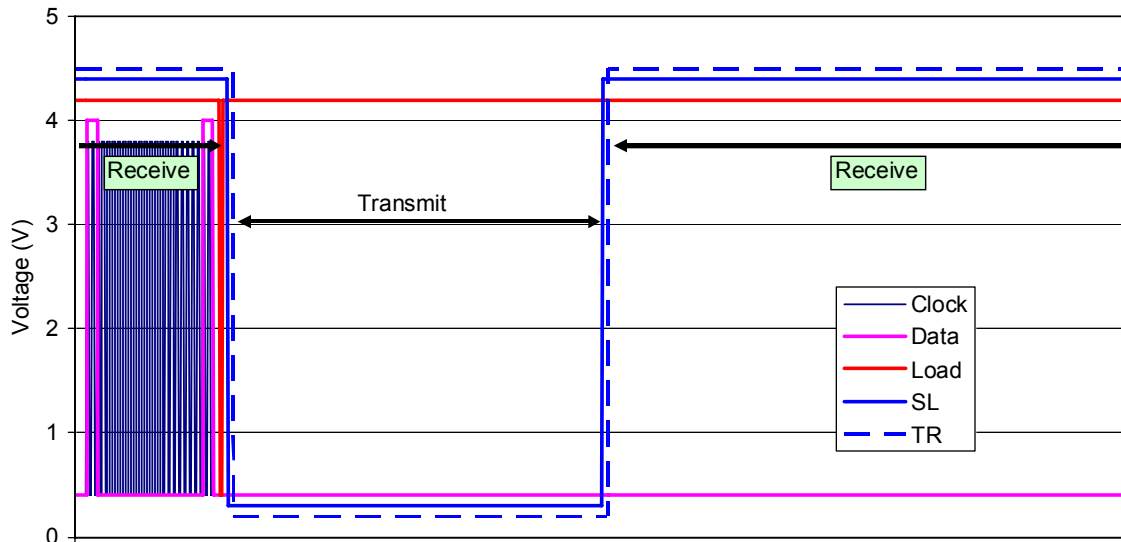


Figure 9. Timing Diagram, Transmit/Receive Relationship

Mechanical Information

Chip Size: 6.0 x 4.0 x 0.075 mm (236 x 157 x 3 mils)

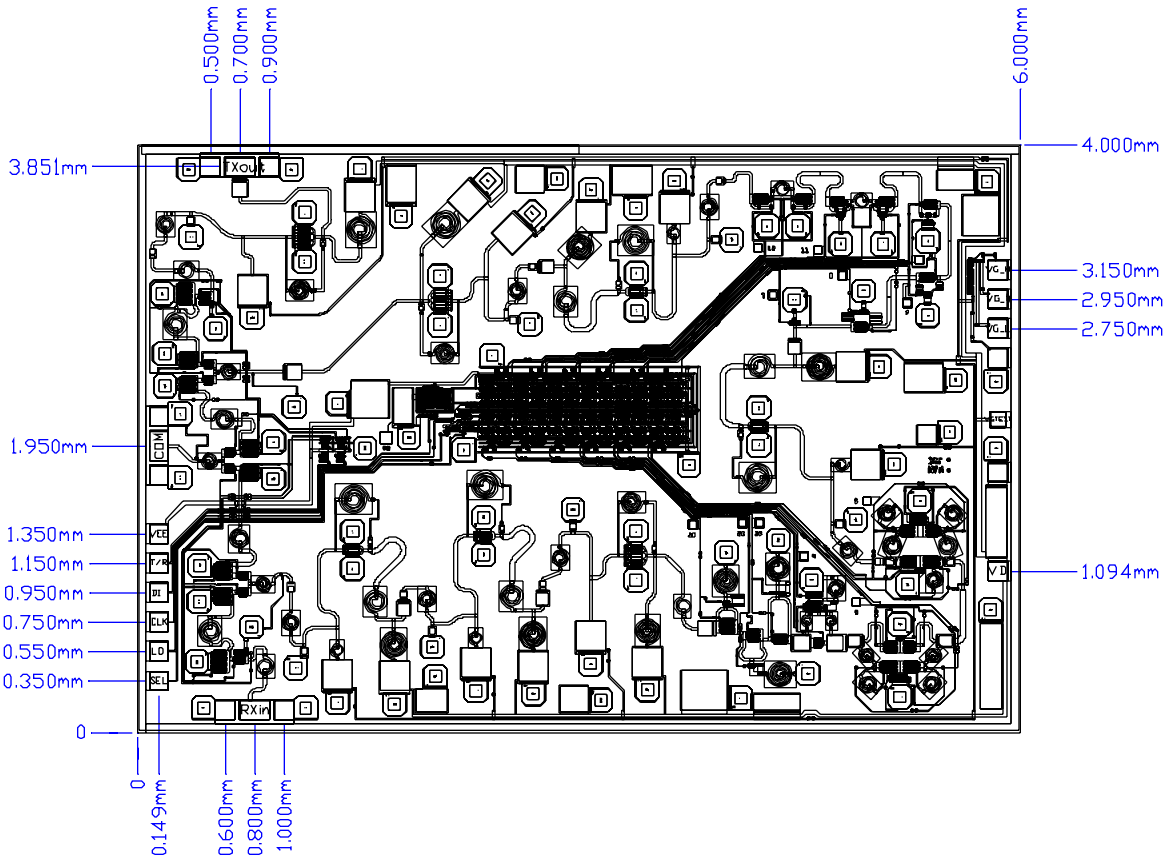


Figure 10 . Die Layout

Bond Pad Information

Pad	Type	Nominal Voltage	Size	
			(μm)	(mils)
Common, Tx Out, Rx In	RF	N/A	150 x 150	6 x 6
T/R, Sel, Load, Data, Clock	Control	0 / 5 V	125 x 125	5 x 5
V _{DD}	DC	5.0 V	150 x 150	6 x 6
V _{EE}	DC	-5.0 V	125 x 125	5 x 5
V _{G-HI} , V _{G-N} , V _{G-LO}	DC	-5.0 V	150 x 150	6 x 6

Assembly and Bonding Diagram

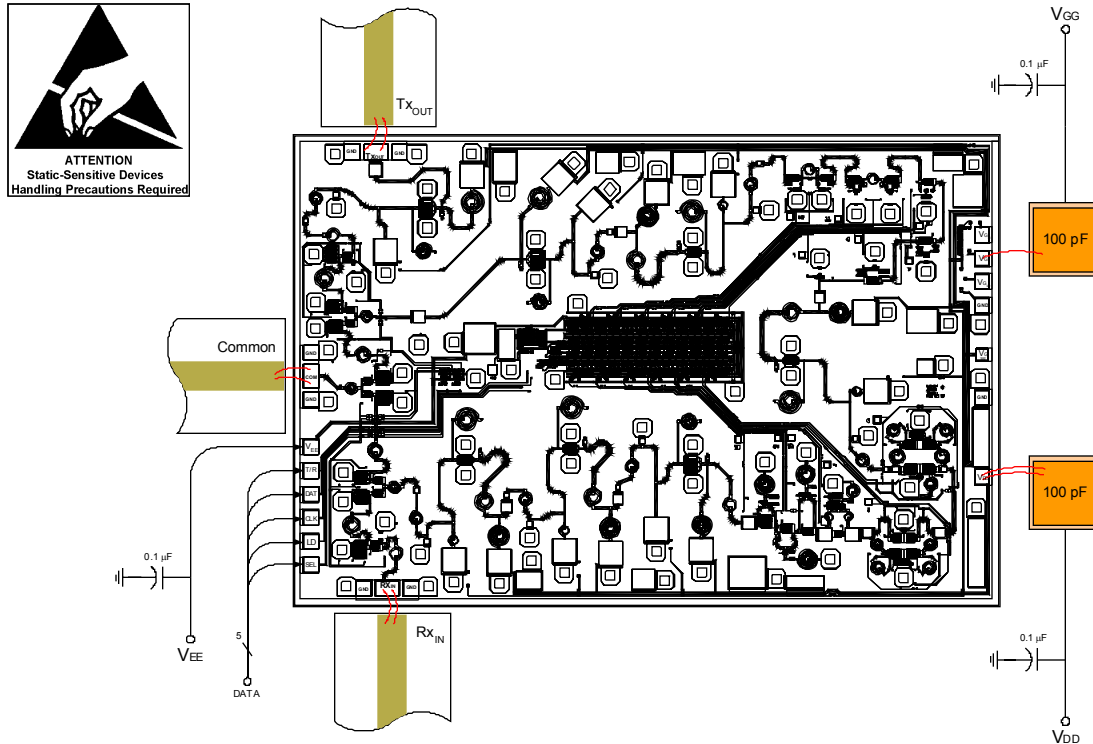


Figure 11. Recommended bonding diagram.
Support circuitry typical of MMIC characterization fixture for CW testing.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply $V_{GG} = -5$ V, $V_{EE} = -5$ V, $V_{DD} = 0$ V.
2. Ramp V_{DD} to desired voltage, typically 5 V.
3. Adjust V_{GG} to set I_{DQ} .
4. Set RF input.
5. Power down in reverse. Turn V_{GG} off last.

