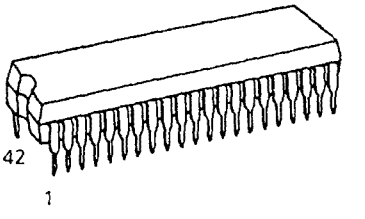
TC5092AP

(13 - BIT A - D CONVERTER)

1. GENERAL DESCRIPTION

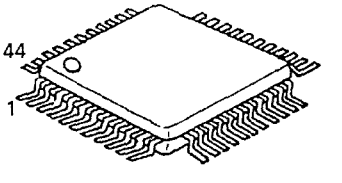
The TC5092AP/AF is an integration 13-bit A-D converter of high precision and low power consumption. The 13-bit , 3-state data output is capable of independent enable in 4 bits so as to be connected directly to 4-bit / 8-bit / 12-bit data bus. (LSB is common to lower order 4 bits.)

Further, since this converter has an 8-channel analog multiplexer, and a serial clock output function, it is most suitable as data collection unit of various industrial control instruments.



DIP42 - P - 600

Under Development



QFP44 - P - 1414D

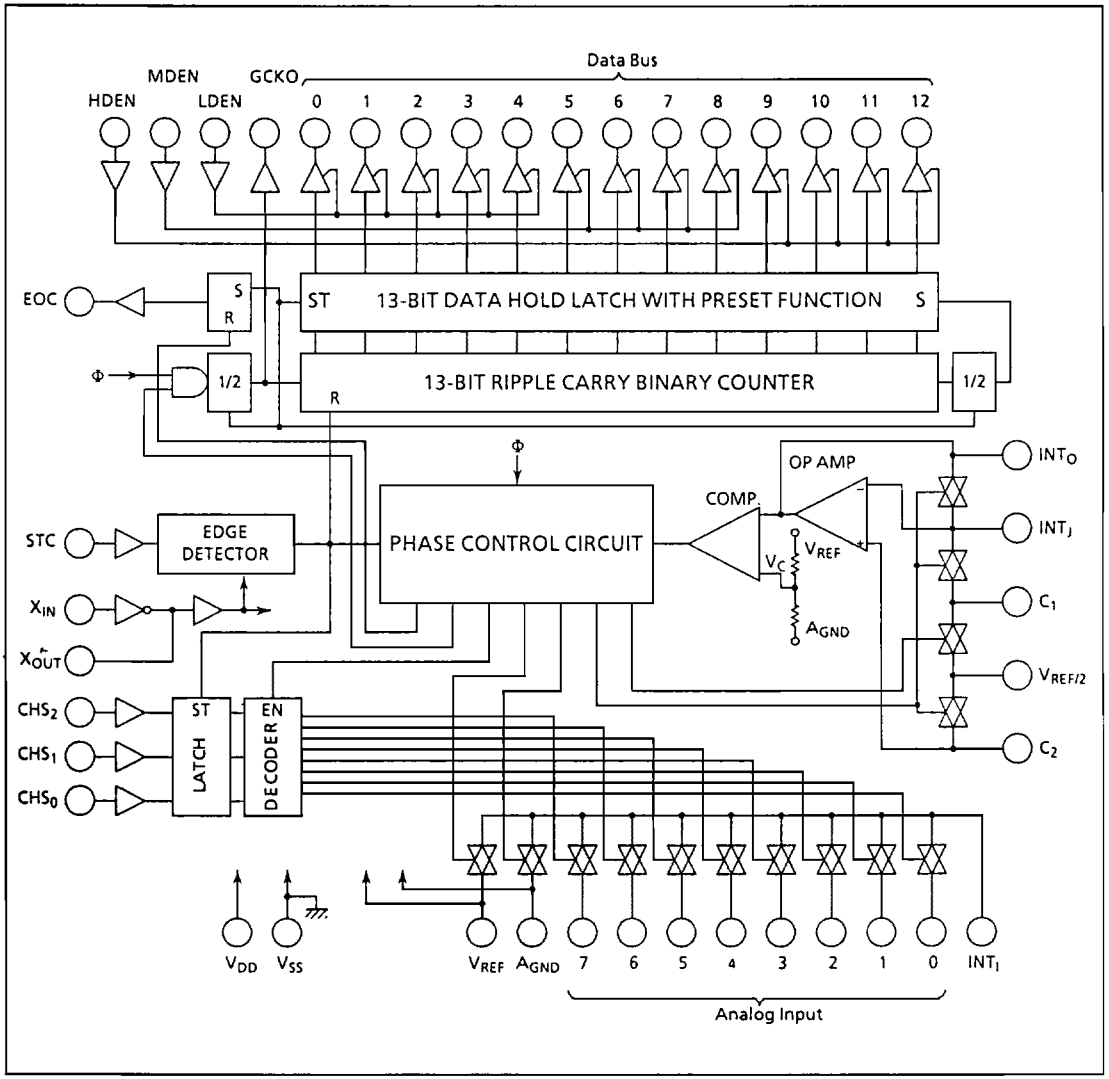
2. FEATURES

- ☐ High precision ..... ±1 LSB (Typ.)
- ☐ Low power consumption ... 10 mW (Typ.)
- ☐ Single power supply ..... V_{DD} = 5 V ± 0.5 V
- ☐ High-speed conversion .... f_{cp} Max. = 5 MHz
- ☐ 8 - channel analog multiplexer contained
- ☐ TTL / CMOS compatible digital Input / Output
- ☐ Capable of direct connection to 4 - / 8 - / 12 - bit bus

2.1 APPLICATIONS

- ☐ Various industrial control instruments
- ☐ Data collection modules

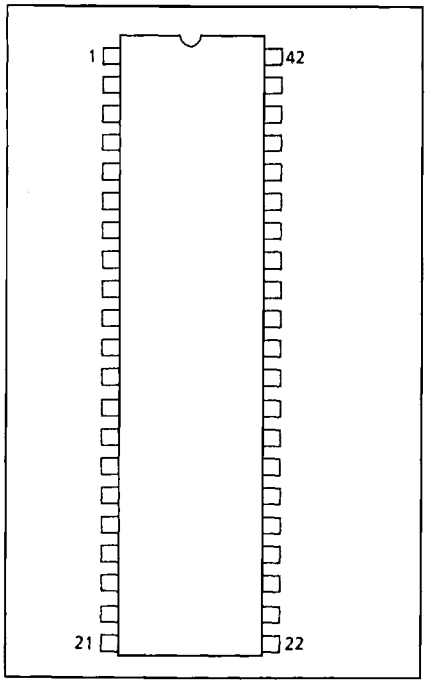
3. SYSTEM DESCRIPTION



4. PIN DESCRIPTION

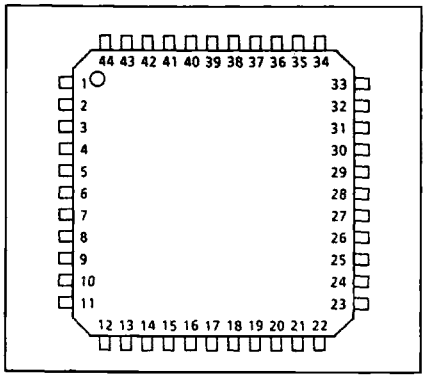
4.1 PIN ASSIGNMENT

TC5092AP



No.	PIN NAME	No.	PIN NAME
1	DB12	22	A_{GND}
2	DB11	23	$1/2\,V_{REF}$
3	DB10	24	V_{REF}
4	DB 9	25	A_{IN7}
5	DB 8	26	A_{IN6}
6	DB 7	27	A_{IN5}
7	DB 6	28	A_{IN4}
8	DB 5	29	A_{IN3}
9	DB 4	30	A_{IN2}
10	DB 3	31	A_{IN1}
11	DB 2	32	A_{IN0}
12	DB 1	33	INT_I
13	DB 0	34	INT_J
14	EOC	35	INT_O
15	LDEN	36	C_2
16	MDEN	37	C_1
17	STC	38	HDEN
18	CHS_2	39	GCKO
19	CHS_1	40	X_{OUT}
20	CHS_0	41	X_{IN}
21	V_{SS}	42	V_{DD}

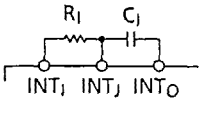
TC5092AF



No.	PIN NAME	No.	PIN NAME
1	DB 7	23	A_{IN4}
2	DB 6	24	A_{IN3}
3	DB 5	25	A_{IN2}
4	DB 4	26	A_{IN1}
5	DB 3	27	A_{IN0}
6	DB 2	28	INT_I
7	DB 1	29	INT_J
8	DB 0	30	INT_O
9	EOC	31	C_2
10	LDEN	32	C_1
11	MDEN	33	HDEN
12	STC	34	NC
13	CHS_2	35	GCKO
14	CHS_1	36	X_{OUT}
15	CHS_0	37	X_{IN}
16	V_{SS}	38	V_{DD}
17	A_{GND}	39	DB12
18	$1/2V_{REF}$	40	DB11
19	V_{REF}	41	DB10
20	A_{IN7}	42	DB 9
21	A_{IN6}	43	DB 8
22	A_{IN5}	44	NC

4.2 PIN DESCRIPTION

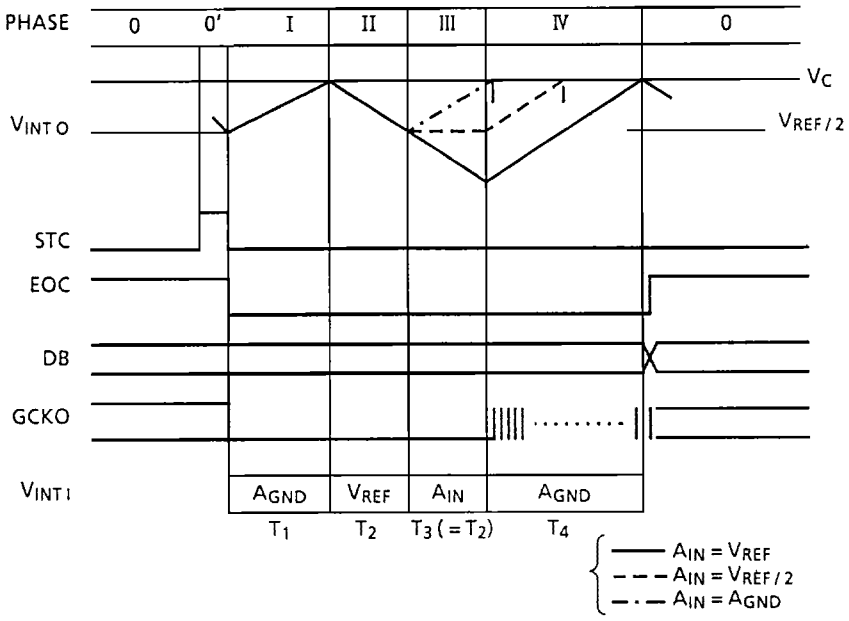
PIN No. DIP	PIN No. QFP	Symbol	NAME & FUNCTION
1	39	DB12	3 - state Parallel Data Outputs DB12 : MSB DB 0 : LSB
2	40	DB11	
3	41	DB10	
4	42	DB 9	
5	43	DB 8	
6	1	DB 7	
7	2	DB 6	
8	3	DB 5	
9	4	DB 4	
10	5	DB 3	
11	6	DB 2	
12	7	DB 1	
13	8	DB 0	
14	9	EOC	End of Conversion EOC goes to "L" level at the fall of STC signal, and returns to "H" level at the end of conversion.
15	10	LDEN	Low Data Enable DB_0~DB_4 are read by "H" level input.
16	11	MDEN	Medium Data Enable DB_5~DB_8 are read by "H" level input.
17	12	STC	Start Conversion Conversion starts at the fall time, if pulse input at "H" level is provided. "L" level should be kept during conversion.
18	13	CHS_2	Channel Select Inputs These pins are address inputs for selecting eight analog inputs of A_{IN0}~A_{IN7}, and are taken into the internal latch
19	14	CHS_1	
20	15	CHS_0	
21	16	V_{SS}	Digital Ground
22	17	A_{GND}	Analog Ground
23	18	$V_{REF/2}$	Reference voltage supply terminal, which supplies the voltage of $\frac{V_{REF} - A_{GND}}{2}$
24	19	V_{REF}	Reference voltage supply terminal

<table>
<tr><th colspan="2">PIN No.</th><th rowspan="2">Symbol</th><th rowspan="2">NAME & FUNCTION</th></tr>
<tr><th>DIP</th><th>QFP</th></tr>
<tr><td>25</td><td>20</td><td>A_{IN7}</td><td rowspan="8">Analog input terminal
Input voltage range : A_{GND}~V_{REF}
Arbitrary input can be selected by CHS input.
<table><tr><th>CHS_0</th><th>CHS_1</th><th>CHS_2</th><th>A_{IN}</th></tr><tr><td>L</td><td>L</td><td>L</td><td>A_{IN0}</td></tr><tr><td>H</td><td>L</td><td>L</td><td>A_{IN1}</td></tr><tr><td>L</td><td>H</td><td>L</td><td>A_{IN2}</td></tr><tr><td>H</td><td>H</td><td>L</td><td>A_{IN3}</td></tr><tr><td>L</td><td>L</td><td>H</td><td>A_{IN4}</td></tr><tr><td>H</td><td>L</td><td>H</td><td>A_{IN5}</td></tr><tr><td>L</td><td>H</td><td>H</td><td>A_{IN6}</td></tr><tr><td>H</td><td>H</td><td>H</td><td>A_{IN7}</td></tr></table></td></tr>
<tr><td>26</td><td>21</td><td>A_{IN6}</td></tr>
<tr><td>27</td><td>22</td><td>A_{IN5}</td></tr>
<tr><td>28</td><td>23</td><td>A_{IN4}</td></tr>
<tr><td>29</td><td>24</td><td>A_{IN3}</td></tr>
<tr><td>30</td><td>25</td><td>A_{IN2}</td></tr>
<tr><td>31</td><td>26</td><td>A_{IN1}</td></tr>
<tr><td>32</td><td>27</td><td>A_{IN0}</td></tr>
<tr><td>33</td><td>28</td><td>INT_I</td><td rowspan="3">Integrator Input
Integrator Junction
Integrator Output
The integrator consists of these three terminals.
 

R_I and C_I should satisfy the following formula and be set as small a value as possible
$R_I \cdot C_I > \frac{13000}{f_{OSC}}$ [S]
However, R of 1 ~ 2 MΩ should be used.</td></tr>
<tr><td>34</td><td>29</td><td>INT_J</td></tr>
<tr><td>35</td><td>30</td><td>INT_O</td></tr>
<tr><td>36</td><td>31</td><td>C_2</td><td rowspan="2">Capacitors connection terminals for offset calibration.
0.1 μF is connected between C_2 and C_1, and 0.01 μF C_1 and V_{SS}, respectively.</td></tr>
<tr><td>37</td><td>32</td><td>C_1</td></tr>
<tr><td>38</td><td>33</td><td>HDEN</td><td>High Data Enable
DB_9 ~ DB_{12} are read by "H" level input.</td></tr>
<tr><td>39</td><td>35</td><td>GCKO</td><td>Gated Clock Output
Pulses of number equivalent to conversion data are output during conversion.</td></tr>
<tr><td>40</td><td>36</td><td>X_{OUT}</td><td rowspan="2">Terminals for system clock oscillation.
Crystal oscillators are connected to both the ends of terminals.</td></tr>
<tr><td>41</td><td>37</td><td>X_{IN}</td></tr>
<tr><td>42</td><td>38</td><td>V_{DD}</td><td>Supply Voltage 5 V ± 0.5 V</td></tr>
</table>

5. FUNCTIONAL DESCRIPTION

5.1 TIMING CHART



5.2 CONVERSION CYCLE

In the state of PHASE 0', the operation of LSI is at a stop and the integrating amplifier performs as voltage follower. Under this condition the external capacitor (0.1 μF across C_1 and C_2)

When STC is given, the offset voltage charged into external capacitors is applied to non - inversion of the integrator, thus canceling the offset voltage equivalently. In PHASE I, the integrator continues to integrate A_{GND} until its output reaches V_C.

In PHASE III the integrator integrates the analog input for the same period of time as T_2 after it has integrated V_{REF} for a fixed period of time (T_2) in PHASE II.

Finally, in PHASE IV the integrator continues to integrate A_{GND} until its output reaches V_C.

Let the time in PHASE IV be T_4. Then the following equation is made (formed) by omitting error factors such as offset drift.

$$V_{AIN} = \frac{T_4}{2T_2} V_{REF} \ (A_{GND} = 0V) \cdots (1)$$

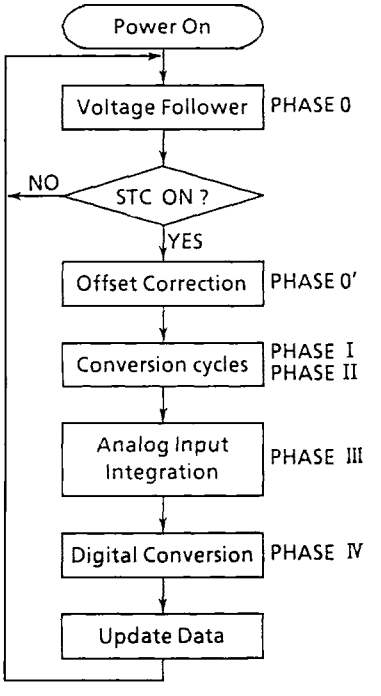
In case of this LSI, T_2 is designed by 4096 x 2·T_{OSC} (T_{OSC} denotes reference clock synchronization). Therefore, the above formula letting 2·T_{OSC} be T is changed as follows:

$$\frac{V_{AIN}}{V_{REF}} = \frac{T_4}{8192T} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (2)$$

That is, 13 - bit resolution A / D conversion of FS (full scale) = 8192 can be made by counting the period of T_4 by use of a clock having T frequency.

However, it is recommended that R_I and C_I composing the integrator be set to the values close to 13000 / f_{OSC} as possible after having satisfied the following formula.

$$R_I C_I > 13000 / f_{OSC}, \ R_I = 1 \sim 2 \ M\Omega \text{ is used.} \cdots\cdots\cdots (3)$$



5.3 OUTPUT DATA FORMAT

13 - bit output data are output to 13 independent 3 - state data buses DB_0~DB_{12}. Since 13 - bit outputs can be independently placed on 3 - state every group of High, Medium and Low of 4 bits / 4 bits / 5 bits from the higher order, it is easy to connect the microcomputer to buses of 4, 8, 12 bits.

TRUTH TABLE

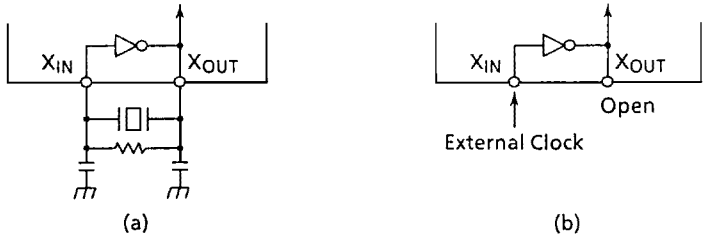
LDEN	MDEN	HDEN	Analog Input	DATA OUTPUTS (DB)												
				0	1	2	3	4	5	6	7	8	9	10	11	12
L	L	L	Don't care	Z					Z				Z			
H	L	L		D	D	D	D	D								
L	H	L		Z					D	D	D	D				
H	H	L		D	D	D	D	D	D	D	D	D				
L	L	H		Z					Z				D	D	D	D
H	L	H		D	D	D	D	D					D	D	D	D
L	H	H		Z					D	D	D	D	D	D	D	D
H	H	H	< 1 / 2 LSB	L	L	L	L	L	L	L	L	L	L	L	L	L
			1 / 2 LSB ~ 3 / 2 LSB	H	L	L	L	L	L	L	L	L	L	L	L	L
			.....	Straight Binary												
			"FS" - 5 / 2LSB ~ "FS" - 3 / 2LSB	L	H	H	H	H	H	H	H	H	H	H	H	H
			"FS" - 3 / 2LSB <	H	H	H	H	H	H	H	H	H	H	H	H	H

Note : FS ····· Full Scale, 1 LSB = (V_{REF} - A_{GND}) / 8192, Z ··· High Impedance
D ··· "H" or "L" Level

5.4 BASIC CLOCK

Since this LSI operates on the basis of the frequency given to X_{IN} input, a stable clock ($\Delta f < 0.005$ %) must be used for the clock to be given to X_{IN}.

Therefore, it is proper that the oscillation circuit is configured as shown in the following figure (a) by the use of externally mounted crystal because the LSI has a built-in inverter for crystal oscillation.



5.5 HOW TO GIVE STC INPUT, CONVERSION TIME, AND SAMPLING CYCLE

STC input is taken in with the reference clock of LSI, but the positive pulse having the pulse width for at least two cycles is required for internal starting.

The conversion time of from the fall of STC input to the rise of EOC output. Letting this time be Tc MAX (Maximum conversion time), then the following equation is obtained.

$$TcMAX = 41000 \times T_{OSC}\,[S] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

(where T_{OSC} is oscillation cycle of basic clock.)

For example, when $f_{CP} = 5$ MHz, TcMAX = 8.2 ms. For one - time sampling, an accurate output can be obtained from the falling edge of STC input after the lapse of TcMAX.

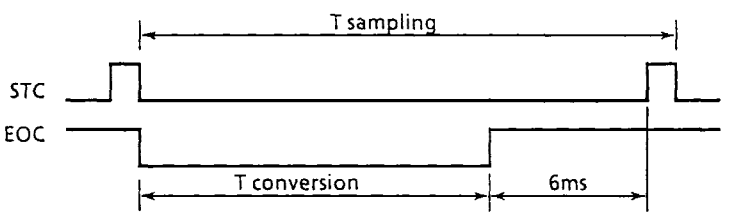
For consecutive sampling, however, STC input must be given after the lapse of a given period of time (6 ms) from the rise of EOC. This period (6 ms) is the time required for the recovery of LSI to normal state.

Therefore, the minimum sampling cycle TsMIN is as follows :

$$TsMIN = 41000 \times T_{OSC} + 0.006 + t_w\,(STC)\,[S] \quad \ldots\ldots\ldots \quad (5)$$

Note: When power is set ON, following start - up procedure is required due to indefinite state of internal circuitry.

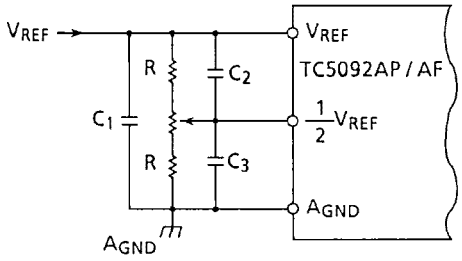
1. Applying clock, STC is to be set high over 10 ms.
2. Complete at least one cycle as a dummy conversion cycle.



5.6 REFERENCE VOLTAGE

This LSI has three reference input voltage terminals of A_{GND}, 1 / 2 V_{REF}, and V_{REF}. Since analog input signal is quantized to 1 / 8192 in the range of A_{GND}~A_{REF} for digitization, stable voltages must be supplied to 1 / 2 V_{REF} and V_{REF}.

Especially the value of 1 / 2 V_{REF} voltage has direct effects upon conversion accuracy; therefore, it is recommended that adjustment be made so as to agree output data with analog input by actually making A / D convert by use of input voltage at FS (full scale) or 1 / 2 FS level.



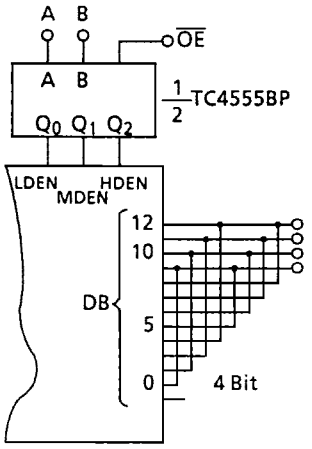
The left figure shows an example of reference voltage supplying circuit.

C_1~C_3 are filter capacitors for preventing reference voltage variations to be caused by ripple or induction noise. Generally the value of capacitor is about 0.01~0.1 μF, though it varies with the system.

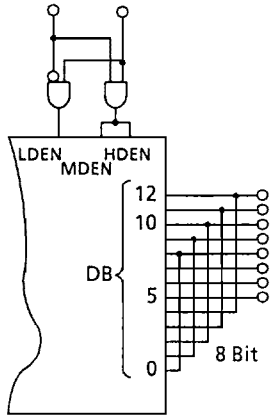
5.7 BUS INTERFACE

For connecting a microcomputer to BUS line, three independent enable terminals are used. These three enable terminals permit the processing in the unit of 4 bits (5 bits for the low order digit only). The microcomputer can be directly connected to the BUS of 4~12 bits easily by allocating proper address of microcomputer to the TC5092AP.

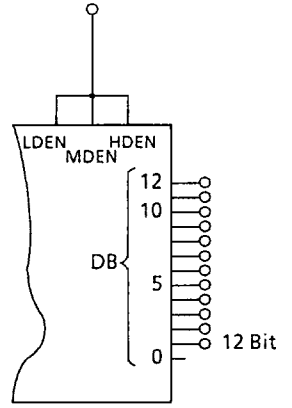
(a) 4 Bit Interface



(b) 8 Bit Interface



(c) 12 Bit Interface



6. ELECTRICAL CHARACTERISTICS

6.1 MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+7$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Reference Supply Voltage	V_{REF}	$V_{AGND} \sim V_{DD}+0.5$	V
Analog Ground Voltage	V_{AGND}	$V_{SS}-0.5 \sim V_{REF}$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP), 180 (QFP)	mW
Operating Temperature Range	T_{opr}	-40~85	°C
Storage Temperature Range	T_{stg}	-65~150	°C

6.2 RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Digital Input Voltage	V_{IN}		0	–	V_{DD}	V
Analog Input Voltage	V_{AIN}		A_{GND}	–	V_{REF}	–
Reference Supply Voltage	V_{REF}		4.0	–	V_{DD}	V
Analog Ground Voltage	V_{AGND}		0	0	0.5	V

6.3 ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10 %, V_{SS} = 0.0 V, T_a = −40~85 °C)

ITEM	SYMBOL	TEST CONDITION		V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output High Voltage	V_{OH}	I_{OH} = -1 μA, Digital output		5	4.9	5.0	–	V
Output Low Voltage	V_{OL}	I_{OL} = 1 μA, Digital output		5	–	0.0	0.1	
Input High Voltage	V_{IH}	Digital Input except X_{IN}		5	2.4	–	–	V
		X_{IN}		5	4.5	–	–	
Input Low Voltage	V_{IL}	Digital Input except X_{IN}		5	–	–	0.8	
		X_{IN}		5	–	–	0.5	
Output High Current	I_{OH}	V_{OH} = 2.4 V Digital output except X_{OUT}		4.75	− 1.0	–	–	mA
Output Low Current	I_{OL}	V_{OL} = 0.4 V Digital output except X_{OUT}		4.75	1.6	–	–	mA
Output Disable Current	I_{DH}	V_{OH} = 5.5 V, DB_0~DB_{12}		5.5	–	10^{-3}	5	μA
	I_{DL}	V_{OL} = 0.0 V, DB_0~DB_{12}		5.5	–	-10^{-3}	-5	
Input Current	I_{IH}	V_{IN} = 5.5 V, Digital input		5.5	–	10^{-5}	1.0	
	I_{IL}	V_{IL} = 0.0 V, Digital input		5.5	–	-10^{-5}	-1.0	
Analog Switch Off - Leak	I_{OFF}	Analog input / output		5.5	–	± 10^{-4}	–	μA
Analog Switch On Resistor	R_{ON}	R_L = 10 kΩ		5	–		–	Ω
Operating Consumption Current	I_{DD}	V_{REF} = V_{DD} Digital output open Digital input GND	f_{cp} = 5 MHz	5	–	2	–	mA
			f_{cp} = 1 MHz	5	–	1	–	

6.4 SWITCHING CHARACTERISTICS (V_{DD} = 5.0 V ± 10 %, V_{SS} = 0.0 V, T_a = 25 °C, C_L = 50 pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}	Digital output	–	50	150	nS
Output Fall Time	t_{THL}	Digital output	–	40	150	
Output Enable Time	t_{ZL} t_{ZH}	LDEN MDEN HDEN } -DB Output	–	80	250	nS
Output Disable Time	t_{LZ} t_{HZ}		–	280	500	
Max. Clock Frequency	$f_{MAX\varnothing}$	X_{IN} Duty 40~60 %	5.0	–	–	MHz
Min. Clock Frequency	$f_{MIN\varnothing}$	X_{IN} Duty 40~60 %	–	–	–	MHz
Input Capacity	C_{IN}	Digital input	–	5	–	pF
	C_{IN}	Analog input	–	–	–	
3 - State Output Capacity	C_{OUT}	DB Output	–	8	–	

6.5 SYSTEM CHARACTERISTICS (V_{DD} = 5.0 V ± 10 %, V_{SS} = 0.0 V, T_a = 25 °C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution	n		–	13	–	Bit
Conversion Time	Tc	f_{cp} = 5 MHz	–	–	8.2	mS
		f_{cp} = 1 MHz	–	–	41	
Sampling Cycle	T_{SPL}	f_{cp} = 5 MHz	14.2	–	–	mS
		f_{cp} = 1 MHz	47	–	–	
Nonlinearity		$V_{DD} = V_{REF}$	–	± 1		LSB
Zero Scale Error	E_{ZP}		–	± 2		
Full Scale Error	E_{FS}		–	± 1		
STC Min. Pulse Width	t_w		–	–	2 / f_{OSC}	S