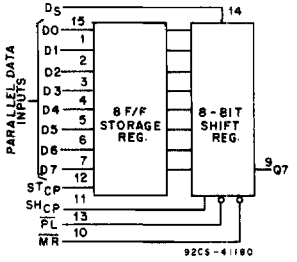
CD54/74HC597
CD54/74HCT597

File Number **1915**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Bit Shift Register with Input Storage

Type Features:

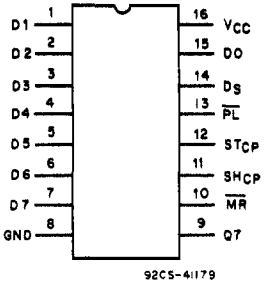
- *Buffered Inputs*
- *Asynchronous Parallel Load*
- *Typical f_{MAX} = 60 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC597 and CD54/74HCT597 are high-speed si-gate CMOS devices that are pin-compatible with the LSTTL 597 devices. Each device consists of an 8-flip-flop input register and an 8-bit parallel-in/serial-in, serial-out shift register. Each register is controlled by its own clock. A "low" on the parallel load input (PL) shifts parallel stored data asynchronously into the shift register. A "low" master input (MR) clears the shift register. Serial input data can also be synchronously shifted through the shift register when PL is high.

The CD54HC/HCT597 devices are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT597 devices are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +125°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}
- *Alternate Source is Philips/Signetics*



TERMINAL ASSIGNMENT

CD54/74HC597
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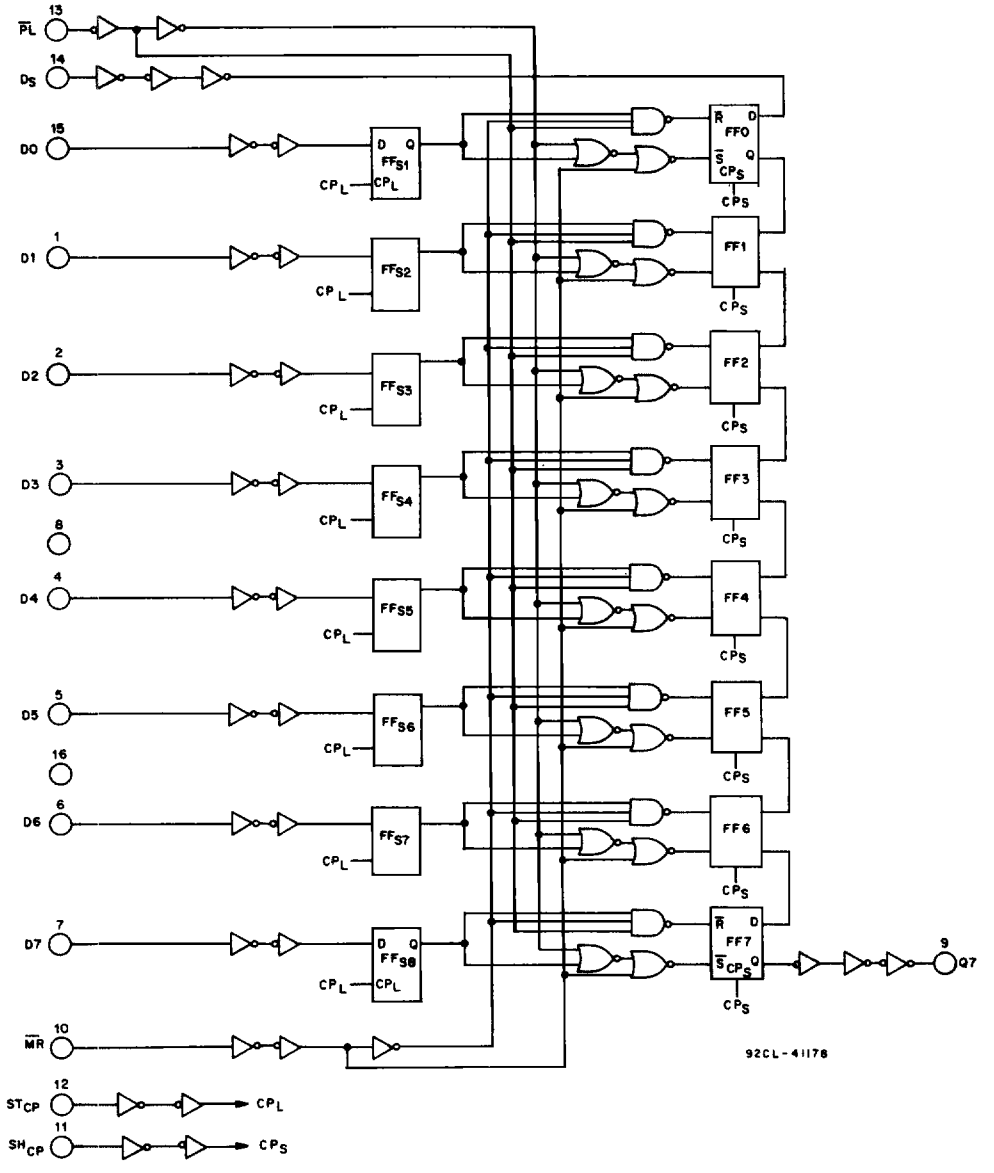

Fig. 1 — Logic diagram for the CD54/74HC597 and CD54/74HCT597.

CD54/74HC597
CD54/74HCT597

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			74HC/54HC			74HC		54HC −55/ +125°C		TEST CONDITIONS		74HCT/54HCT			74HCT		54HCT −55/ +125°C		UNITS
				+25°C			−40/ +85°C		74HC −40/ +125°C				+25°C			−40/ +85°C		74HCT −40/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	−0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IH} or V_{IH}	−4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IH} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		−5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IL}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IL}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}−2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D_s	0.2
D_n	0.3
$\overline{PL}$, $\overline{MR}$	1.5
ST_{CP}, SH_{CP}	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V or $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = −55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = −40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... −55 to +125°C
PACKAGE TYPE E, M ..... −40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	−40	+125	°C
CD54 Types	−55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay:					
SH_{CP} to Q7	15	t_{PHL}	14	16	ns
$\overline{PL}$ to Q7	15	t_{PLH}	17	20	
$\overline{MR}$ to Q7	15		14	18	
ST_{CP} to Q7	15		20	23	
Power Dissipation Capacitance*	—	C_{PD}	13.5	18.5	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f + \Sigma (C_L V_{CC}^2 f_o)$ where:

f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

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PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Min.	Max.	
SH_{CP} Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
SH_{CP} Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
ST_{CP} Pulse Width	t_W	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	13	—	15	—	16	—	18	—	20	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
$\overline{MR}$ Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	18	—	20	—	23	—	24	—	27	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{PL}$ Pulse Width	t_W	2	70	—	—	—	90	—	—	—	105	—	—	—	ns
		4.5	14	—	16	—	18	—	20	—	21	—	24	—	
		6	12	—	—	—	15	—	—	—	18	—	—	—	
ST_{CP} to SH_{CP} Setup Time	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	24	—	25	—	30	—	30	—	36	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
D_S to SH_{CP} Setup Time	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
D_n to ST_{CP} Setup Time	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
ST_{CP} to SH_{CP} Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
D_S to SH_{CP} Hold Time	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
		4.5	3	—	3	—	3	—	3	—	3	—	3	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
D_n to ST_{CP} Hold Time	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
		4.5	3	—	3	—	3	—	3	—	3	—	3	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
MR to SH_{CP} Removal Time	t_{REM}	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
		4.5	3	—	10	—	3	—	13	—	3	—	15	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
SH_{CP} to Q7	t_{PHL}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	
$\overline{PL}$ to Q7	t_{PHL}	4.5	—	40	—	48	—	50	—	60	—	60	—	72	ns
		6	—	34	—	—	—	43	—	—	—	51	—	—	
	t_{PLH}	2	—	240	—	—	—	300	—	—	—	360	—	—	
ST_{CP} to Q7	t_{PHL}	4.5	—	48	—	56	—	60	—	70	—	72	—	84	ns
		6	—	41	—	—	—	51	—	—	—	61	—	—	
		2	—	175	—	—	—	220	—	—	—	265	—	—	
$\overline{MR}$ to Q7	t_{PHL}	4.5	—	35	—	44	—	44	—	55	—	53	—	66	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Output Transition	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Time		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

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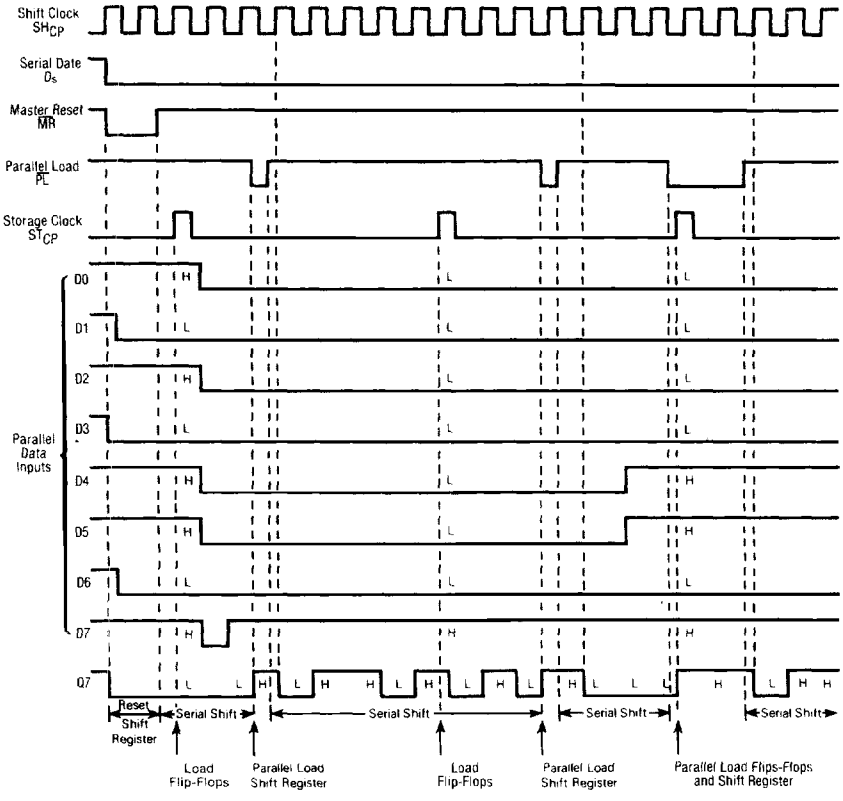

TIMING DIAGRAM

FUNCTION TABLE

ST_{CP}	SH_{CP}	PL	MR	FUNCTION
_/‾	X	X	X	data loaded to input Flip-Flops
_/‾	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input Flip-Flops to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	_/‾	H	H	shift register clocked Qn = Qn-1, Q0 = D_s

H = HIGH voltage level
L = LOW voltage level
X = don't care
_/‾ = LOW-to-HIGH CP transition

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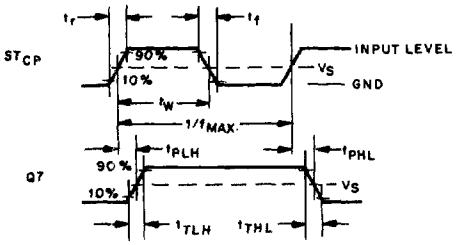
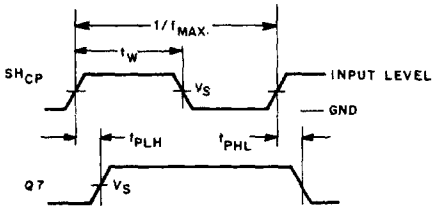
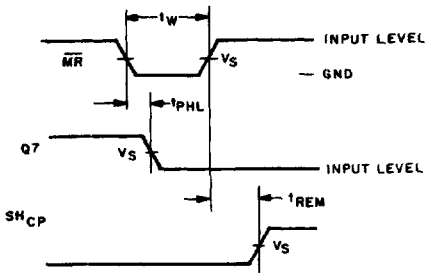
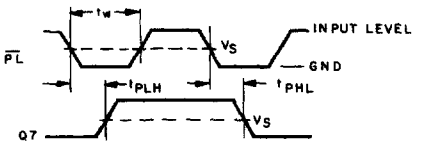
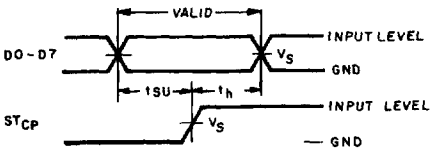
SWITCHING WAVEFORMS

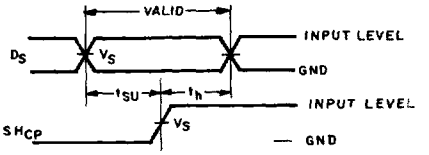


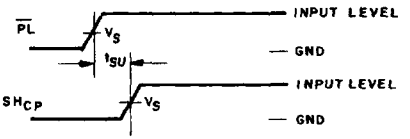












	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V