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AK2500

Preliminary

DS3/STS-1 Analog Line Receiver

Features

- AK2500 Provides Complete Analog Line Receiver for DS3 and STS-1 Applications
- Provides Line Equalization, and Clock and Data Recovery Functions
- The Signal Conditioning Circuit can be bypassed for OC-1 optical applications
- Includes local loopback multiplexor

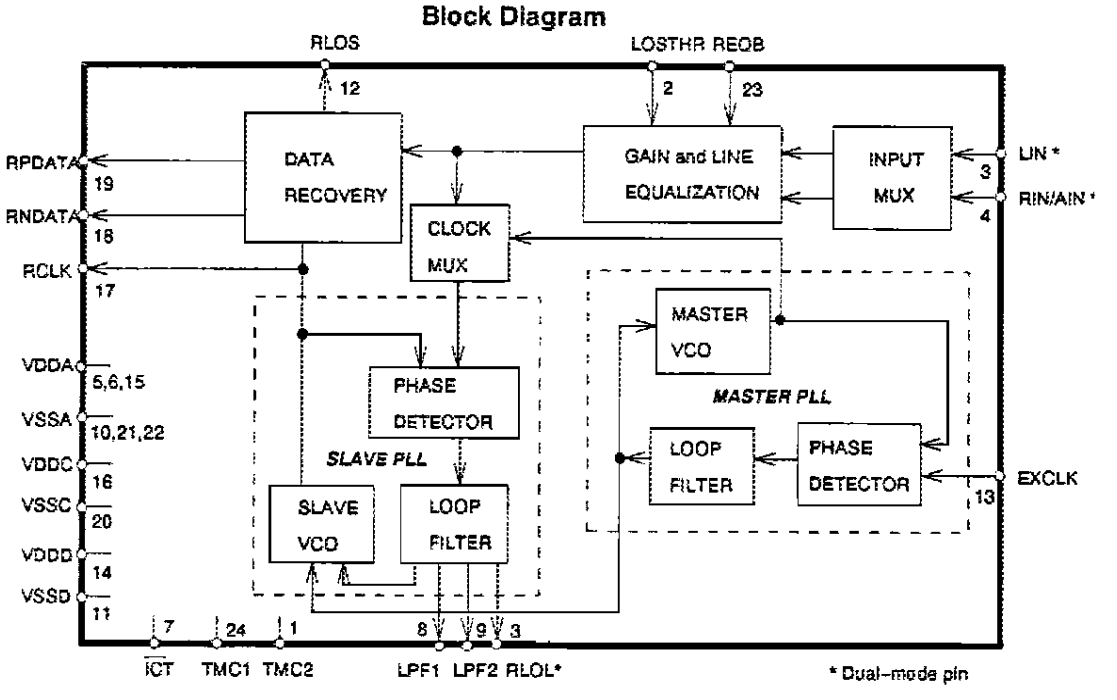
General Description

The AK2500 provides the analog receive line interface functions for a 44.736 MHz DS3 or 51.84 MHz STS-1 interface, and an OC-1 optical interface. The device operates from a single +3.3 Volt supply and is transparent to the framing format.

Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-3 cross connect.
- Interfacing customer premises equipment to a line.

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	V+	-0.3	6.0	V
Input Voltage, Any Pin (Note 2)	V_{in}	GND-0.3	(V+)+0.3	V
Input Voltage, EXCLK Pin	V_{exin}	GND-0.3	5.5	V
Input Current, Any Pin (Note 3)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-40	85	℃
Storage Temperature	t_{stg}	-65	150	℃
Power Dissipation	P_D	-	1	W

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note; 1. GND=VSSA=VSSC=VSSD=0V

2. Except EXCLK pin.

3. Transient currents of up to 100 mA will not cause SCR latch up.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply (referenced to GND)		V+	3.0	3.3	3.6	V
Ambient Operating Temperature		T_A	-40	25	85	℃
Supply Current:	DS3	I_S	-	80	105	mA
	STS-1		-	85	110	mA
	Optical Operation		-	25	32	mA
EXCLK Frequency	DS3		44.736 - 100ppm	44.736	44.736 + 100ppm	MHz
	STS-1		51.84 - 100ppm	51.84	51.84 + 100ppm	MHz

ANALOG SPECIFICATIONS (T_A = T_{min} to T_{max}; V+ = 3.3V±0.3V; GND = 0V)

Parameter		Min	Typ	Max	Units
Slave PLL Jitter Transfer	3dB Bandwidth	-	205	-	kHz
with repetitive 1000 pattern	Peaking (Note 4)	-	0.05	0.1	dB
Jitter Tolerance	(Note 4, 5)				
	3.2kHz	14	-	-	UIpp
	150kHz - 300kHz	0.3	-	-	UIpp
	900kHz - 4.5MHz	0.05	-	-	UIpp
Signal Noise Immunity	(Note 6)	-	11	-	dB
Output Jitter with Jitter-Free Input:	All one's pattern	-	1.4	-	ns_{p-p}
(Note 4)	Repetitive 1000 pattern	-	1.8	-	ns_{p-p}
Output Clock Duty Cycle	(Note 4)	45	-	55	%
Slave PLL Lock Acquisition Time	(Note 4, 7)	-	1.0	-	ms
Receiver Input Range		70	-	850	mV
AIN Signal Amplitude	(Note 8)	0.6	-	2.0	V_{p-p}
Jitter Tolerance with NRZ input	(Note 9)				
	30 Hz	15			UIpp
	300 - 2.0kHz	1.5			UIpp
	20kHz	0.15			UIpp

Note; 4. Measured with repetitive input at nominal DSX-3 level with (V+)=3.3V, T_A=25℃

5. Typical performance is shown in Figure 1.

6. Measured with sinusoidal noise, peak amplitude of noise is 11dB down from peak amplitude of signal. The noise frequency is 22MHz±22kHz.

7. With device powered up. Measurement starts at the time when signal is reapplied to RIN/AIN.

8. An ECL signal can be directly AC-coupled into AIN. CMOS and TTL signals should be attenuated before being AC-coupled.

9. Conditioning circuit bypass mode (TMC1=1 and TMC2=0)

AK2500 DS3 SWITCHING SPECIFICATIONS

(T_A = T_{min} to T_{max}; V+ = 3.3V±0.3V; GND = 0V; Input: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
RCLK Pulse Width		t_{pwh}	10.1	11.177	12.2	ns
	(Note 10, 11)	t_{pwl}	10.1	11.177	12.2	ns
EXCLK Duty Cycle		t_{pwhl}	40	-	60	%
Rise Time, RCLK	(Note 11)	t_r	-	-	3.5	ns
Fall Time, RCLK	(Note 11)	t_f	-	-	3.5	ns
Receive Propagation Delay	(Note 12)	t_{PD}	0.6	-	3.5	ns

AK2500 STS-1 SWITCHING SPECIFICATIONS

(T_A = T_{min} to T_{max}; V+ = 3.3V±0.3V; GND = 0V; Input: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
RCLK Pulse Width		t_{pwh}	8.7	9.645	10.6	ns
	(Note 12, 13)	t_{pwl}	8.7	9.645	10.6	ns
EXCLK Duty Cycle		t_{pwhl}/t_{pw}	40	-	60	%
Rise Time, RCLK	(Note 13)	t_r	-	-	3.5	ns
Fall Time, RCLK	(Note 13)	t_f	-	-	3.5	ns
Receive Propagation Delay	(Note 12)	t_{PD}	0.6	-	3.5	ns

Note; 10. Assumes Slave PLL is locked to 44.736 MHz signal.

11. The sum of the pulse widths must always meet the frequency specifications.

12. At max load of 10 pF. Guaranteed by design and characterization.

13. Assumes Slave PLL is locked to 51.84 MHz signal.

DIGITAL CHARACTERISTICS (T_A = T_{min} to T_{max}; V+ = 3.3V±0.3V; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 14)	V_{IH}	(V+) x 0.7	-	(V+)	V
EXCLK High-Level Input Voltage	V_{EXIH}	(V+) x 0.7	-	5.5	V
Low-Level Input Voltage (Note 14)	V_{IL}	GNDD	-	0.5	V
EXCLK Low-Level Input Voltage	V_{EXIL}	GNDD	-	0.5	V
High-Level Output Voltage (Note 15,16) I_{OUT}=-40 μ A	V_{OH}	(V+) x 0.8	-	(V+)	V
Low-Level Output Voltage I_{OUT}=1.6mA (Note 15) I_{OUT}=0.4mA (Note 16)	V_{OL}	GND	-	0.4	V
Input Leakage Current (Note 17)				±10	μ A

Note; 14. Pins TMC1, TMC2, $\overline{ICT}$

15. Pins RCLK, RPDATA, RNDATA

16. Pins RLOS, RLOL

17. Except $\overline{ICT}$

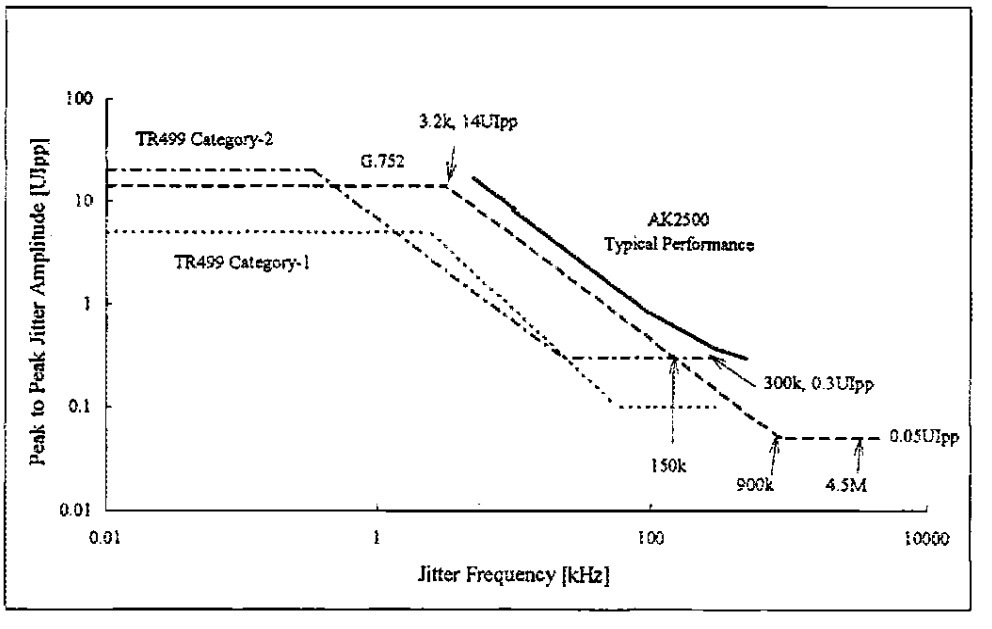


Figure 1 Typical AK2500 Input Jitter Tolerance (DS3)

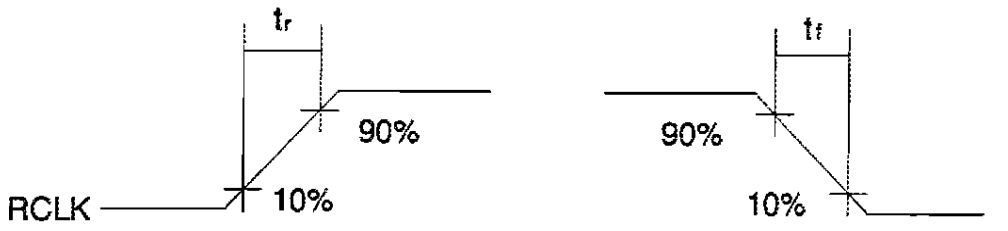


Figure 2. Signal Rise and Fall Characteristics

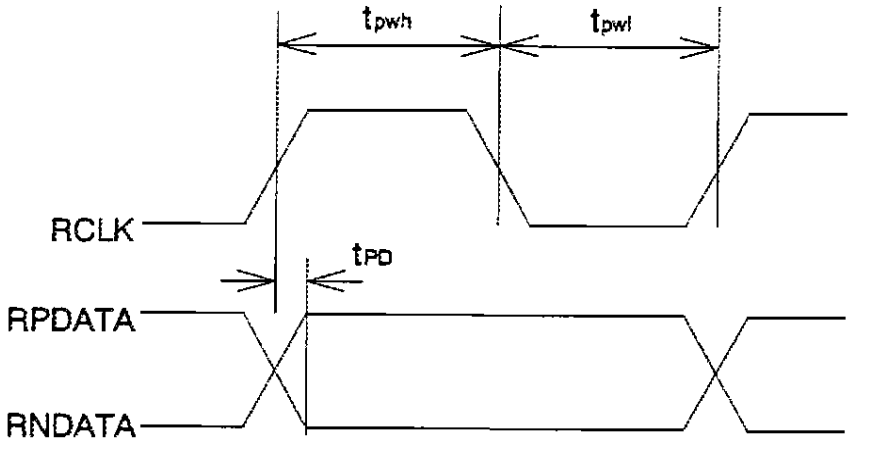


Figure 3. Recovered Clock and Data Switching Characteristics

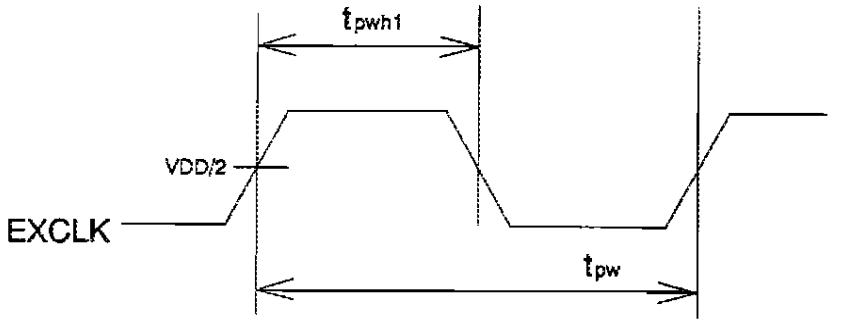


Figure 4. EXCLK Duty Cycle Requirements

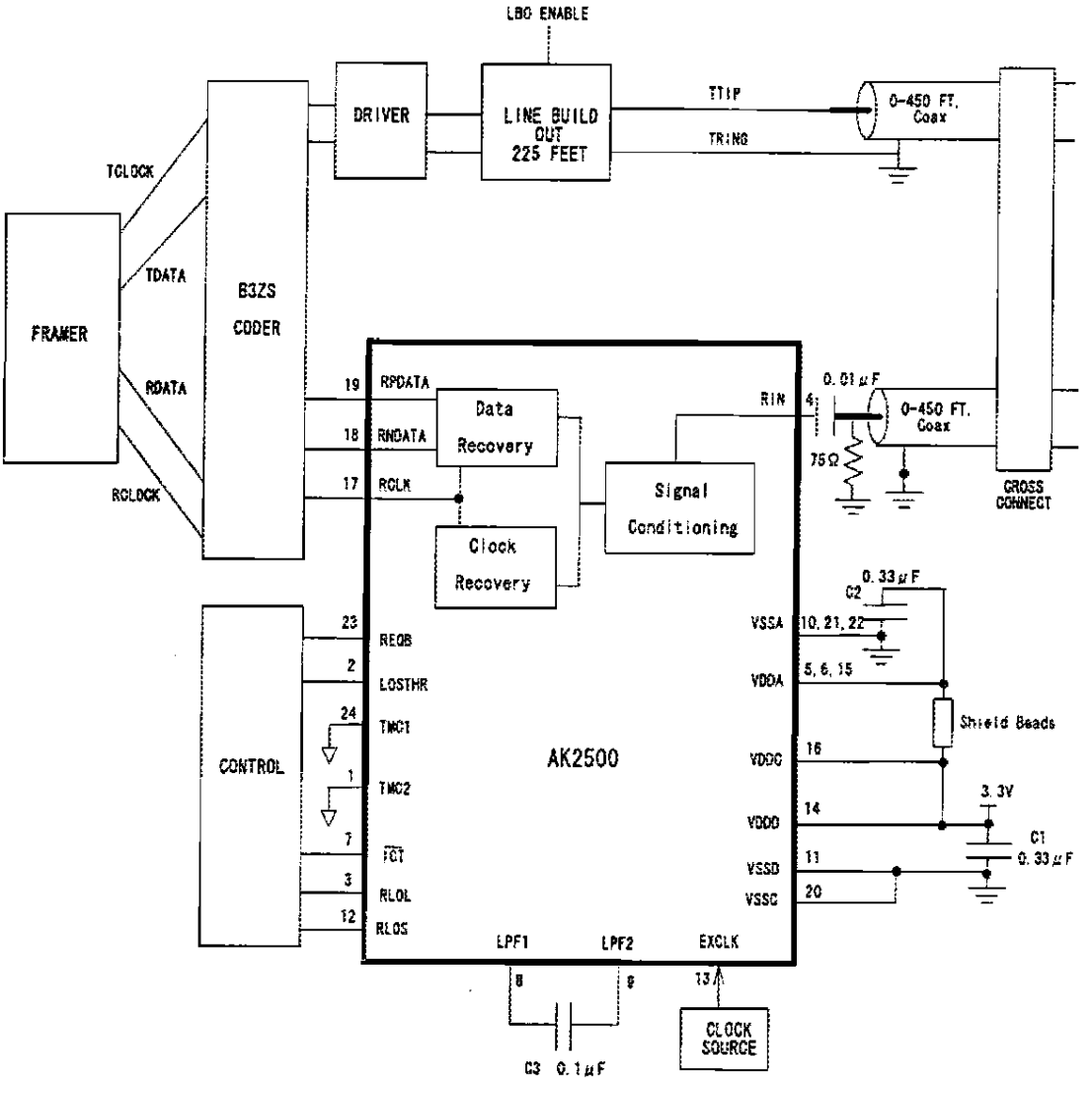


Figure 5. Basic Application Circuit - Normal Coax Operation

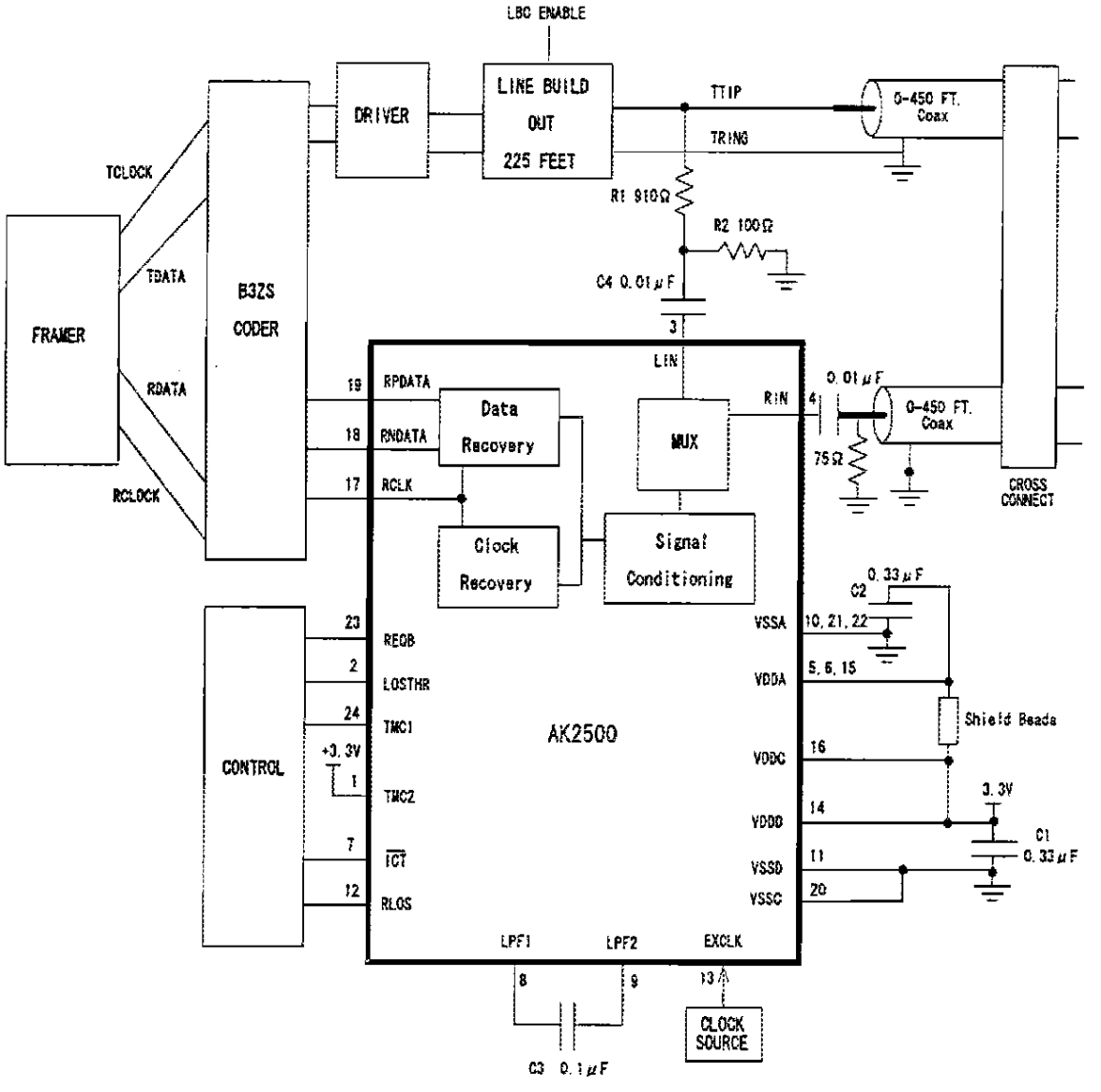


Figure 6. Basic Application Circuit - Loopback Coax Application

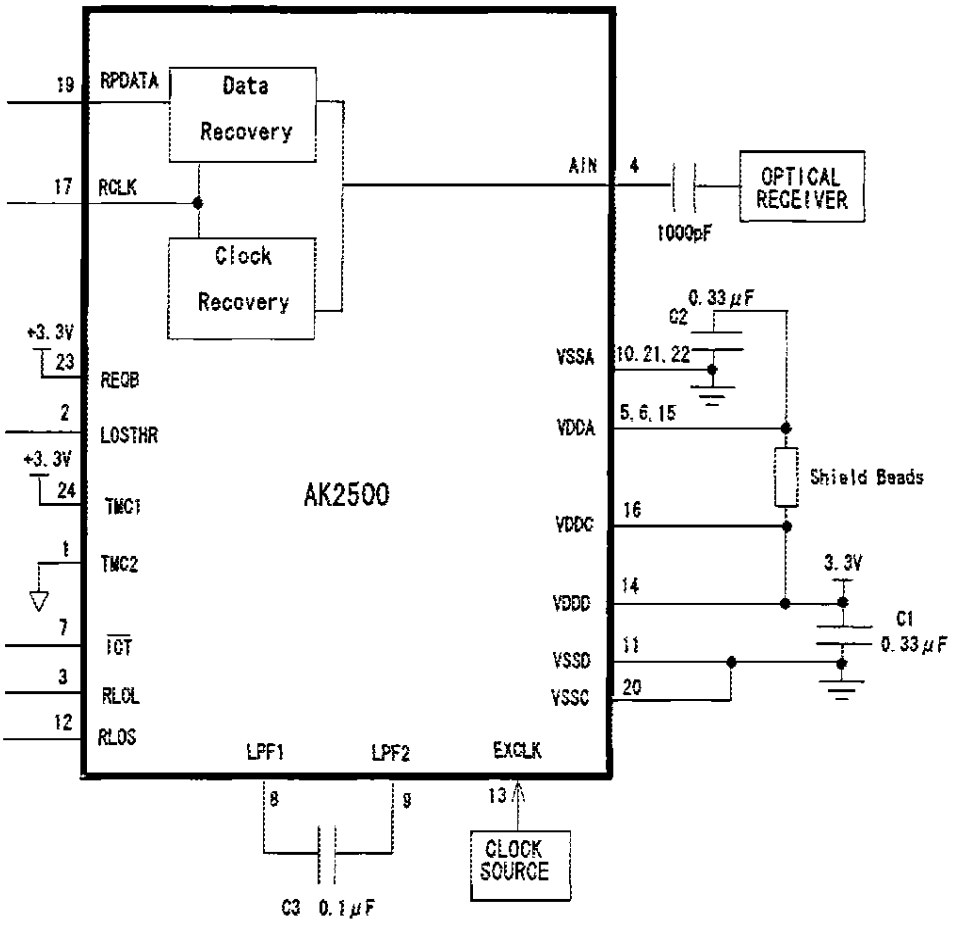


Figure 7. Basic Application Circuit - Optical Operation

THEORY OF OPERATION

The AK2500 provides the basic receiver functions of a high-speed line card as shown in Figures 5, 6 and 7. The receiver extracts data and clock from a B3ZS coded signal and outputs clock and synchronized data. Noise-coupling must be minimized along the path from cable to RIN. Any noise coupled into RIN directly degrades the signal-to-noise ratio of the input signal.

Operating Modes

The AK2500 has three major operating modes as defined by TMC1 and TMC2, as shown in Table 1.

Signal Conditioning

In the receive signal path, the internal equalizer can be included by setting REQB = 0 or bypassed by setting REQB=1. The equalizer bypass option allows easy interfacing of the AK2500 device into systems already containing external equalizers. The equalization is variable and is based upon the level of the incoming signal.

In the AK2500, the equalizer works as follows. When the peak of the amplified signal equals approximately 300mV, the equalizer compensates as appropriate for a nominal DSX-3/STS-1 pulse as attenuated by 450 feet of 728A cable. When the peak of the amplified signal equals approximately 600mV, the equalizer compensates as appropriate for a nominal DSX-3/STS-1 pulse. The equalizer adjusts continually as the signal strength varies between 70 mV and 850 mV.

The pulse stretcher increases the jitter tolerance of the receiver by stretching the incoming pulse.

Clock Recovery

The receiver uses a Master/Slave Phase Lock Loop (PLL) to recover clock. The Master PLL has its center frequency set using the reference clock, EXCLK. The same control voltage that is generated to center the frequency of the Master VCO is also used to center the frequency of the Slave VCO. This insures continuous frequency lock of the Slave PLL, and also insures immunity to false lock. The Slave VCO is phase locked to the received data stream.

If a valid input signal is assumed to be already present at the analog input, the maximum time between the application of device power and error-free operation is typically 20 ms. If power has already been applied and input data is then lost, the interval between the restoration of valid data and error-free operation is nominally 1.0 ms and typically no longer than 4 ms.

An external loop filter is used by the slave PLL, allowing the jitter tolerance and transfer function to be tailored for a variety of applications. The component values for the capacitor is 0.1 μF±20%. A low-leakage (e.g., ceramic) capacitor should be used.

TMC1	TMC2	Mode	Pin 4 Definition	Pin 3 Definition
0	0	Normal Coax Operation Coax-compatible analog signal input on RIN (pin 4)	RIN Input	RLOL Output
0 1	1 1	*Loopback Coax Operation TMC1 used to select between two coax- compatible analog signal; TMC1=low selects pin 4 for normal operation: TMC1=high selects pin 3 for loopback.	RIN Input	LIN Input
1	0	Optical Operation Output of optical receiver input on AIN (pin 4)	AIN Input	RLOL Output

Table 1. Mode Control

**Note*

Loopback Mode is not available in the current revision. TMC2 bit must be set 0.

Loss-of-Lock Detection

The PLL monitors the retimed data to detect possible phase-lock which is 180° out of a normal phase alignment. Loss of lock is detected if either or both of the following conditions exist:

- the frequency difference between the Slave PLL clock and the incoming signal (on RIN/AIN) exceeds than approximately ± 0.5%.
- In the normal coax operation, seven consecutive 0's are detected in the retimed data (indicates possible lock which is 180° out of normal alignment). In the optical operation, any consecutive 0's are not detected.

External Reference Clock

An external reference clock is used to set the frequency of the Master PLL. The reference clock should be within ±100ppm of the line signal.

Data Recovery

Comparators are used to detect pulses on the analog input. The comparator data decision threshold is dynamically established by peak detectors.

Loss of Signal

Receiver loss of signal is indicated upon receiving consecutive zeros or if the input signal falls below the alarm threshold level. A digital counter counts received zeros based on RCLK cycles. The alarm threshold is 175± 75 zeros. The receiver reports loss of signal by setting the Loss of Signal pin, RLOS, high.

When receiving signals from a coax cable, or during loopback, RLOS operates as follows. As shown in Figure 9, if the incoming signal level falls below a certain threshold (see Table 2), the output clock of the master VCO is muxed directly into the slave VCO, replacing the received data as the signal source for the slave VCO. This replacement of the signal source improves the frequency accuracy of the slave VCO, since the slave VCO is normally trained to only within ±5% of the frequency of the master VCO. When the receiver reports loss of signal, the recovery data (RPDATA and RNDATA) is fixed zeros. The signal source for the slave VCO reverts back to the received data signal when the incoming signal level rises to a certain threshold (Table 2), RLOS returns to logic zero upon detection of 33% ones density (based on 58 ones out of 175 bit periods). RLOS does not return to logic zero if any subintervals of 100 pulse positions containing no pulses of either polarity were observed.

When receiving signals on AIN from a optical receiver, RLOS operates as follows. As shown in Figure 10, if 175±75 zeros are detected, the output clock of the master VCO is muxed directly into the slave VCO, replacing the received data as the signal source for the slave VCO. This replacement of the signal source improves the frequency accuracy of the slave VCO, since the slave VCO is normally trained to only within ± 5% of the frequency of the master VCO. The signal source for the slave VCO reverts back to the received data signal and RLOS returns to a logic zero upon detection of 33% ones density (based on 58 ones out of 175 bit periods),if any subintervals of 100 pulse positions containing no pulses of either polarity were not observed.

Under all normal and RLOS conditions, the slave VCO frequency is output on RCLK, and the recovered data is output on RPDATA/RNDATA. A Power-On reset sets RLOS high.

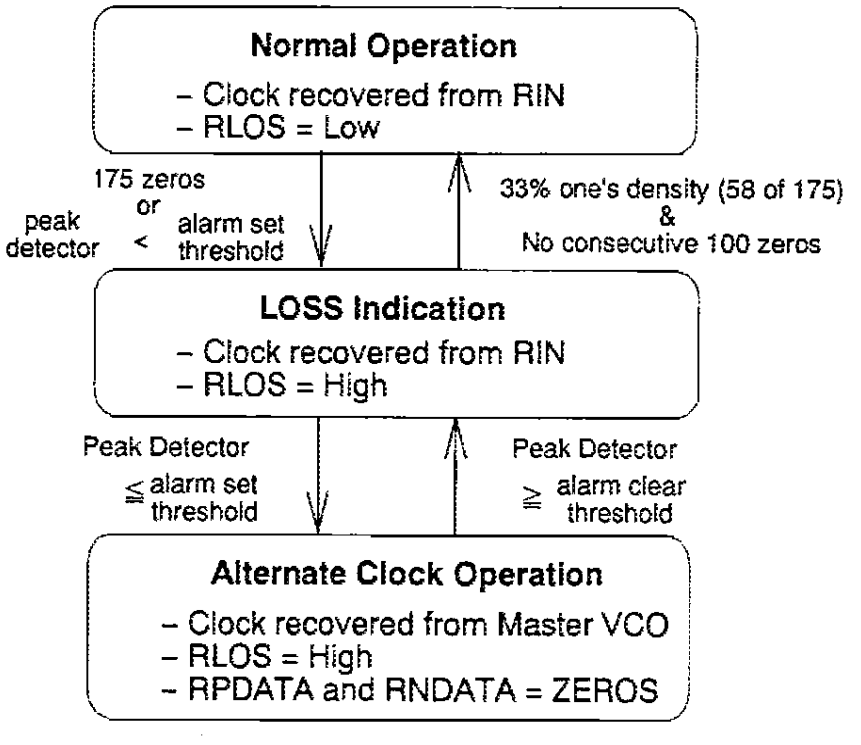


Figure 9. Loss of Signal state diagram with an electrical input selected

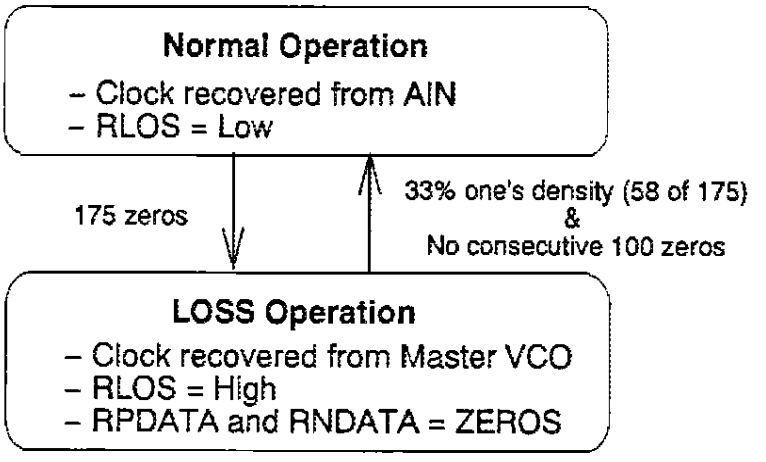


Figure 10. Loss of Signal state diagram with an optical input selected

LOSTHR Voltage	Clears Alarms		Sets Alarms		Units
	Min. Upper Threshold	Max. Upper Threshold	Min. Lower Threshold	Max. Lower Threshold	
GND	71	125	59	105	mV
VDD/2	56	99	47	83	mV
VDD	45	79	37	66	mV

Table 2. Analog Loss-of-Signal thresholds

Alternate Input

For optical applications, the signal conditioning circuit can be bypassed by setting TMC1 high and TMC2 low. When bypassed, an NRZ data signal can be input on AIN. An ECL signal (e.g., the output of an optical receiver module) can be directly AC coupled into AIN. CMOS and TTL signals should be attenuated to a typically 0.8Vp-p signal level before being AC-coupled into AIN.

Power On Reset

Upon power-up, the IC performs a reset. The PLLs are continuously calibrated through the Master/Slave architecture foregoing any requirement to recalibrate the receiver when in operation.

Local Loopback

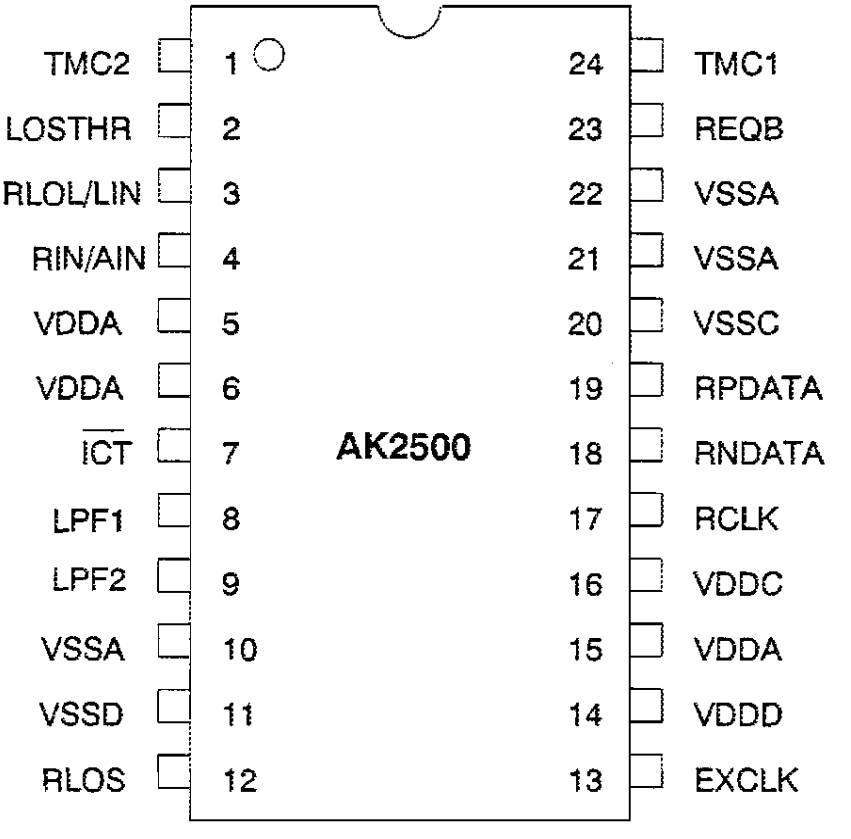
An additional receiver input is provided to support a local loopback. When TMC2 is high, pin TMC1 is used to select between pin 3 and pin 4 for the input signal. Setting TMC1 low selects pin 4 for normal operation. Setting TMC1 high selects pin 3 for loopback operation. Figure 6 shows a recommended circuit for connecting transmitter outputs into pin 3. The series resistor R1 and R2 decrease the signal by 20 dB, minimizing crosstalk effects during normal reception.

Power Supply

The device operates from a single 3.3 Volt supply. The VDDC and VSSC inputs power the output drivers. The VDDD and VSSD inputs power the digital circuitry on the device. The VDDA and VSSA inputs power the sensitive analog circuitry. The recommended power supply decoupling circuit is illustrated in Figure 7. Good quality high-frequency, low lead-inductance capacitors should be used. All capacitors should be as close to the device as possible, and the connection between the shield beads and C2 should be as short as possible.

PIN DESCRIPTIONS

24 PIN SOP Package



Power Supplies

VDDA, VDDC, VDDD - Positive Power Supply, Pins 5, 6 and 15, 16, and 14

Positive power supplies for the device; typically +3.3 volts.

VSSA, VSSC, VSSD - Ground, Pins 10, 21 and 22, 20, and 11

Power supply grounds for the device; typically 0 volts.

Clock

EXCLK - External Reference Clock, Pin 13

A valid DS3 or STS-1 clock must be provided at this input. The duty cycle of EXCLK, referenced to VDD/2 levels, must be 40% - 60%. The EXCLK frequency determines the operating frequency of the device.

Control

TMC1, TMC2 - Mode Control 1 and 2, Pins 24 and 1

Modes are enabled within the device by using TMC1 and TMC2. (See Table 1)

$\overline{\text{ICT}}$ - Output in Circuit Test Control (Active-Low), Pin 7

If $\overline{\text{ICT}}$ is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-impedance state to allow for in-circuit testing.

$\overline{\text{ICT}}$ has an internal pull-up (nominally 50k Ω).

REQB - Receive Equalization Bypass, Pin 23

A High on this pin bypasses the internal equalizer. A low places the equalizer in the data path.

LOSTHR - Loss of Signal Threshold Control, Pin 2.

The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, VDD/2, or VDD at LOSTHR (see Table 2).

Inputs

RIN - Receive Input, Pin 4.

Unbalanced analog receive input. The B3ZS receive signal is input to this pins. Data and clock are recovered and output on RPDATA, RNDATA and RCLK.

LIN - Loopback Input, Pin 3.

A B3ZS signal can be input to this pins. This signal is input to the receiver under control of TMC1 and TMC2 (See Table 1).

AIN - Alternate Data Input, Pin 4.

Allows NRZ format input data to be input into the clock and data recovery circuit, bypassing the RIN receiver signal conditioning circuit. The AIN input is activated by setting TMC1 high and TMC2 low.

LPF1, LPF2 - PLL Filter 1 and 2, Pins 8 and 9.

An external capacitor (0.1 μF±20%) is connected between these pins.

Status

RLOS - Receive Loss-of-Signal, Pin 12.

This pin is set high on loss of the data signal at the receive input.

RLOL - Receive PLL Loss-of-Lock, Pin 3.

This pin is set high on loss of slave PLL lock, when not in local loopback mode. (set high when frequency difference between Slave PLL and received signal exceeds approximately ± 0.5%)

Outputs

RCLK, RPDATA, RNDATA - Recovered Clock, Receive Positive Data and Receive Negative Data, Pins 17, 19 and 18.

Data and clock are recovered from RIN inputs and are output at these pins. A signal on RPDATA corresponds to a positive pulse received on RIN, while a signal on RNDATA corresponds to the receipt of a negative pulse. RPDATA and RNDATA are NRZ. RPDATA and RNDATA are stable and valid on the falling edge of RCLK. When an alternative data stream is input on AIN (selected by pins TMC1 and TMC2), the output data is on RPDATA, and RNDATA is low.

Marking

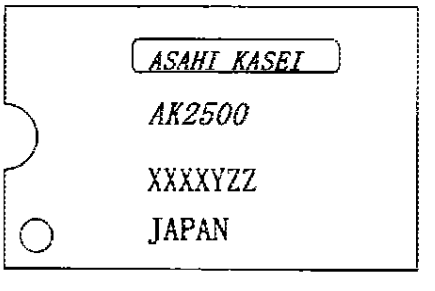
(1)Pin #1 indication

(2)Date Code: 7digits XXXXYZZ

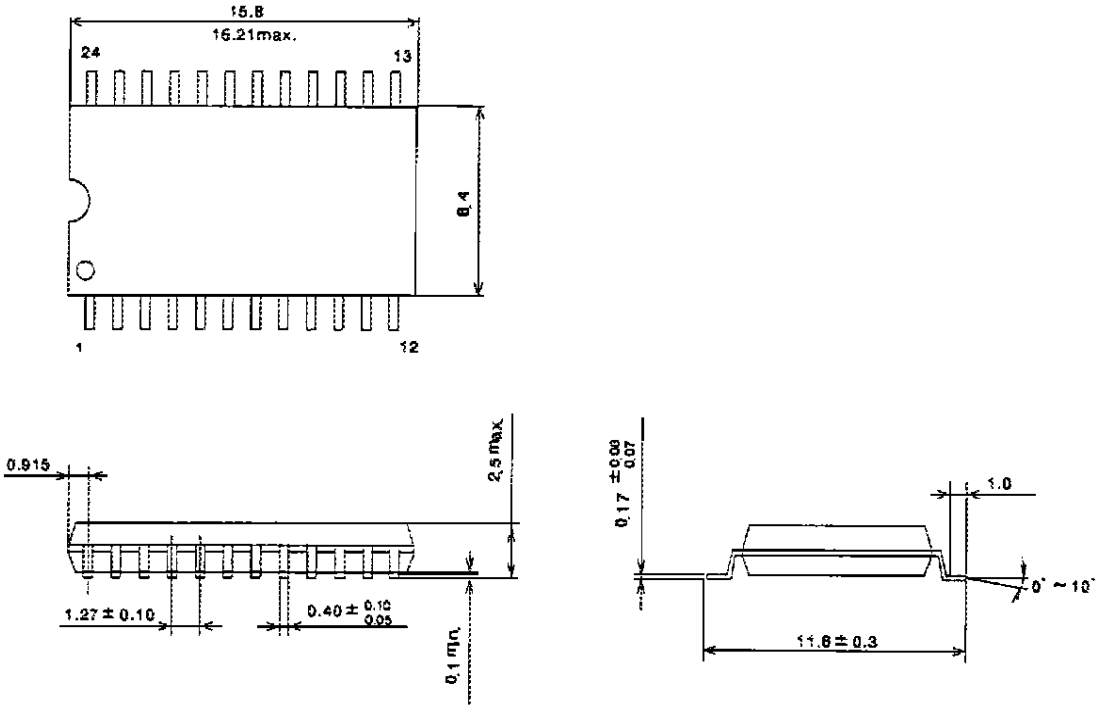
(3)Marketing Code: AK2500

(4)Country of Origin: JAPAN

(5)Asahi Kasei Logo



Outline Dimensions



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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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