1.0 Product Description

1.1 Overview

The Bt8215 is a bidirectional buffer with a 36-bit bidirectional port and 9-bit unidirectional ports that can be configured to transfer fixed-length cells. Each direction can store up to 512 36-bit words. This part, therefore, replaces eight unidirectional FIFOs and associated control circuitry for communication between asynchronous byte-wide ports, a 32-bit-wide processor, or other synchronous systems. This product is designed as a single CMOS integrated circuit, packaged in a 100-pin Plastic Quad Flat Pack (PQFP).

The bidirectional port reads data from the input buffer and writes data to the output buffer. Each port can be programmed to be synchronous or asynchronous. The bidirectional port can also be configured to connect directly to a microprocessor. Buffer status indications include empty, full, almost-full, almost-empty and half-full flags. A padding function that controls unidirectional reading and writing of data blocks that do not end on a word boundary is available.

The product can autonomously control catalog synchronous or asynchronous buffers (FIFOs) to increase buffer depth at a reduced cost. No additional circuitry other than the generic FIFO is required to implement a deeper buffer. The generic FIFOs can be cascaded among themselves for even greater depth. The Bt8215 also has the ability to autonomously transfer data to the unidirectional port of another Bt8215 buffer. The unidirectional port can be configured to interface with Brooktree's Bt8222 ATM/PLCP and Bt8330 HDLC formatter chips and also with an AMD TAXI® chip.

There are two principal modes of operation for this product: stand-alone smart FIFO mode and microprocessor mode. In stand-alone smart FIFO mode, the bidirectional port has a common buffer interface. In microprocessor mode, features are controlled through a microprocessor control register, including fixed-size cell formatting and delineation as well as additional parity operations. Also, microprocessor mode supports a cell mode that allows cell headers to be read and written and the cell data to be burst read or burst written. This reduces the processing power needed in the processor to transfer cells.

1.2 Brief Block Description

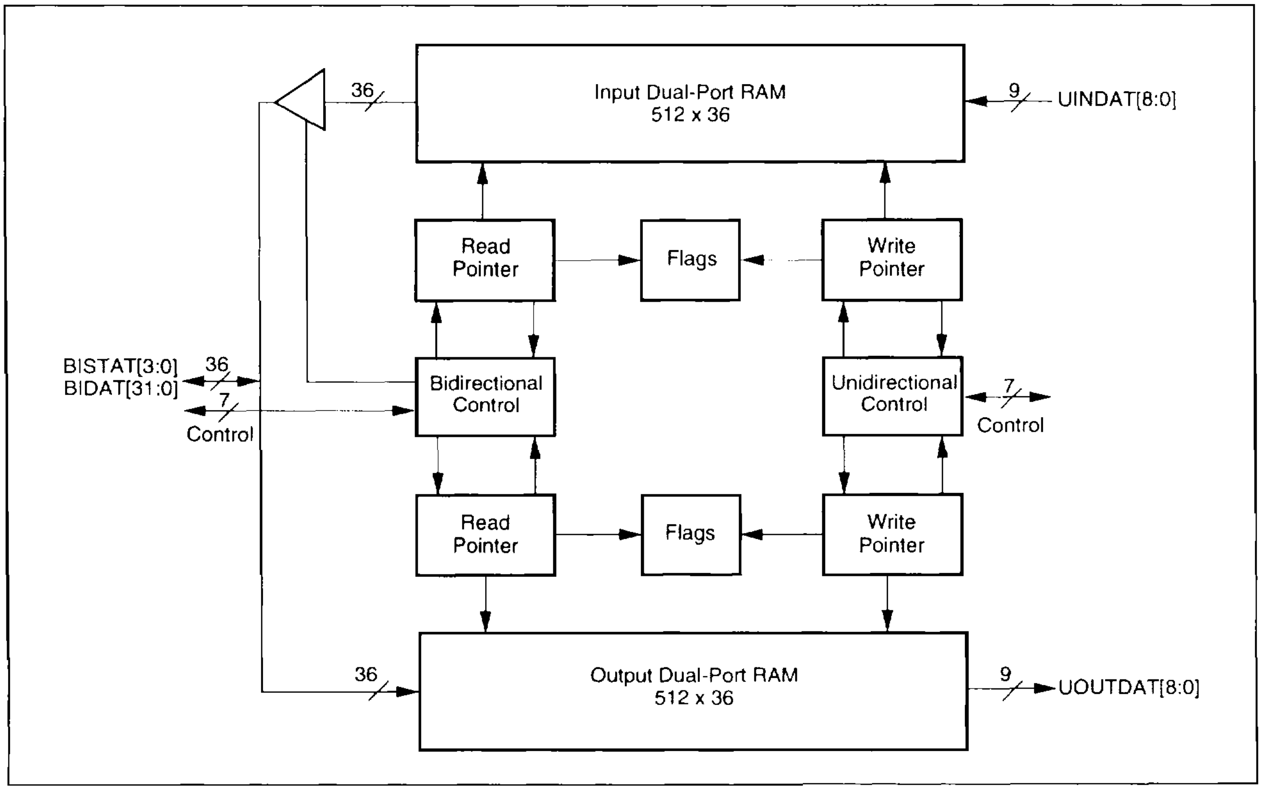
A block diagram of the bidirectional cell buffer is shown in Figure 1-1. Each 512 x 36 dual-port RAM bank has an associated read and write pointer and flag circuitry. The read and write pointers are sequentially incremented on read and write operations, respectively. The pointers are 9 bits wide to cover the address range of the dual-port RAM. The flag circuitry compares the flags to determine empty, almost-empty, half-full, almost-full, and full conditions.

The unidirectional control block controls read and write pointers, flags, and strobe outputs for the unidirectional port, and supports padding and cascade operations. The unidirectional interface operates with synchronous or asynchronous timing operation, and supports a parity check/generate operation in microprocessor mode.

The bidirectional control block controls the read and write pointers, flags, and strobes for the bidirectional port. It supports either the stand-alone smart FIFO mode or the microprocessor mode. The bidirectional interface supports synchronous or asynchronous timing operation in the stand-alone smart FIFO mode and a dedicated synchronous processor interface in the microprocessor mode.

Control of features is performed through input pins in the stand-alone smart FIFO mode and through control registers in the microprocessor mode.

Figure 1-1. Functional Block Diagram

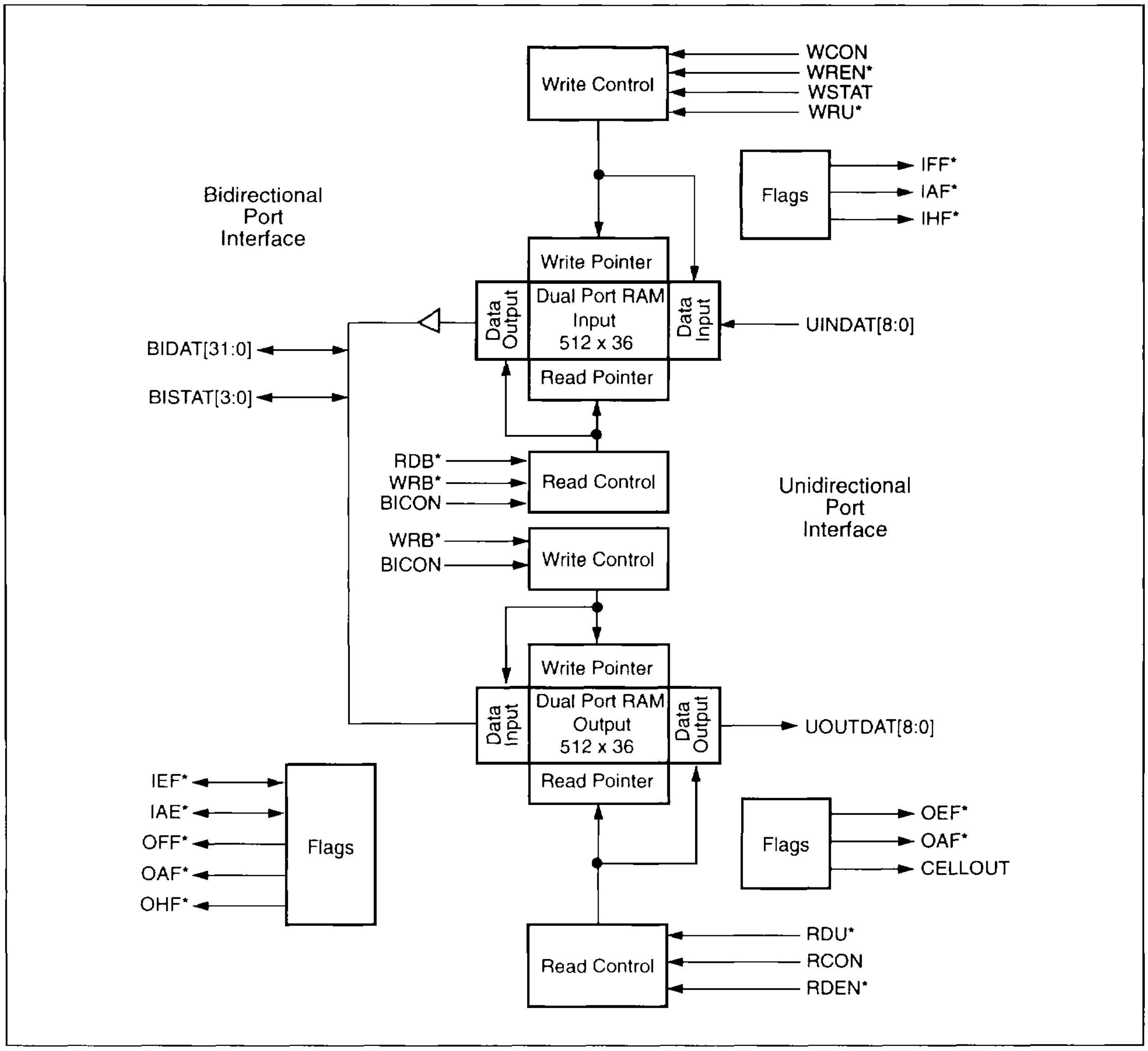


2.0 Stand-Alone Smart FIFO Mode

2.1 System Overview

Stand-alone smart FIFO mode provides a basic buffer interface for the bidirectional port. Several clocking schemes and multiple interface options are available for connecting unidirectional byte-wide signals to a bidirectional 32-bit interface. The buffer absorbs timing differences and can pack an odd number of bytes into a 32-bit word format. Figure 2-1 illustrates a block diagram of the Bt8215.

Figure 2-1. Stand-Alone Smart FIFO Mode Block Diagram



2.2 Pin Descriptions

A functionally partitioned logic diagram of the bidirectional cell formatter in stand-alone smart FIFO mode is shown in Figure 2-2. The unidirectional port inputs and outputs are shown at the top of the diagram. The inputs to this interface consist of byte-wide input (UINDAT), write control signals (WCON, WREN*, WSTAT, and WRU*), and read control signals (RCON, RDEN*, and RDU). The outputs from the unidirectional byte-wide port are cell markers and full, almost-full, half-full, almost-empty, and empty flags.

The bidirectional interface consists of input strobes to initiate read and write operations and a single control lead. Bidirectional pins provide 32 bits of data and 4 status bits. Output pins are provided for flags.

All control in stand-alone smart FIFO mode is hard-wired. There are retransmit controls for the input and output buffers, five control inputs, and one reset for each of the input and output buffers. To select stand-alone smart FIFO mode, the MODE input must be a logic low. The bidirectional port modes are selected through the BIMODE input; unidirectional port modes are selected through inputs S[0], S[1], and S[2]. The input buffer read and write pointers are reset by a logic low on RSTIN* and the output buffer pointers are reset by a logic low on RSTOUT*. The RTIN* input will asynchronously reset the input buffer read pointer to the physical beginning of the buffer. The RTOUT* input will asynchronously reset the output buffer read pointer to the beginning of the output buffer. Table 2-1 gives the pin descriptions, labels, and I/O assignments for the stand-alone smart FIFO mode.

Figure 2-2. Stand-Alone Smart FIFO Mode Logic Diagram

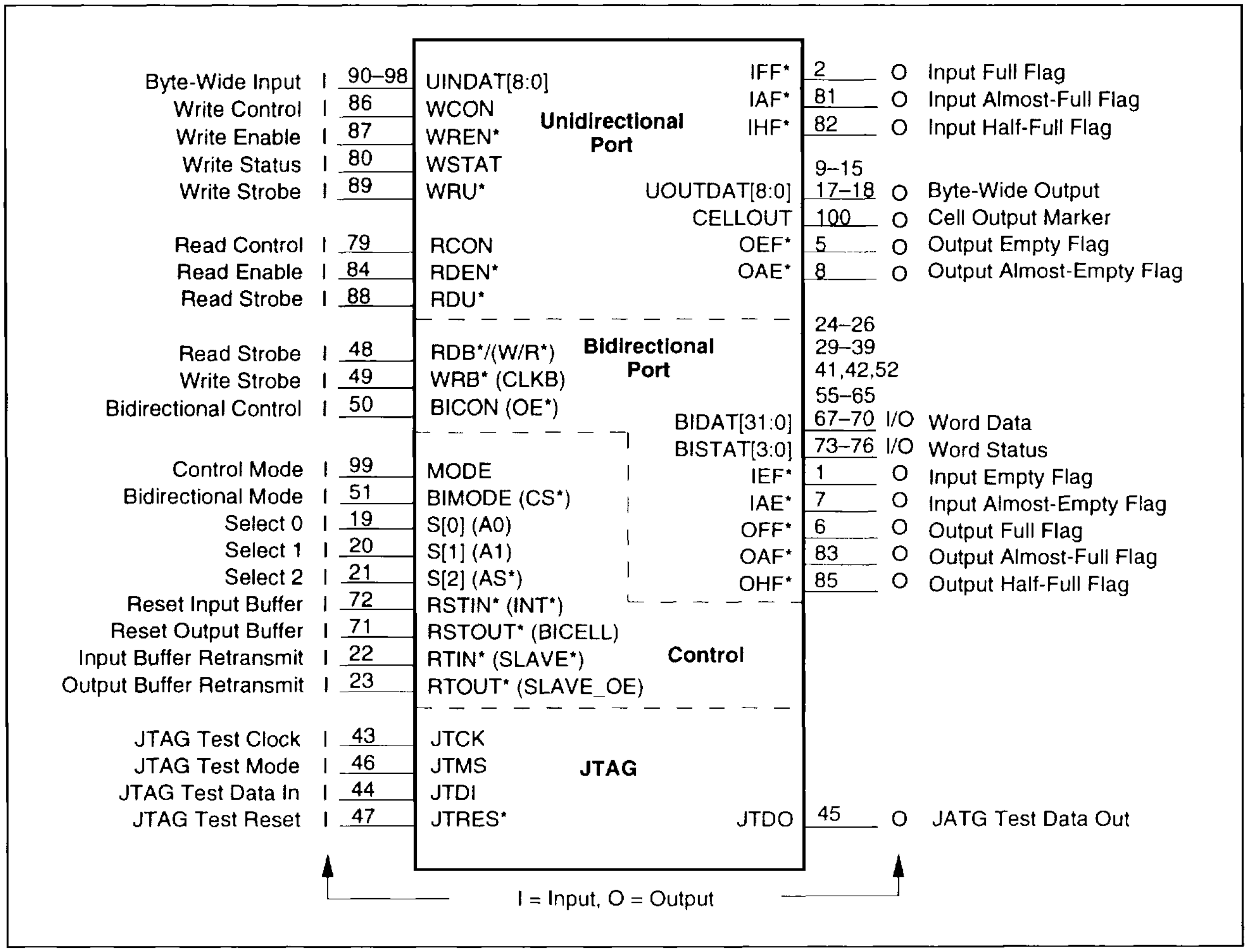

Byte-Wide Input I 90–98 UINDAT[8:0]
Write Control I 86 WCON
Write Enable I 87 WREN*
Write Status I 80 WSTAT
Write Strobe I 89 WRU*
Unidirectional Port
IFF* 2 O Input Full Flag
IAF* 81 O Input Almost-Full Flag
IHF* 82 O Input Half-Full Flag
UOUTDAT[8:0] 9–15 17–18 O Byte-Wide Output
CELLOUT 100 O Cell Output Marker
OEF* 5 O Output Empty Flag
OAE* 8 O Output Almost-Empty Flag
Read Control I 79 RCON
Read Enable I 84 RDEN*
Read Strobe I 88 RDU*
Read Strobe I 48 RDB*/(W/R*)
Write Strobe I 49 WRB* (CLKB)
Bidirectional Control I 50 BICON (OE*)
Bidirectional Port
BIDAT[31:0] 24–26 29–39 41,42,52 55–65 67–70 I/O Word Data
BISTAT[3:0] 73–76 I/O Word Status
IEF* 1 O Input Empty Flag
IAE* 7 O Input Almost-Empty Flag
OFF* 6 O Output Full Flag
OAF* 83 O Output Almost-Full Flag
OHF* 85 O Output Half-Full Flag
Control Mode I 99 MODE
Bidirectional Mode I 51 BIMODE (CS*)
Select 0 I 19 S[0] (A0)
Select 1 I 20 S[1] (A1)
Select 2 I 21 S[2] (AS*)
Reset Input Buffer I 72 RSTIN* (INT*)
Reset Output Buffer I 71 RSTOUT* (BICELL)
Input Buffer Retransmit I 22 RTIN* (SLAVE*)
Output Buffer Retransmit I 23 RTOUT* (SLAVE_OE)
Control
JTAG Test Clock I 43 JTCK
JTAG Test Mode I 46 JTMS
JTAG Test Data In I 44 JTDI
JTAG Test Reset I 47 JTRES*
JTAG
JTDO 45 O JATG Test Data Out
I = Input, O = Output

Table 2-1. Hardware Signal Definitions—Stand-Alone Smart FIFO Mode (1 of 2)

	Pin Label	Signal Name	I/O	Definition
Control Signals	MODE	Control Mode	I	Set to a logic low to select stand-alone smart FIFO mode.
	BIMODE (CS*)	Bidirectional Mode	I	Selects the bidirectional port modes. A logic low selects the asynchronous timing operation while a logic high selects synchronous timing.
	S[2:0] (A[1,0], AS*)	Select[2:0]	I	Selects the unidirectional port modes. Refer to Table 2-3
	RSTIN* (INT*)	Reset Input Buffer	I	An active-low input that resets the input buffer read and write pointers.
	RSTOUT* (BICELL)	Reset Output Buffer	I	An active-low input that resets the output buffer read and write pointers.
	RTIN* (SLAVE*)	Retransmit Input Buffer	I	An active-low input that asynchronously resets the input buffer read pointer to the physical beginning of the input buffer.
	RTOUT* (SLAVE_OE)	Retransmit Output Buffer	I	An active-low input that asynchronously resets the output buffer read pointer to the physical beginning of the output buffer.
Unidirectional Port	RCON	Read Control	I	Provides control of the unidirectional output port.
	RDEN*	Read Enable	I	An active-low input that enables reading of the unidirectional output port.
	RDU*	Read Strobe	I	Clocks the unidirectional output port.
	WRU*	Write Strobe	I	Clocks the unidirectional input port.
	WSTAT	Write Status	I	Provides control of the unidirectional input port.
	WREN*	Write Enable	I	An active-low input that enables writing of the unidirectional input port.
	WCON	Write Control	I	Provides control of the unidirectional input port.
	UINDAT[8:0]	Byte-Wide Input	I	The unidirectional byte-wide input data.
	IFF*	Input Full Flag	O	Provides full status for the input buffer.
	IAF*	Input Almost-Full Flag	O	Provides almost-full status for the input buffer.
	IHF*	Input Half-Full Flag	O	Provides half-full status for the input buffer.
	OAE*	Output Almost-Empty Flag	O	Provides almost-empty status for the output buffer.
	OEF*	Output Empty Flag	O	Provides empty status for the output buffer.
	CELLOUT	Cell Output	O	Used as a TAXI interface transmit strobe.
	UOUTDAT[8:0]	Byte-Wide Output	O	The unidirectional byte-wide output data.

Table 2-1. Hardware Signal Definitions—Stand-Alone Smart FIFO Mode (2 of 2)

	Pin Label	Signal Name	I/O	Definition
Bidirectional Port	RDB* (W/R*)	Read Strobe	I	Used as a read strobe in asynchronous timing operation and as a read enable in synchronous mode.
	WRB*(CLKB)	Write Strobe	I	Used as a write strobe in asynchronous timing mode. In synchronous timing mode, this pin is used as a bidirectional port clock.
	BICON (OE*)	Bidirectional Control	I	Not used in asynchronous timing mode, and should be tied low. Used as a write enable in synchronous timing mode.
	OHF*	Output Half-Full Flag	O	Provides half-full status for the output buffer.
	OAF*	Output Almost-Full Flag	O	Provides almost-full status for the output buffer.
	OFF*	Output Full Flag	O	Provides full status for the output buffer.
	IAE*	Input Almost-Empty Flag	O	Provides almost-empty status for the input buffer.
	IEF*	Input Empty Flag	O	Provides empty status for the input buffer.
	BISTAT[3:0]	Bidirectional Word Status	I/O	Provides a status bit for each byte on BIDAT[31:0].
	BIDAT[31:0]	Bidirectional Data Word	I/O	The bidirectional 32-bit wide data bus.
JTAG	JTCK	JTAG Test Clock	I	The test clock input.
	JTMS	JTAG Test Mode	I	A serial command input that sets up various JTAG tests.
	JTDI	JTAG Test Data In	I	The JTAG serial data input.
	JTRES*	JTAG Test Reset	I	An active-low signal that asynchronously resets the JTAG test circuitry.
	JTDO	JTAG Test Data Out	O	The JTAG serial data output.
VCC and GND	V_{CC}	Supply Voltage	–	Five pins are provided for power.
	GND	Ground	–	Six pins are provided for ground.

2.3 Bidirectional Port Control

The bidirectional port has two interface timing selections: asynchronous and synchronous. A logic low on the BIMODE input selects asynchronous timing operation. In this case, reading and writing are controlled by the use of strobes, providing identical operation to that of conventional buffers. With synchronous timing, reading and writing are controlled by a clock input and enable control signals on the input pins. Table 2-2 gives the pin functionality for both timing functions. This mode provides a full complement of buffer status flags. These flag indications provide empty and full status for the input and output buffers.

Table 2-2. Bidirectional Mode Selection

BIMODE	RDB*	WRB*	BICON
0 = Asynchronous	Read Strobe	Write Strobe	0[1]
1 = Synchronous	Read Enable	Clock	Write Enable
Notes: (1). BICON is not used as a signal input and should be grounded for asynchronous timing operation			

2.3.1 Asynchronous Timing Operation

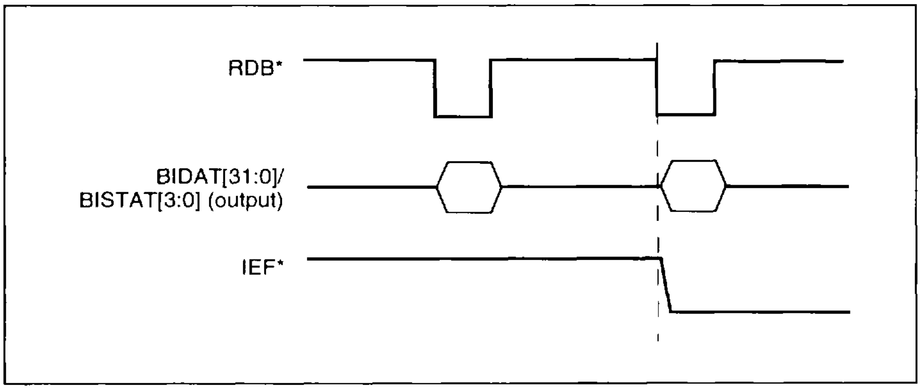
Asynchronous timing operation is provided for both reading from and writing to the bidirectional port. Since this port is bidirectional, the read and write operations cannot be active at the same time, except to transfer data from the input buffer to the output buffer. Detailed timing specifications for guard time between read and write operations are given in Chapter 5.0.

The read cycle begins when RDB* goes to a low state. The BIDAT[31:0] and BISTAT[3:0] buses are driven as outputs and the data being read becomes valid. The rising edge of RDB* clocks the output buffer read pointer and disables the BIDAT[31:0] and BISTAT[3:0] buses. When the last location of the input buffer containing data is read, IEF* goes active on the falling edge of RDB* and inhibits further reading of the input buffer.

A functional timing diagram for this operation is shown in Figure 2-3, where the input buffer empty flag is active on the second read operation.

IEF* goes high after an input buffer write operation from the byte-wide port to a 36-bit boundary. This occurs when either 4 bytes have been written to the input buffer or a padding operation has been performed at the byte-wide port. A read cycle can start while IEF* is active, thus decreasing the read on empty time. While IEF* is active, RDB* can be applied. Upon a valid write, data is present at BIDAT[31:0] and IEF* goes high. The read cycle can then be completed by setting RDB* high.

Figure 2-3. Bidirectional Asynchronous Read Timing

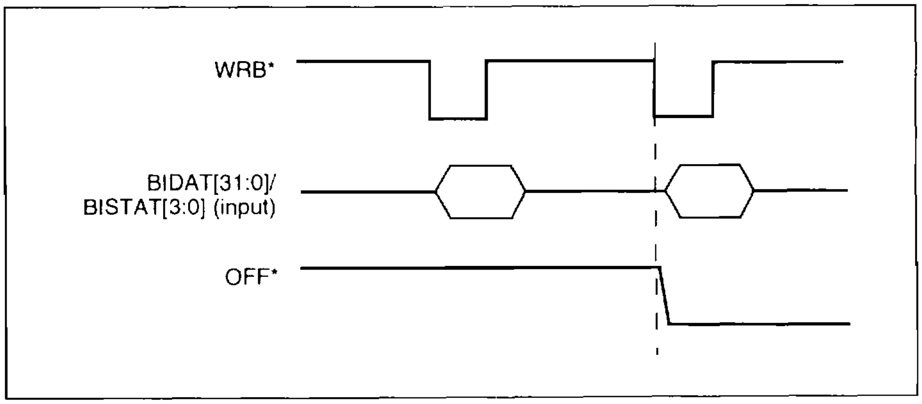


As shown in Figure 2-4, the write cycle begins when WRB* goes to a low state. Setup of the data on BIDAT[31:0] and BISTAT[3:0] to the buffer starts when WRB* is low. On the rising edge of WRB*, the data is stored in the buffer and the write pointer is incremented. The full flag, OFF*, goes active on the falling edge of WRB* when writing to the last available memory location of the output buffer. While OFF* is active, writing to the output buffer is inhibited. The output buffer full flag is shown going active after the second write operation.

OFF* goes inactive when a word has been read from the output buffer. A write cycle can start while OFF* is active. WRB* is applied while OFF* is active. Upon a valid read, OFF* will go inactive and WRB* can then go high to clock data into the buffer.

Data can be transferred from the input buffer to the output buffer by operating WRB* and RDB* together. Data should not be applied to the bidirectional data port when this operation is taking place.

Figure 2-4. Bidirectional Asynchronous Write Timing



2.3.2 Synchronous Timing Operation

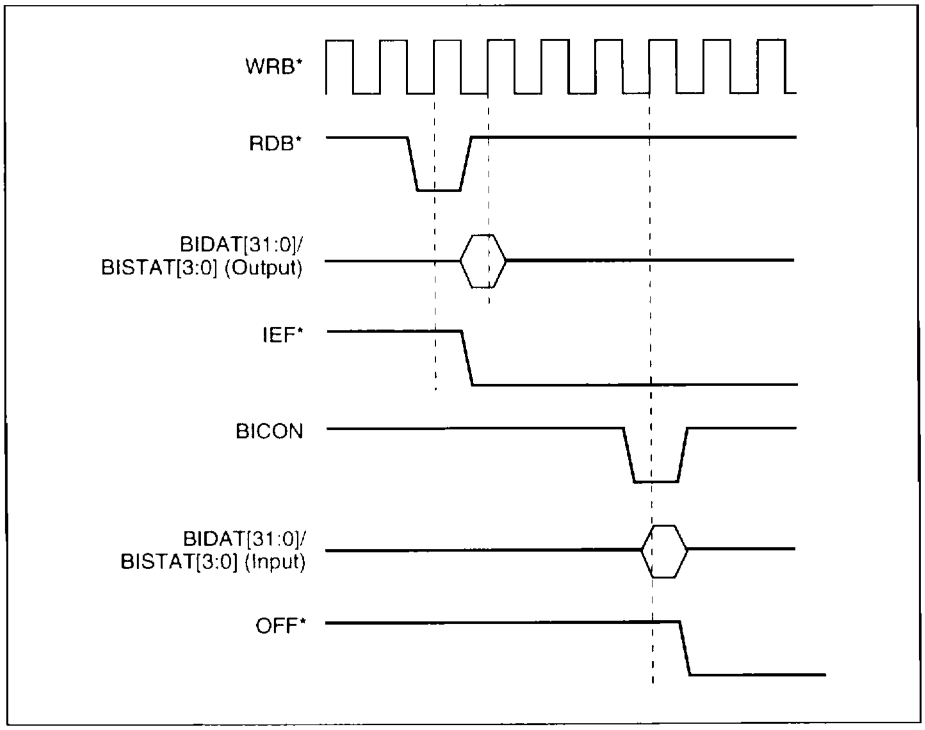
In synchronous timing operation, reading and writing are controlled by enable signals and a common clock. This function allows connection of the bidirectional port to a Reduced Instruction Set Computer (RISC) microprocessor or other state-machine implementation.

A read operation is performed by setting RDB* low before the clock cycle for which the read is to be performed. When RDB* is sampled low by the rising edge of the clock on WRB*, the port is enabled and valid data is applied to the bus. If the last location of the input buffer is being read, then IEF* will go low and the data from the last location will be valid. After a word write to the input buffer, IEF* will go high on the next rising edge of the clock. While IEF* is low, reading of the input buffer is inhibited; read-enable signals will be ignored.

Data on BIDAT[31:0] is written to the output buffer when BICON is sampled low on a rising edge of the clock signal on WRB*. This also increments the write pointer. The full flag, OFF*, goes active on the rising edge of the clock during a write to the last available location of the output buffer. While OFF* is active, writing to the output buffer is inhibited. OFF* goes inactive on the rising edge of WRB* after a word read from the output buffer.

Figure 2-5 shows a read operation followed by a write operation, with each function initiating flags. RDB* and BICON can be low on the same clock cycle, resulting in a write on that clock cycle and a read on the following cycle.

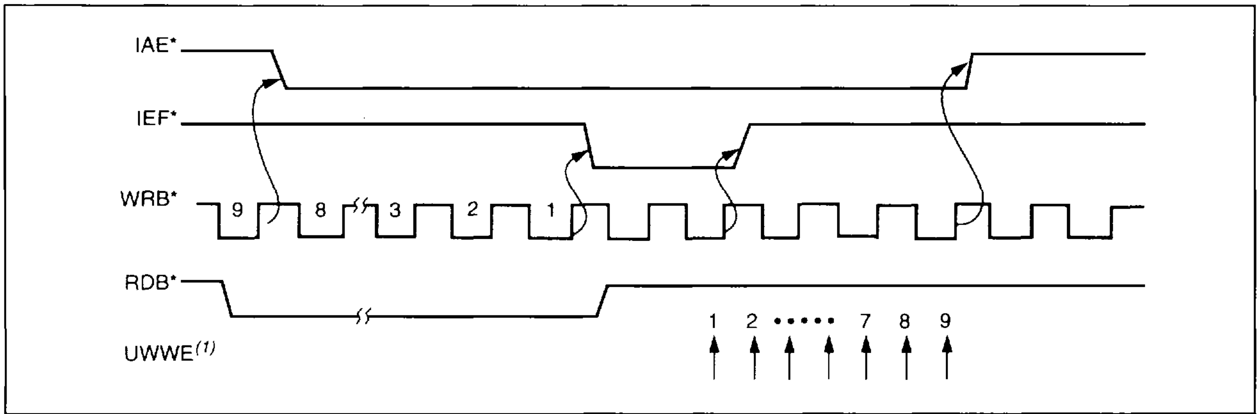
Figure 2-5. Synchronous Bidirectional Port Read and Write



2.3.3 Bidirectional Almost-Empty, Almost-Full, and Half-Full Flags

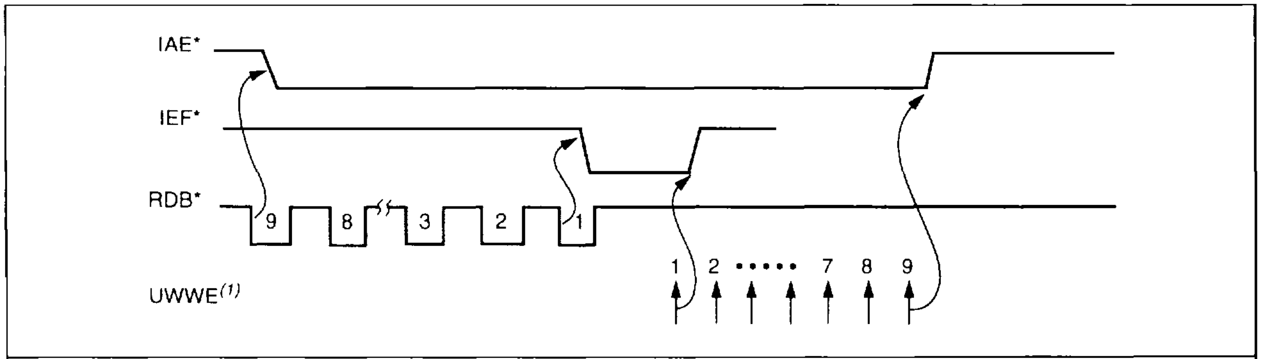
IAE* provides almost-empty status for the input buffer. The offset is preset at eight words for the stand-alone smart FIFO mode. Flag timing depends on the port timing. The flag goes active in conjunction with a read of the input buffer. If the reading port is synchronous, the flag goes active on the rising edge of the read clock (see Figure 2-6). If it is asynchronous, it goes active when the read strobe goes low (see Figure 2-7). Similarly, the flag goes inactive in conjunction with a write of the buffer. It goes inactive in response to either the rising edge of a write strobe in asynchronous operation or the rising edge of the read clock input following a write operation in synchronous mode. Transitions of the flag only occur on word boundaries.

Figure 2-6. IAE Synchronous Operation*



Notes: (1). Unidirectional Port Word Write Event. The event consists of 4 unidirectional byte writes or 1–3 unidirectional byte writes with WCON input low on the last byte write, i.e., pad insertion.

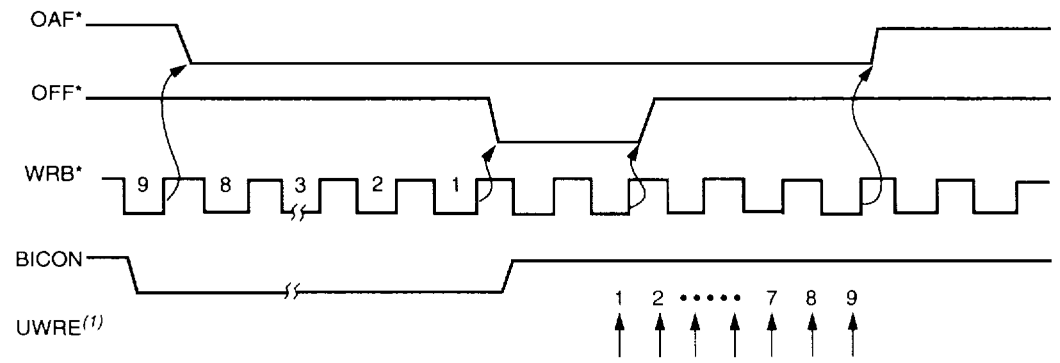
Figure 2-7. IAE Asynchronous Operation*



Notes: (1). Unidirectional Port Word Write Event. The event consists of 4 unidirectional byte writes or 1–3 unidirectional byte writes with WCON input low on the last byte write, i.e., pad insertion.

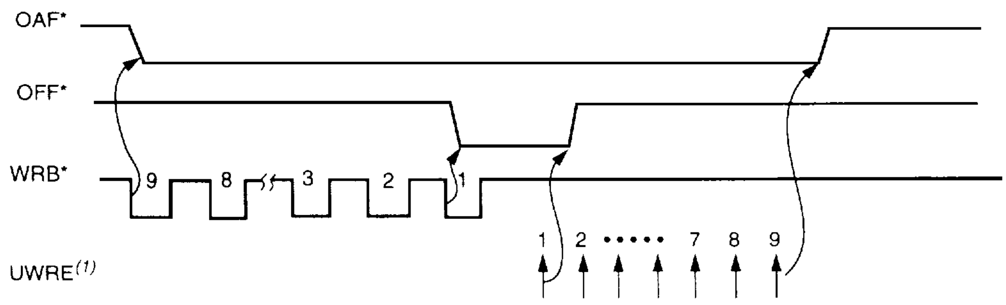
OAF* provides almost-full status for the output buffer. The offset is preset at eight words for the stand-alone smart FIFO mode. Flag timing depends on the port timing. The flag goes active in conjunction with a write of the output buffer. If the writing port is synchronous, the flag goes active on the rising edge of the write clock (see Figure 2-8). If it is asynchronous, it goes active when the write strobe goes low (see Figure 2-9). Similarly, the flag goes inactive in conjunction with a read of the buffer in response to either the rising edge of a read strobe in asynchronous operation or the rising edge of the write clock input following a read operation in synchronous mode. Transitions of the flag only occur on word boundaries.

Figure 2-8. OAF Synchronous Operation*



Notes: (1). Unidirectional Port Word Read Event. This event consists of 4 unidirectional reads or 1–3 unidirectional byte reads with RCON input low on last byte read, i.e., pad extraction.

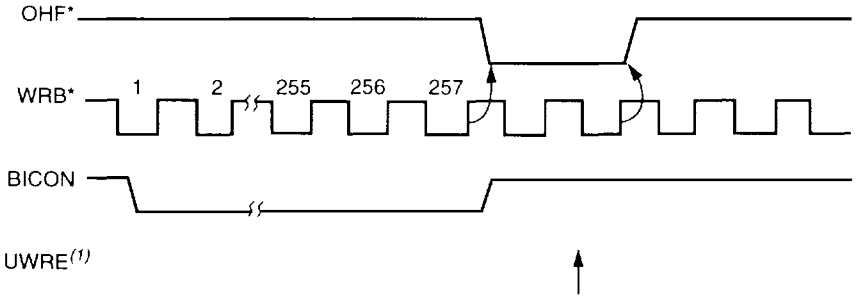
Figure 2-9. OAF Asynchronous Operation*



Notes: (1). Unidirectional Port Word Read Event. This event consists of 4 unidirectional reads or 1–3 unidirectional byte reads with RCON input low on last byte read, i.e., pad extraction.

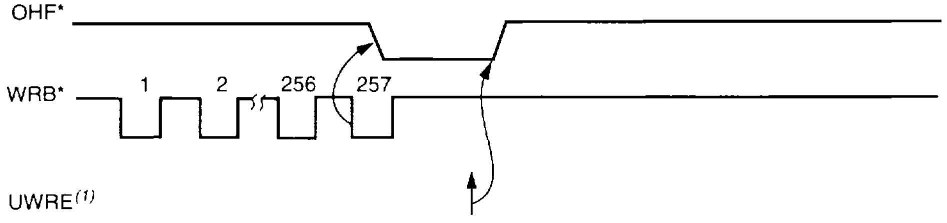
OHF* provides half-full status for the output buffer. An active flag indicates that the output buffer is greater than half full. Flag timing depends on the port timing. The flag goes active in conjunction with a write of the buffer. If the writing port is synchronous, the flag goes active on the rising edge of the write clock (see Figure 2-10). If it is asynchronous, it goes active when the write strobe goes low (see Figure 2-11). Similarly, the flag goes inactive in conjunction with a read of the buffer. It goes inactive in response to either the rising edge of a read strobe in asynchronous timing operation or the rising edge of the write clock input following a read operation in synchronous mode. Transitions of the flag only occur on word boundaries.

Figure 2-10. OHF Synchronous Operation*



Notes: (1). Unidirectional Port Word Read Event. This event consists of 4 unidirectional reads or 1–3 unidirectional byte reads with RCON input low on last byte read, i.e., pad extraction.

Figure 2-11. OHF Asynchronous Operation*



Notes: (1). Unidirectional Port Word Read Event. This event consists of 4 unidirectional reads or 1–3 unidirectional byte reads with RCON input low on last byte read, i.e., pad extraction.

2.4 Unidirectional Byte-Wide Port Control

In the stand-alone smart FIFO mode, the unidirectional port can operate in various timing interface regimes selected by the S[0], S[1], and S[2] input pins. The unidirectional timing interface selections are listed in Table 2-3.

Table 2-3. Unidirectional Byte Mode Selection

Function	S[2]	S[1]	S[0]
Asynchronous	0	0	0
Synchronous	0	0	1
HDLC	1	Enable FCS	1
TAXI	0	1	1
Cascade-Async	0	1	0
Cascade-Sync	1	1	0

Synchronous and asynchronous timing operations are identical for both unidirectional and bidirectional interfaces. Selecting HDLC provides a parallel interface to the Brooktree Bt8330 HDLC controller. The TAXI mode interface connects directly to the AMD TAXI® part set. The two Cascade selections provide the ability to cascade the unidirectional port with conventional asynchronous and synchronous buffers, respectively.

All parallel interface selections have a 9-bit unidirectional port. Bit mapping from the bidirectional port to the unidirectional port is detailed in Table 2-4.

Table 2-4. Bidirectional to Unidirectional Bit Mappings

Bidirectional Pin	Unidirectional Input	Unidirectional Output	Description
BIDAT[31:24]	UINDAT[7:0]	UOUTDAT[7:0]	First Byte
BIDAT[23:16]	UINDAT[7:0]	UOUTDAT[7:0]	Second Byte
BIDAT[15:8]	UINDAT[7:0]	UOUTDAT[7:0]	Third Byte
BIDAT[7:0]	UINDAT[7:0]	UOUTDAT[7:0]	Fourth Byte
BISTAT[3]	UINDAT[8]	UOUTDAT[8]	First Byte Status
BISTAT[2]	UINDAT[8]	UOUTDAT[8]	Second Byte Status
BISTAT[1]	UINDAT[8]	UOUTDAT[8]	Third Byte Status
BISTAT[0]	UINDAT[8]	UOUTDAT[8]	Fourth Byte Status

2.4.1 Asynchronous Timing Operation

Asynchronous timing provides a conventional strobed 9-bit buffer interface. Table 2-5 lists the control input and output pin functions for the unidirectional port.

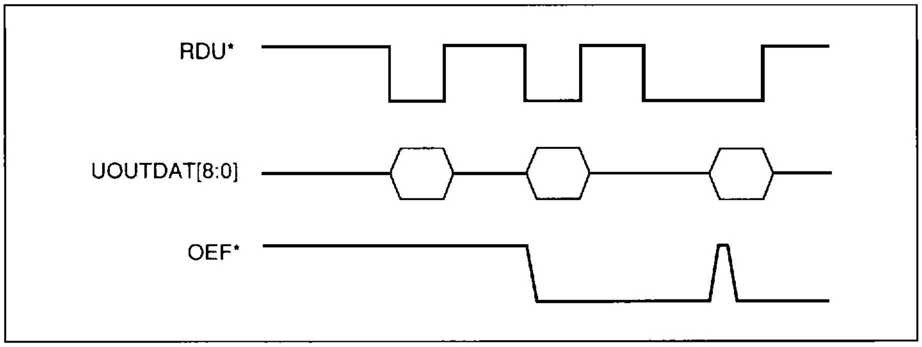
Table 2-5. Asynchronous Pin Functions for Unidirectional Port

Pin Name	Function
WCON	End Write Command for Padding, Active Low
WREN*	Not Used, Connect to Ground
WSTAT	Not Used, Connect to Ground
WRU*	Write Strobe, Active Low
RCON	End Read Command for Padding, Active Low
RDEN*	Not Used, Connect to Ground
RDU*	Read Strobe, Active Low
CELLOUT	Not Used
IFF*	Input Buffer Full Flag, Active Low
OEF*	Output Buffer Empty Flag, Active Low

As illustrated in Figure 2-12, the read cycle begins when RDU* goes to a low state. The data output drivers are enabled and the data on UOUTDAT[8:0] becomes valid. The rising edge of RDU* clocks the output buffer read pointer and three-states UOUTDAT[8:0]. Upon reading the last location of the output buffer, OEF* goes active on the falling edge of RDU* and inhibits further reading of the output buffer. An output buffer write operation occurring while OEF* is low causes this flag to change to a logic high. A read cycle can start while OEF* is active by applying RDU*. Upon a valid write, data is present at UOUTDAT[8:0] and OEF* goes high. The read cycle is then completed by setting RDU* high.

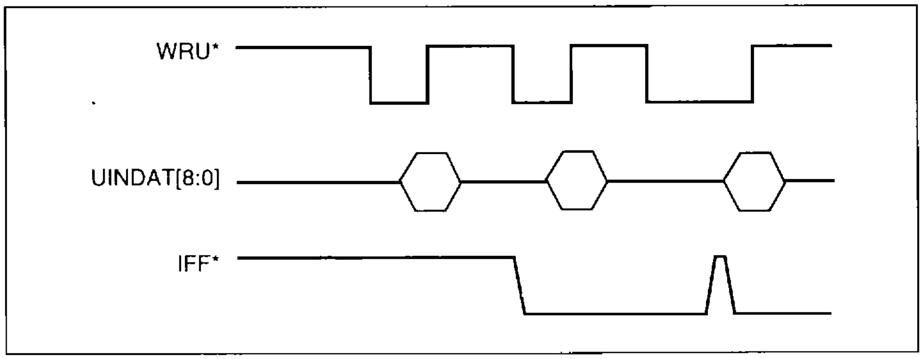
The second read operation empties the output buffer, so the output buffer empty flag goes low. It stays low, and if the read strobe is low when a write operation from the bidirectional port causes the buffer to read, the OEF* will pulse high and data will be enabled until the read strobe is released.

Figure 2-12. Unidirectional Asynchronous Read Operations



The write cycle begins when the write strobe WRU* goes to a low state (see Figure 2-13). Setup of the data on UINDAT[8:0] to the buffer starts when the write strobe is low. On the rising edge of the write strobe, the data is stored in the buffer and the write pointer is incremented. The full flag, IFF*, goes active on the falling edge of WRU* when writing to the last memory location of the input buffer. While IFF* is active, writing to the input buffer is inhibited. IFF* goes inactive on the first read of the input buffer. A write cycle can start while IFF* is active by applying WRU*, thus decreasing the write on full time. Upon a valid read, IFF* will go inactive and WRU* can then go high to clock data into the buffer.

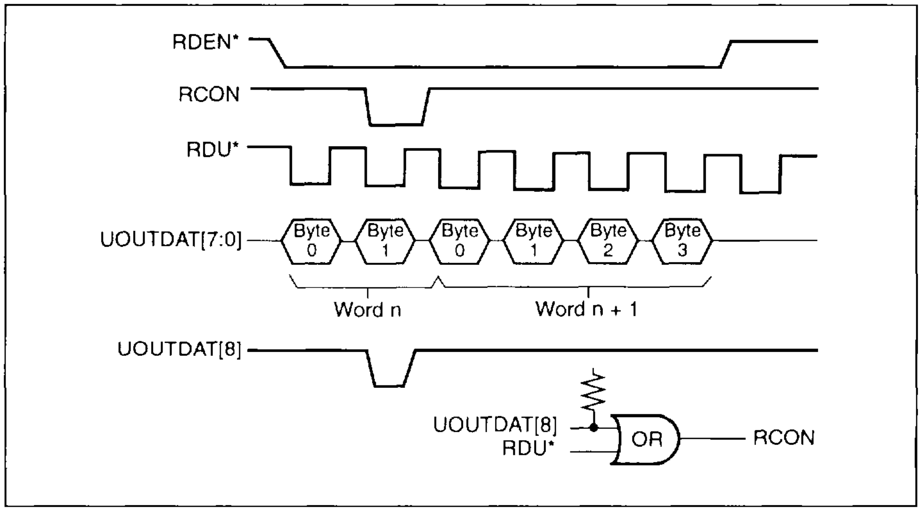
Figure 2-13. Unidirectional Asynchronous Write Operations



2.4.1.1 Insertion and Extraction of Pad Bytes, Asynchronous Mode

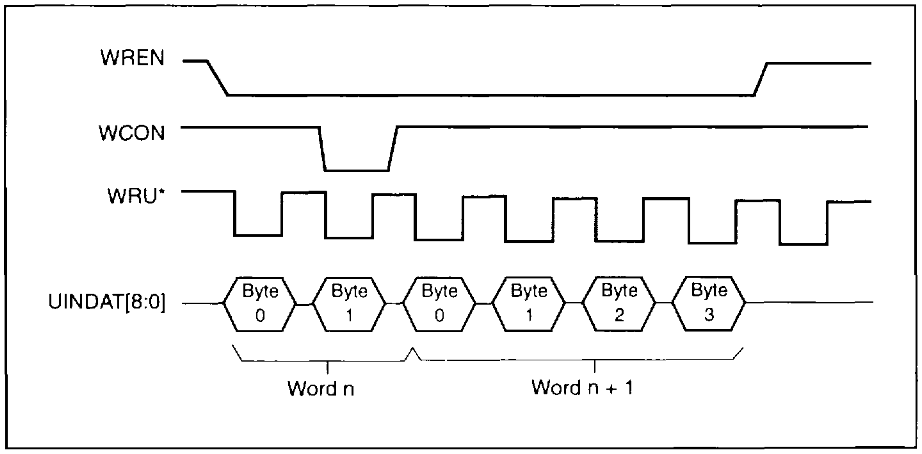
As shown in Figure 2-14 and Figure 2-15, asynchronous timing operation allows for the insertion of pad bytes in the 9-bit input port to fill to a 36-bit boundary, and for removal of pad bytes on the 9-bit output port. When RCON is low during a unidirectional read cycle, the read pointer is incremented to a 36-bit boundary at the end of the cycle. Bit 9 can be used as a delineation bit by connecting it to RCON. Due to the three-stated UOUTDAT[8] output, the user must ensure that RCON is a logic high before RDU* goes to a logic low. This can be accomplished by gating UOUTDAT[8] with RDU* externally.

Figure 2-14. Pad Byte Extraction



When WCON is a logic low during a write cycle, the next write cycle will store data starting on a 36-bit boundary. The pad byte value is undefined. The padding operation can be disabled during asynchronous operation by holding both RCON and WCON at a logic high.

Figure 2-15. Pad Byte Insertion



2.4.2 Synchronous Timing Operation

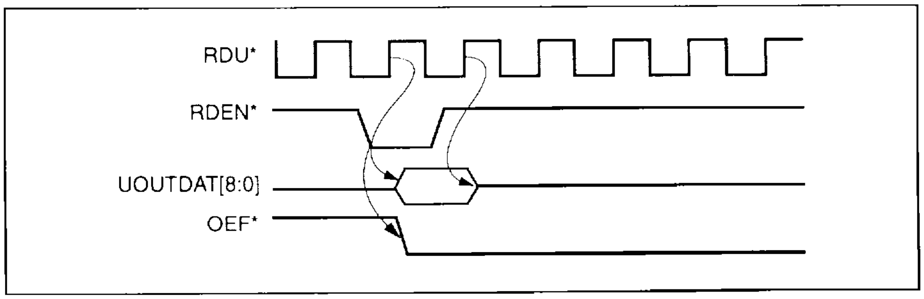
Synchronous timing operation provides a clocked 9-bit buffer interface. Separate read and write clocks and read-enable and write-enable signal inputs are provided. The control input and output pin functions for the unidirectional port are given in Table 2-6.

Table 2-6. Synchronous Pin Functions

Pin Name	Function
WCON	End Write Command For Padding, Active Low
WREN*	Write Enable, Active Low
WSTAT	Not Used, Connect to Ground
WRU*	Write Clock
RCON	End Read Command for Padding, Active Low
RDEN*	Read Enable, Active Low
RDU*	Read Clock
CELLOUT	Not Used
IFF*	Input Buffer Full Flag, Active Low
OEF*	Output Buffer Empty Flag, Active Low

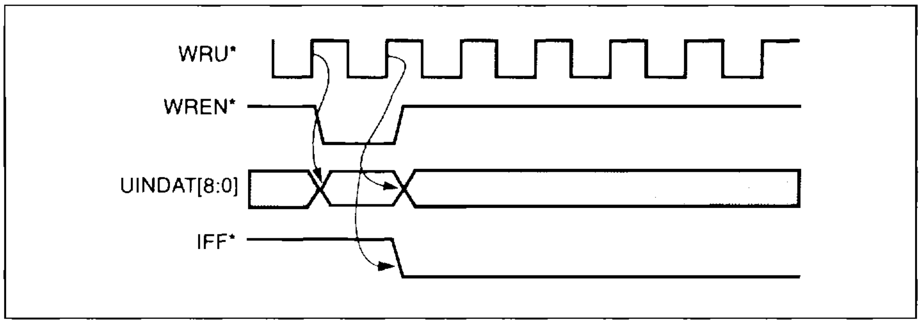
RDU* provides a free-running read clock to the unidirectional port (see Figure 2-16). When RDEN* is sampled low by the rising edge of the read clock on RDU*, the output unidirectional port is enabled and valid data is set up before the next rising clock edge. If the last location of the output buffer is being read, OEF* goes low and data from the last location becomes valid. After a write to the output buffer, OEF* goes high synchronous to the rising edge of RDU*. While OEF* is low, reading of the output buffer is inhibited.

Figure 2-16. Unidirectional Synchronous Read Timing



WRU* provides a free-running write clock to the unidirectional port (see Figure 2-17). When WREN* is sampled low by a rising edge of WRU*, unidirectional input data is written to the input register on the same rising clock edge. If a write to the last location of the input buffer occurs, IFF* goes low synchronous to the rising edge of WRU*. Upon reading the input buffer, IFF* goes inactive synchronous to WRU*. Writing to the input buffer is inhibited while IFF* is active.

Figure 2-17. Unidirectional Synchronous Write Timing



2.4.2.1 Insertion and Extraction of Pad Bytes, Synchronous Mode

As shown in Figure 2-18 and Figure 2-19, a capability for the insertion of pad bytes in the 9-bit input port to fill to a 36-bit boundary and for removal of pad bytes on the 9-bit output port is provided. When RCON is a logic low during a unidirectional read cycle, the read pointer is incremented to a 36-bit boundary at the end of the read cycle. Bit 9 can be used as a delineation bit by connecting the RCON input to ground. If this input is not tied to ground, it must be a logic high during reset to properly initialize the circuit.

When WCON is active during a write cycle, the next write cycle will store data starting on a 36-bit boundary. The pad byte value is undefined. By holding both RCON and WCON at a logic high, the padding operation can be disabled.

Figure 2-18. Synchronous Mode Pad Byte Insertion

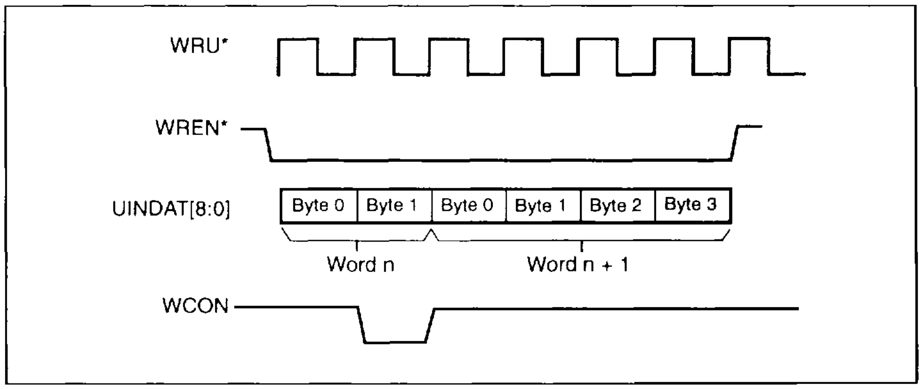
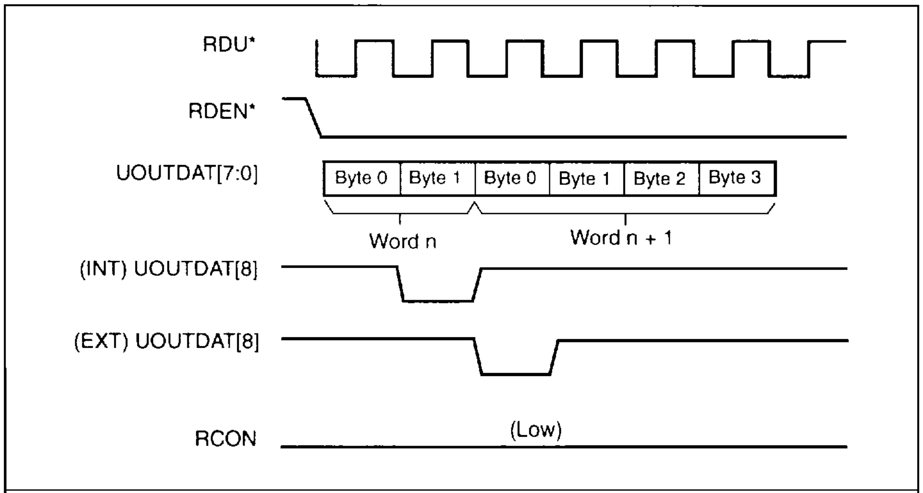


Figure 2-19. Synchronous Mode Pad Byte Extraction



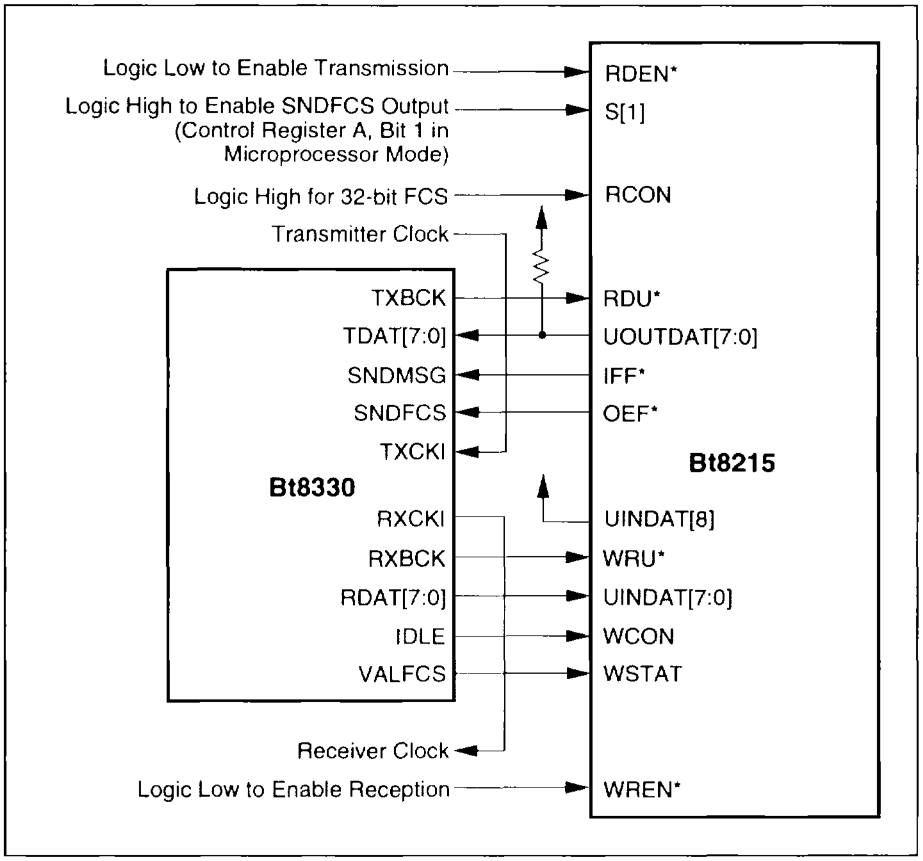
Note: The pipelined version of UOUTDAT[8] (INT) is used internally for delineation when RCON is tied low.

2.4.3 HDLC Operation

HDLC configures the unidirectional port to interface directly with the Bt8330 HDLC formatter. All HDLC-framed messages start on a 32-bit boundary for the buffer enabling easy reading and writing by a 32-bit processor. Bit 9 of each byte is used as a message delineation bit to indicate the last byte of each message.

The control input and output pin functions, as required for connection to the Bt8330, are shown in Figure 2-20. UINDAT[8] input must be tied to the power supply for proper operation. Pullup resistors are suggested on the UOUTDAT[7:0] bus since it is set to a high-impedance state during Frame Check Sequence (FCS) octets and when no message is being transferred.

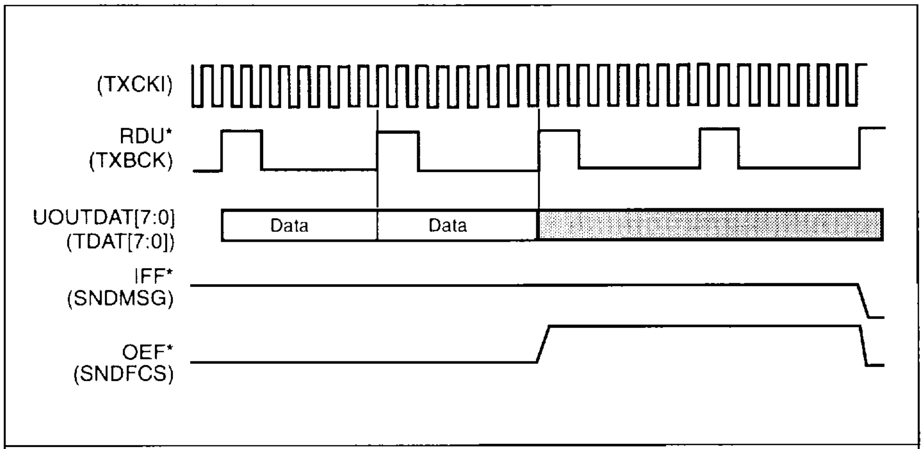
Figure 2-20. Pin Connections for HDLC Operation with the Bt8330



The HDLC formatter provides a transmit clock (TXBCK) to the output buffer. External circuitry provides the RDEN*, S[1], and RCON inputs, which control HDLC transmit functions. The output buffer provides the byte data, SNDMSG, and SNDFCS signals to the HDLC formatter.

Each transmitted frame starts on a 32-bit boundary when written to the output buffer. The delineation bit is low on the last octet of the frame prior to the FCS bytes. Transmission will start when RDEN* is at a logic low. If the output buffer is not empty and RDEN* is low, then the IFF* output goes to a logic high. The frame is continuously transmitted until the delineation bit is encountered. Therefore, the output buffer must not be allowed to empty while a message is being transferred to the Bt8330. If SNDFCS is enabled (by setting the S[1] input to a logic high), OEF* will go to a logic high for 2 bytes if RCON is a logic low, or 4 bytes if RCON is a logic high. If SNDFCS is not enabled, the FCS is assumed to be generated by the microprocessor and the Bt8330 will not overwrite an FCS at the end of a message. At the end of the message, the read pointer is incremented to the next 32-bit boundary. Both IFF* and OEF* will be inactive for at least one clock period. Functional timing is shown in Figure 2-21

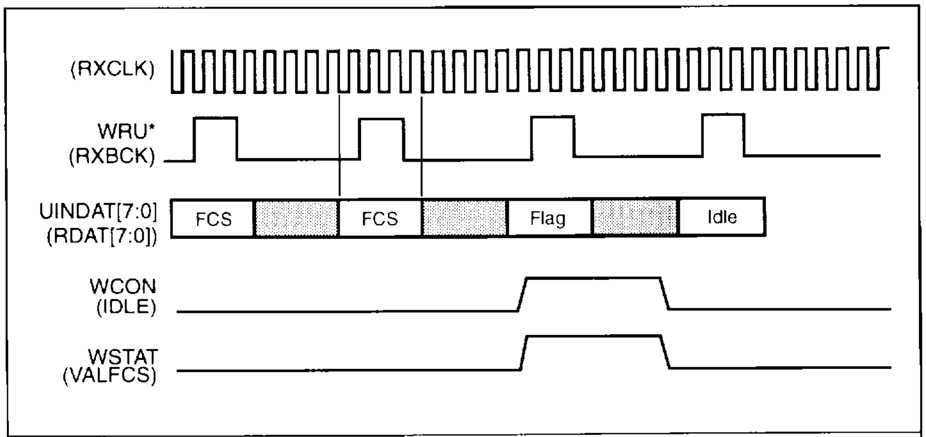
Figure 2-21. HDLC Transmit Timing



Note: Bt8330 signal names are enclosed in parentheses.

For reception, the HDLC formatter provides a receive clock RXBCK, IDLE, VALFCS, a receive status input to WREN*, and byte data to the input buffer. A frame starts on a 32-bit boundary. To initialize the writing of a frame, WREN* must be low and IDLE must be high. Writing starts when IDLE goes low. Functional timing is shown in Figure 2-22 (refer also to the Bt8330 specification).

Figure 2-22. HDLC Receive Timing



Note: Bt8330 signal names are enclosed in parentheses.

When VALFCS, IDLE or WREN* are high, a status byte and delineation bit (active low) are written to the input buffer. Note that the status byte is an additional byte position appended to the received HDLC frame. The read pointer is incremented to the next 32-bit boundary when the status byte is written, so that the next frame received will begin on a word boundary. The status word has four values:

1. End of message with invalid FCS (VALFCS = 0, IDLE = 1) results in a status value of 1;
2. End of message with good FCS (VALFCS = 1, IDLE = 1) results in a status value of 3
3. Abort sequence detected (VALFCS = 1, IDLE = 0) with status of 2
4. External abort error (caused by WREN* high during the message) with a status of greater than or equal to four (see Table 2-7).

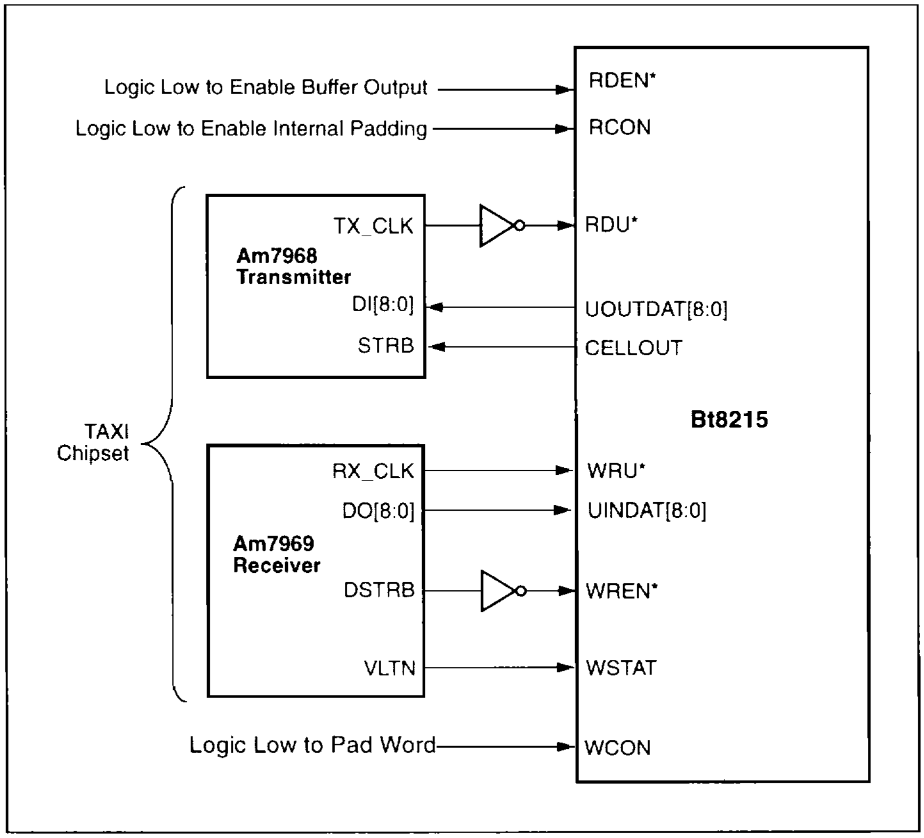
Table 2-7. HDLC Receive Status Byte

Status Byte	Description
000	Unused
001	Message with Bad FCS
010	Abort Received
011	Message with Good FCS
1xx	External Abort

2.4.4 TAXI Operation

TAXI timing configuration allows the unidirectional port to interface directly with the TAXI chipset. External circuitry can be added to control the interface to allow insertion of TAXI commands or data into the transmit path. Bit 9 can be configured to provide delineation or parity, or to mark violations. Pin connections for this configuration are shown in Figure 2-23. Pullup resistors should be attached to UOUTDAT[8:0] signals since they are three-stated when the interface is inactive.

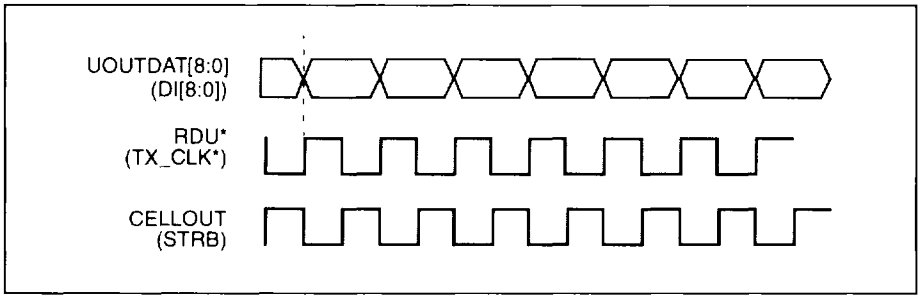
Figure 2-23. Pin Connections for Operation with TAXI Chipset



To transmit, the TAXI chipset provides the output buffer with a transmit clock connected to RDU*. The output buffer returns transmit data and a transmit strobe connected to STRB. Data is read from the output buffer synchronously to TX_CLK* whenever RDEN* is active and the buffer is not empty.

If RCON is connected to ground, bit 9 will be used for internal padding; this allows the Bt8215 to transfer partial words to the TAXI chipset. Otherwise, bit 9 can be used for parity or data and transmitted by the TAXI part. If RCON is not tied to ground, it must be a logic high during reset. Functional timing is shown in Figure 2-24.

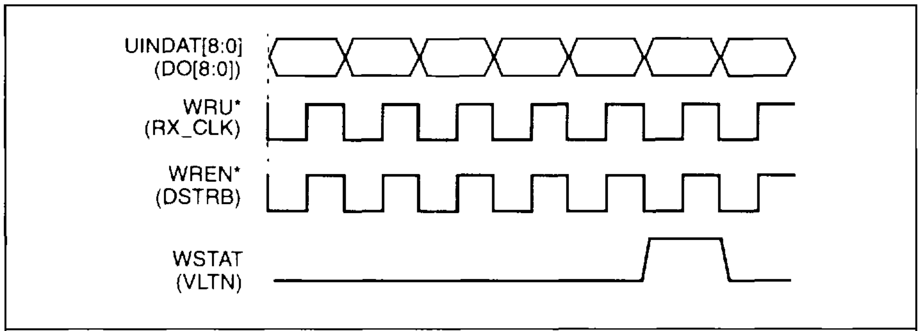
Figure 2-24. TAXI Transmitter Functional Timing



To receive, the TAXI chipset provides a receive clock (RX_CLK), receive strobe (DSTRB), violation indication (VLTN), and receive data signal (DO[8:0]), connected as shown in Figure 2-23. Whenever DSTRB is a logic high, data is written to the input buffer synchronously with RX_CLK. If padding is desired, this information must be transmitted in the TAXI by one of the data bits. This data output must be connected both to UINDAT[8] and WCON. When it is low, the following data will be written to the first byte in a word.

The VLTN output of the TAXI chipset may be connected to the WSTAT input of the Bt8215. A logic high on the VLTN output indicates a transmission error in the TAXI output data. A logic high on the WSTAT input inhibits the writing of data to the buffer. If this function is not desired, WSTAT can be tied to ground. Functional timing for the receiver is shown in Figure 2-25

Figure 2-25. TAXI Receiver Functional Timing



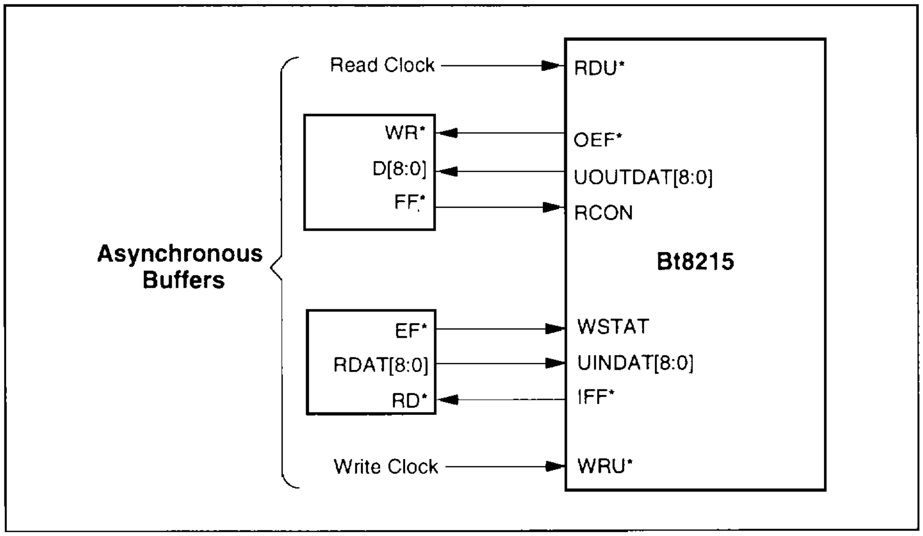
Note: Setup time requirement exists for WREN* relative to WRU*

2.4.5 Cascade with Asynchronous Buffers

This configuration allows cascading of the buffer with catalog asynchronous buffers. These buffers can be further cascaded among themselves for added depth. Padding is not supported in this mode. The pin connections are shown in Figure 2-26.

The interface to catalog buffers is autonomous and only requires a unidirectional read and write port clock. RDU* and WRU* can be tied together for single port clock operation. The basic timing of the unidirectional port is synchronous except that control signals pass between the devices.

Figure 2-26. Asynchronous Buffer Cascade Interface



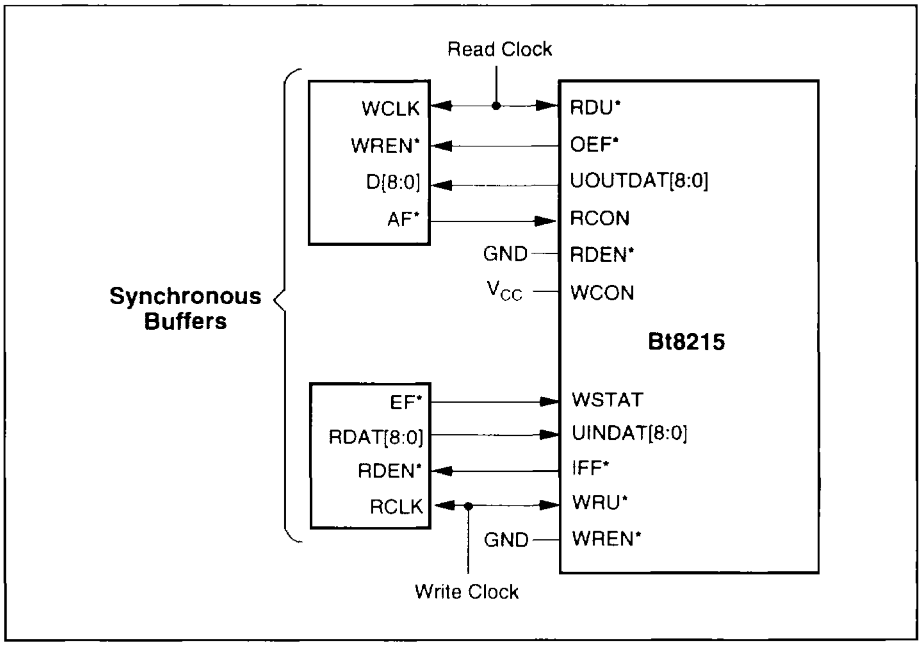
On the input side, the generic FIFO empty flag will be high when it has data. If the input buffer is not full and the generic FIFO has data, then the IFF* will toggle to read data into the input buffer until either the input buffer is full or the generic FIFO is empty. A similar control occurs on the output side. When the generic FIFO's full flag is high and the output buffer is not empty, then the OEF* will toggle to write data into the generic FIFO. This will continue until the slave is full or the master is empty.

Empty and full unidirectional indications are derived from generic FIFOs. On the input side, if the generic FIFO is full then the input buffer is also full; otherwise, it would be transferring data. On the output side, an empty generic FIFO indicates an empty output buffer; otherwise, it also would be transferring data.

2.4.6 Cascade with Synchronous Buffers

This is the same as asynchronous cascade except that the generic FIFOs are port synchronous. In this case, RSTB* and WSTB* do not have to toggle to perform reads or writes. The pin connections are shown in Figure 2-27. Also the generic FIFO must supply an almost-full flag instead of a full flag.

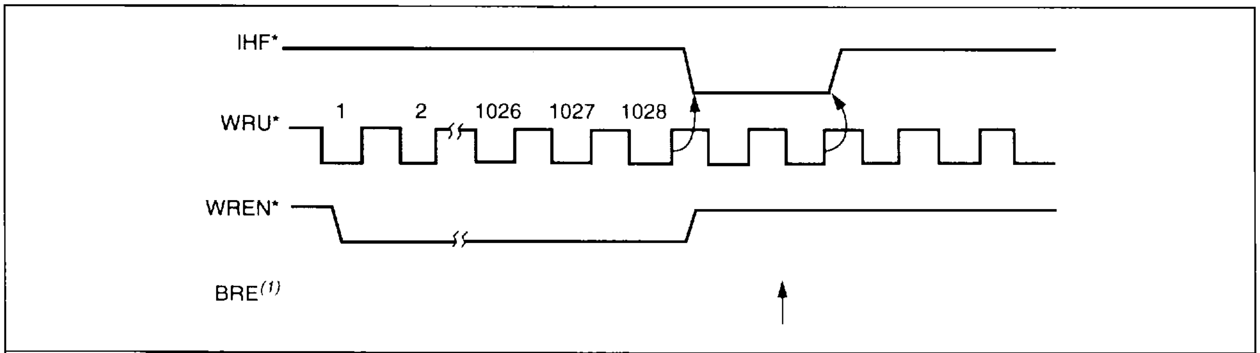
Figure 2-27. Synchronous Buffer Cascade Interface



2.4.7 Unidirectional Half-Full, Almost-Empty and Almost-Full Flags

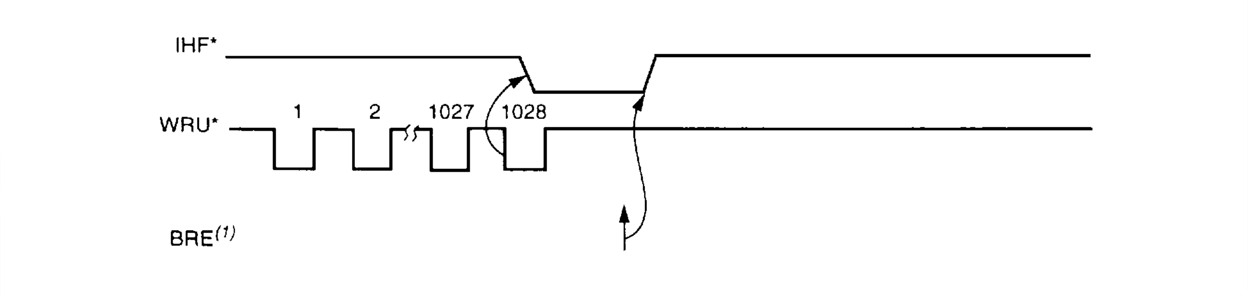
IHF* provides half-full status for the input buffer. An active flag indicates that the input buffer is greater than half full. Flag timing depends on the port timing. The flag goes active in conjunction with a write of the input buffer. If the writing port is not asynchronous, e.g., sync, TAXI, HDLC, the flag goes active on the rising edge of the write clock (see Figure 2-28). If it is asynchronous, it goes active when the write strobe goes low (see Figure 2-29). Similarly, the flag goes inactive in conjunction with a read of the buffer. It goes inactive in response to either the rising edge of a read strobe in asynchronous timing operation or the rising edge of the write clock following a read operation in synchronous mode. Flag transitions occur only on word boundaries.

Figure 2-28. IHF Synchronous Operation*



Notes: (1). Bidirectional Port Read Event.

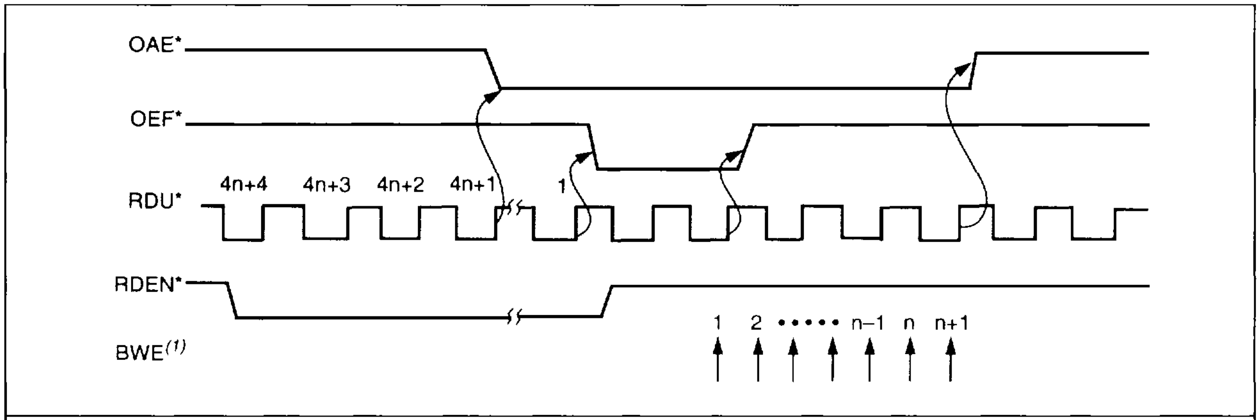
Figure 2-29. IHF Asynchronous Operation*



Notes: (1). Bidirectional Port Read Event.

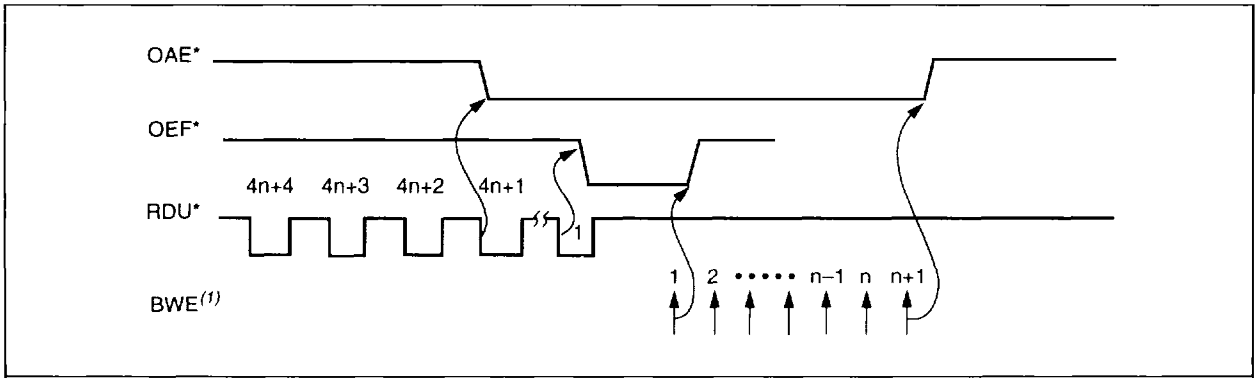
OAE* provides almost-empty status for the output buffer. The offset is preset at eight words (n = 8) for the stand-alone smart FIFO mode. Flag timing depends on the port timing. The flag goes active in conjunction with a read of the output buffer. If the reading port is not asynchronous, e.g., synchronous, TAXI, HDLC, the flag goes active on the rising edge of the read clock (see Figure 2-30). If it is asynchronous, the flag goes active when the read strobe goes low (see Figure 2-31). Similarly, the flag goes inactive in conjunction with a write of the buffer. It goes inactive in response to either the rising edge of a write strobe in asynchronous timing operation or the rising edge of the read clock input following a write operation in synchronous mode. Flag transitions occur only on word boundaries.

Figure 2-30. OAE Synchronous Operation*



Notes: (1). Bidirectional Port Write Event.

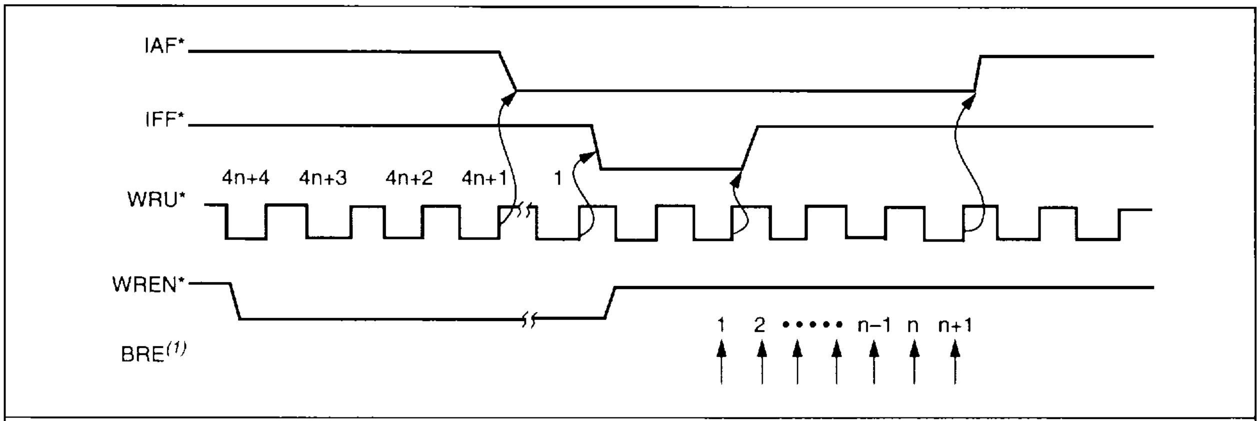
Figure 2-31. OAE Asynchronous Operation*



Notes: (1). Bidirectional Port Write Event.

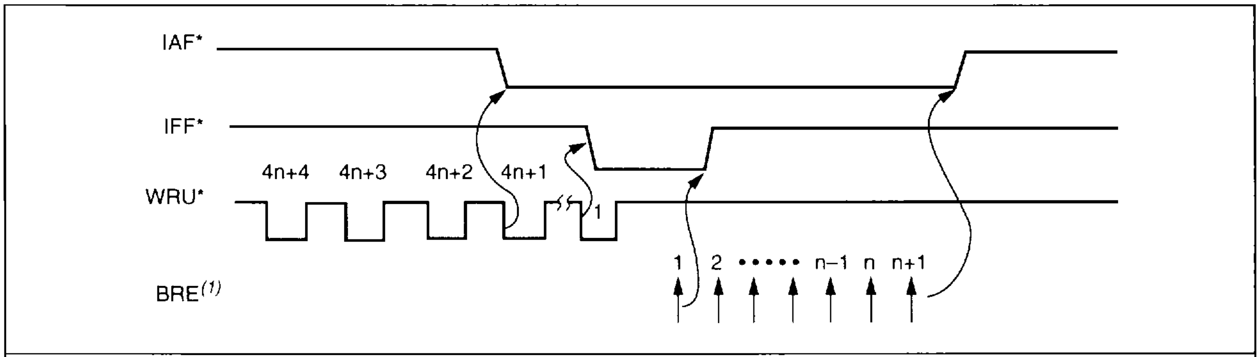
IAF* provides almost-full status for the input buffer. The offset is preset at eight words (n = 8) for the stand-alone smart FIFO mode. Flag timing depends on the port timing. The flag goes active in conjunction with a write of the input buffer. If the writing port is not asynchronous, e.g., synchronous, TAXI, HDLC, the flag goes active on the rising edge of the write clock (see Figure 2-32). If it is asynchronous, it goes active when the write strobe goes low (see Figure 2-33). Similarly, the flag goes inactive in conjunction with a read of the buffer and in response to either the rising edge of a read strobe in asynchronous timing operation or the rising edge of the write clock input following a read operation in synchronous mode. Flag transitions occur only on word boundaries.

Figure 2-32. IAF Synchronous Operation*



Notes: (1). Bidirectional Port Read Event.

Figure 2-33. IAF Asynchronous Operation*



Notes: (1). Bidirectional Port Read Event.

3.0 Microprocessor Control Mode

3.1 System Overview

The microprocessor control mode is selected by setting the MODE input to a logic high. The microprocessor interface is synchronous and can be configured to work with most 32-bit microprocessors. The microprocessor has access to two 32-bit control registers and one 32-bit status register. The control registers select the operational modes, the status register provides operational status.

The microprocessor control mode provides identical functionality to the stand-alone smart FIFO mode, in addition to providing a cell processing feature. The cell processing feature allows the buffer to process both fixed-length cells containing one- and two-word headers as well as variable length cells. Broadcast, start-cell, and end-cell operations are all modes of the cell processing operation. The broadcast mapping can be used to implement a hub or switch. The start-cell or end-cell operation can be used to implement an end point station. The difference in these submodes is in the way that cell headers are processed.

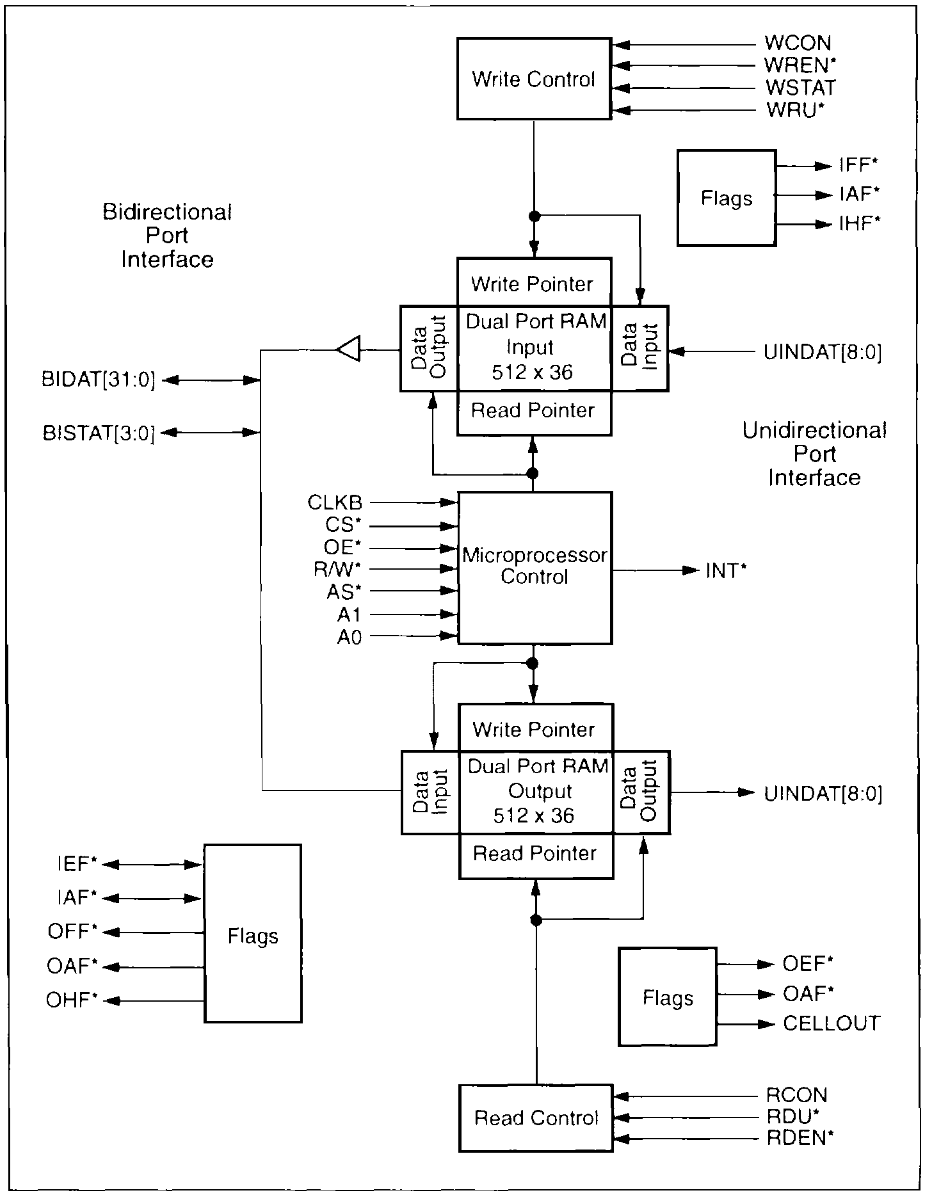
The minimum cell size is 8 octets and the maximum is 2047 octets. Operating modes are selected by bits 21 and 22 of Control Register A and are given in Table 3-1.

Table 3-1. Bidirectional Port Address Map

Mode	AddrMap[1] CRA.22	AddrMap[0] CRA.21
Smart FIFO Mode	0	0
Cell Processing: Broadcast Mode	0	1
Cell Processing: Start-Cell Mode	1	0
Cell Processing: End-Cell Mode	1	1

Figure 3-1 illustrates the block diagram for microprocessor mode. The bidirectional port operates under control of the microprocessor interface. All access (reading and writing) of the input and output buffers is accomplished with the A[0] and A[1] address pins (refer to Table 3-3 and Table 3-5). Multiple reads or writes may be performed (burst read/write cycle) and these cycles are limited only by the FIFO depth. Both the Bidirectional and Unidirectional ports may be active at the same time. Control Register A [CRA;0x00] may be used to configure the available options for both the unidirectional and the bidirectional ports. Control Register B [CRB;0x00] enables an interrupt capability upon a change of state of the buffer flags. The status register makes available various buffer status flags, parity, and delineation indications. These indicators are also available as external pins. The maximum clock rate for the bidirectional port is 33 MHz and the maximum clock rate for the unidirectional port is 20 MHz.

Figure 3-1. Cell Buffer System Diagram (Microprocessor Mode)



3.2 Pin Description

The microprocessor interface consists of nine pins: Chip Select (CS*), Address Strobe (AS*), Clock (CLKB), Write/Read* (W/R*), Output Enable (OE*), two address pins (A[0,1]), a control (MODE), and an interrupt (INT*). A logic diagram of the Bt8215 cell buffer is shown in Figure 3-2. Pins names shown in Figure 3-2 within parentheses have dual functions and alternate names defined for the stand-alone smart FIFO mode. The BICELL and INT* pins are open-drain outputs and may require pullup resisters for proper operation depending upon the application. Table 3-2 lists the pin descriptions, labels, and I/O assignments.

Figure 3-2. Cell Buffer Logic Diagram (Microprocessor Mode)

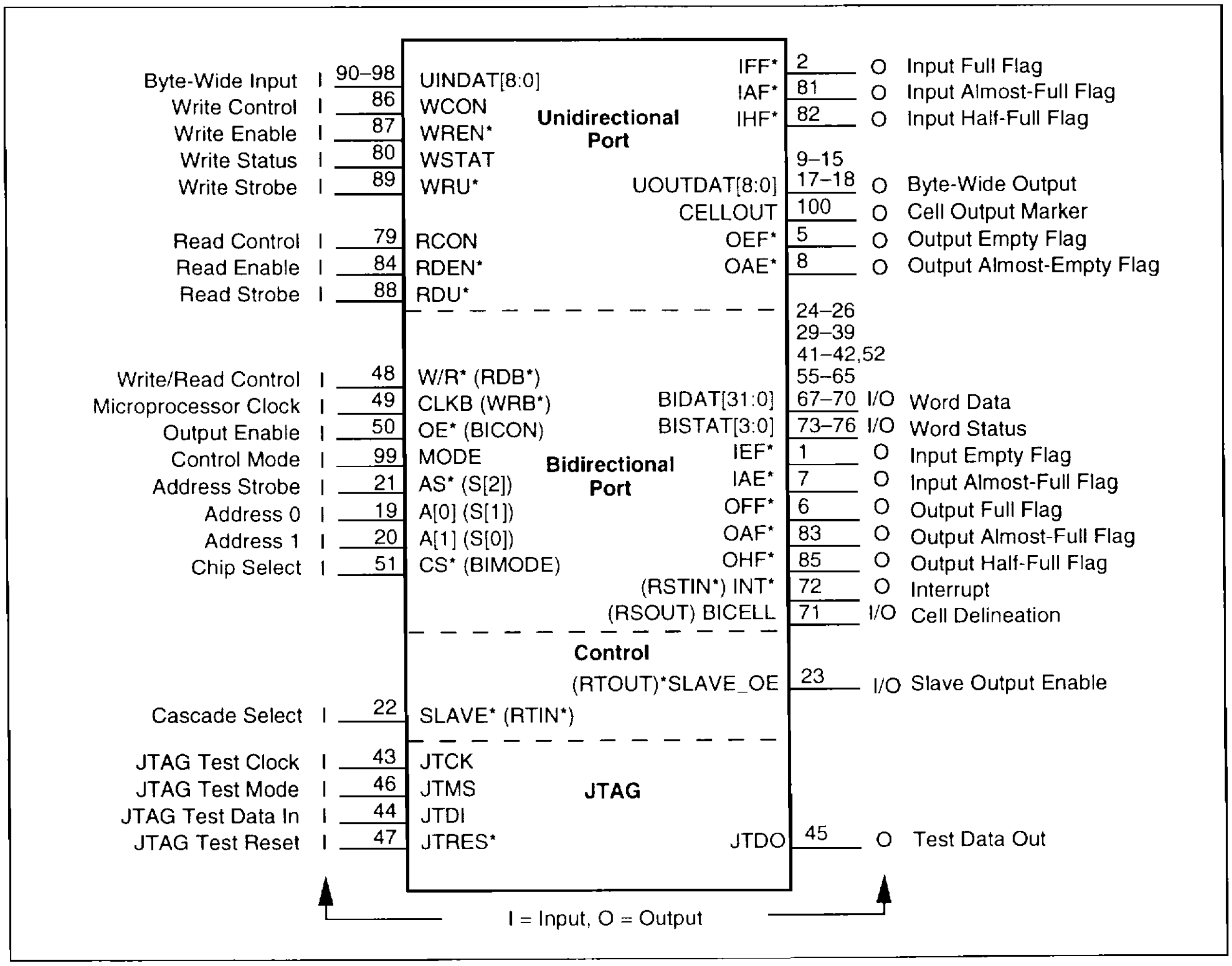

Byte-Wide Input I 90–98 UINDAT[8:0]
Write Control I 86 WCON
Write Enable I 87 WREN*
Write Status I 80 WSTAT
Write Strobe I 89 WRU*
Unidirectional Port
IFF* 2 O Input Full Flag
IAF* 81 O Input Almost-Full Flag
IHF* 82 O Input Half-Full Flag
UOUTDAT[8:0] 9–15 17–18 O Byte-Wide Output
CELLOUT 100 O Cell Output Marker
OEF* 5 O Output Empty Flag
OAE* 8 O Output Almost-Empty Flag
Read Control I 79 RCON
Read Enable I 84 RDEN*
Read Strobe I 88 RDU*
Write/Read Control I 48 W/R* (RDB*)
Microprocessor Clock I 49 CLKB (WRB*)
Output Enable I 50 OE* (BICON)
Control Mode I 99 MODE
Address Strobe I 21 AS* (S[2])
Address 0 I 19 A[0] (S[1])
Address 1 I 20 A[1] (S[0])
Chip Select I 51 CS* (BIMODE)
Bidirectional Port
BIDAT[31:0] 24–26 29–39 41–42,52 55–65 67–70 I/O Word Data
BISTAT[3:0] 73–76 I/O Word Status
IEF* 1 O Input Empty Flag
IAE* 7 O Input Almost-Full Flag
OFF* 6 O Output Full Flag
OAF* 83 O Output Almost-Full Flag
OHF* 85 O Output Half-Full Flag
(RSTIN*) INT* 72 O Interrupt
(RSOUT) BICELL 71 I/O Cell Delineation
Control
(RTOUT)*SLAVE_OE 23 I/O Slave Output Enable
Cascade Select I 22 SLAVE* (RTIN*)
JTAG Test Clock I 43 JTCK
JTAG Test Mode I 46 JTMS
JTAG Test Data In I 44 JTDI
JTAG Test Reset I 47 JTRES*
JTAG
JTDO 45 O Test Data Out
I = Input, O = Output

Table 3-2. Hardware Signal Definitions—Microprocessor Control Mode (1 of 2)

	Pin Label	Signal Name	I/O	Definition
Microprocessor Interface	MODE	Control Mode	I	Must be set to a logic high to select microprocessor control mode.
	CS* (BIMODE)	Chip Select	I	Must be low to cause a read or write operation. CS* can not be high while AS* is high during multiple clock cycles unless bursting is desired. CS* must stay low during the access for proper operation, i.e., must not have decoding glitches.
	A[0] (S[0])	Address Bit 0	I	Address bit available in microprocessor control mode to select between types of access of the input/output buffer.
	A[1] (S[1])	Address Bit 1	I	Address bit available in microprocessor control mode to select between types of access of the input/output buffer.
	AS* (S[2])	Address Strobe	I	If low, a new address is loaded for the operation when AS* goes high. When it is high and CS* is low, a read or a write operation is executed. The address strobe can stay low for multiple clock periods. This allows for the insertion of wait states.
	OE* (BICON)	Output Enable	I	Must be low to enable the data output. The data is enabled between rising clock edges on a read cycle when this pin is low. For most applications this can be tied to ground.
	CLKB (WRB*)	Clock Input	I	Clock input to the microprocessor interface. All inputs are synchronous to the rising edge of this clock except OE*.
	W/R* (RDB*)	Write/Read	I	If low when chip select is low, the subsequent cycle is a read operation. If the operation is a read-and-modify, the register contents are latched during read operation. If this signal is high when chip select is low, the data presented at the end of the next clock cycle will be written if the chip select is still low at that time.
	INT* (RSTIN*)	Interrupt	O	An active low output with open drain.
Bidirectional Port	IEF*	Input Empty Flag	O	Provides an empty status for the input buffer.
	IAE*	Input Almost-Empty Flag	O	Provides an almost-empty status for the input buffer.
	OFF*	Output Full Flag	O	Provides a full status for the output buffer.
	OAF*	Output Almost-Full Flag	O	Provides an almost-full status for the output buffer.
	OHF*	Output Half-Full Flag	O	Provides a half-full status for the output buffer.
	BICELL (RSTOUT*)	Cell Delineation	I/O	Used in the cell mode. Should be tied to a pullup resistor to the supply voltage since it is a bidirectional open drain pin.
	BISTAT[3:0]	Bidirectional Status Word	I/O	Provides a status bit for each byte on BIDAT[31:0].
	BIDAT[31:0]	Bidirectional Data Word	I/O	The bidirectional 32-bit-wide data bus.

Table 3-2. Hardware Signal Definitions—Microprocessor Control Mode (2 of 2)

	Pin Label	Signal Name	I/O	Definition
Unidirectional Port	RCON	Read Control	I	Provides control of the unidirectional output port.
	RDEN*	Read Enable	I	An active-low input that enables reading of the unidirectional output port.
	RDU*	Read Strobe	I	Clocks the unidirectional output port.
	WRU*	Write Strobe	I	Clocks the unidirectional input port.
	WSTAT	Write Status	I	Provides control of the unidirectional input port.
	WREN*	Write Enable	I	An active-low input that enables writing of the unidirectional input port.
	WCON	Write Control	I	Provides control of the unidirectional input port.
	UINDAT[8:0]	Byte-Wide Input	I	The unidirectional byte-wide input data bus.
	IFF*	Input Full Flag	O	Provides a full status for the input buffer.
	IAF*	Input Almost-Full Flag	O	Provides an almost-full status for the input buffer.
	IHF*	Input Half-Full Flag	O	Provides a half-full status for the input buffer.
	OAE*	Output Almost-Empty Flag	O	Provides an almost-empty status for the output buffer.
	OEF*	Output Empty Flag	O	Provides an empty status for the output buffer.
	CELLOUT	Cell Output	O	Provides unidirectional output port cell delineation in cell modes. In TAXI mode, this pin is used as a TAXI interface transmit strobe.
	UOUTDAT[8:0]	Byte-Wide Output	O	The unidirectional byte-wide output data bus.
Control	SLAVE* (RTIN*)	Slave Select	I	Used in the 64-bit cell mode. For all other modes tie this input to the supply voltage. Master device is selected by pulling this pin high; slave device is selected by pulling it low.
	SLAVE_OE (RTOUT*)	Slave Output Enable	I/O	Provides unidirectional output port three-state synchronization between master and slave device.
JTAG	JTCK	JTAG Test Clock	I	The test clock input.
	JTMS	JTAG Test Mode	I	A serial command input that sets up various JTAG tests.
	JTDI	JTAG Test Data In	I	The JTAG serial data input.
	JTRES*	JTAG Test Reset	I	An active-low signal that asynchronously resets the JTAG test circuitry.
	JTDO	JTAG Test Data Out	O	The JTAG serial data output.
VCC and GND	VCC	Supply Voltage	--	Five pins are provided for power.
	GND	Ground	–	Six pins are provided for ground.

3.3 Smart FIFO Mode Operation

Table 3-3 is the smart FIFO mode (non-cell) address map of the microprocessor port (bits 21 and 22 of Control Register A both set to 0). Control Register A configures available options in the microprocessor control mode and the Status Register reports buffer status and parity. The *Read Buffer* and *Write Buffer* commands access the contents of the input and output buffers, respectively. One or more words can be written if the microprocessor interface is operating in burst mode. *The Write Last Word* command writes the 9th bit as a delineation bit so that the unidirectional interface can pad to a word boundary. The *Transfer Word* command writes a word from the input buffer to the output buffer. Detailed timing for the microprocessor interface is given in Section 5.1.

Table 3-3. Smart FIFO Mode Address Map

A[1] Pin 20	A[0] Pin19	Read Commands	Write Commands
0	0	Read Buffer	Write Buffer
0	1	Transfer Word	Write Last Word
1	0	Read Status	(Null Operation)
1	1	Read Control Register	Write Control Register

3.3.1 Bidirectional Port Control

Table 3-3 gives the address map for access to the bidirectional port. The microprocessor initialization procedure is as follows:

- Write Control Register A and Control Register B with the desired configuration and buffer resets active.
- Read Status Register A to release interrupts.

The *Read Buffer* command causes one word to be read from the input buffer and driven on the bidirectional bus. Multiple reads can occur if the microprocessor interface performs a burst operation. The *Write Buffer* command causes a word to be written to the output buffer. Again, multiple writes can occur if the microprocessor interface performs a burst operation. The IEF* and OFF* flags are the same as described in the subsection 2.3.2. The *Transfer Word* command transfers a word from the input buffer to the output buffer. Multiple word transfers can occur if a microprocessor burst cycle takes place.

The Bidirectional Status bits [BiStat[3:0]:SRA.21:24] can be read and written through the 32-bit interface; they correspond to the BISTAT[3:0] pins and the respective 9th bits of the input and output buffers. These status bits can be used for delineation purposes when the words are being padded. On the output buffer side, delineation is provided by the *Write Last Word* command. This command causes a pad field to be inserted and a delineation bit to be written to a logic zero.

The length of the pad field is determined by the Pad Bytes field [PadBytes[1,0]; CRA.4,5]. Pad Bytes = 0 causes no padding and Pad Bytes = 3 delineates for three pad bytes. The last active byte of a word is delineated with a logic zero in bit 9 of the byte. The BISTAT[3:0] pins must be a logic high when writing to the output buffer for the *Write Last Word* command to work properly. The first read of the status register after a read of the input buffer will report delineation on the BiStat[3:0] bits. A Bistat[3:0] bit will be a logic high if the corresponding BiStat[3:0] bit was a logic low during the previous read of the input buffer. Since the content of pad bytes is undefined, more than one delineation bit can occur in a word. The most significant delineation bit indicates the last active byte of a word.

3.3.2 Unidirectional Port Control

The Byte-Wide Function bits [ByteMode[2:0];CRA.2:0] select unidirectional port operation. The functions of these bits are given in Table 3-4. These bits functionally replace inputs S[0], S[1], and S[2] used in the stand-alone smart FIFO mode. The operation of each timing interface given in Table 3-4 is identical to that of the stand-alone smart FIFO mode. Status interrupts can be generated by the unidirectional ports in TAXI and HDLC modes.

Table 3-4. Microprocessor Unidirectional Port Selection

Function	ByteMode[2]	ByteMode[1]	ByteMode[0]
Asynchronous	0	0	0
Synchronous	0	0	1
HDLC	1	Enable FCS	1
TAXI	0	1	1
Cascade-Asynchronous	0	1	0
Cascade-Synchronous	1	1	0

In TAXI mode, if the WSTAT pin (violation) is a logic high and the WREN* pin (data strobe) is a logic low when the clock is going high on the rising edge of WRU* (receive clock), an interrupt is generated if TAXI Violation Interrupt Enable [EnTAXIViol;CRB.19] is enabled. WSTAT set to a logic high inhibits the writing of data to the input buffer.

For HDLC timing, *HDLC Abort*, *HDLC FCS* errors, and *HDLC External Abort* can be programmed to interrupt the microprocessor if a bad FCS or abort sequence error is written in the HDLC status byte at the end of a message or WREN* input goes high in the middle of a message (refer to Table 2-7).

3.3.3 Parity

On the input buffer side, parity can be applied to bit 9 or internally generated. The parity is checked and passed out in the BISTAT[3:0] pins of the bidirectional port. On the output buffer side, parity can be applied to the BISTAT[3:0] pins or generated internally, passed through the output buffer, and checked at the unidirectional output port. Parity is always checked. If an error occurs, Status Register A bits are latched until read. If the parity error interrupt is enabled, an interrupt occurs.

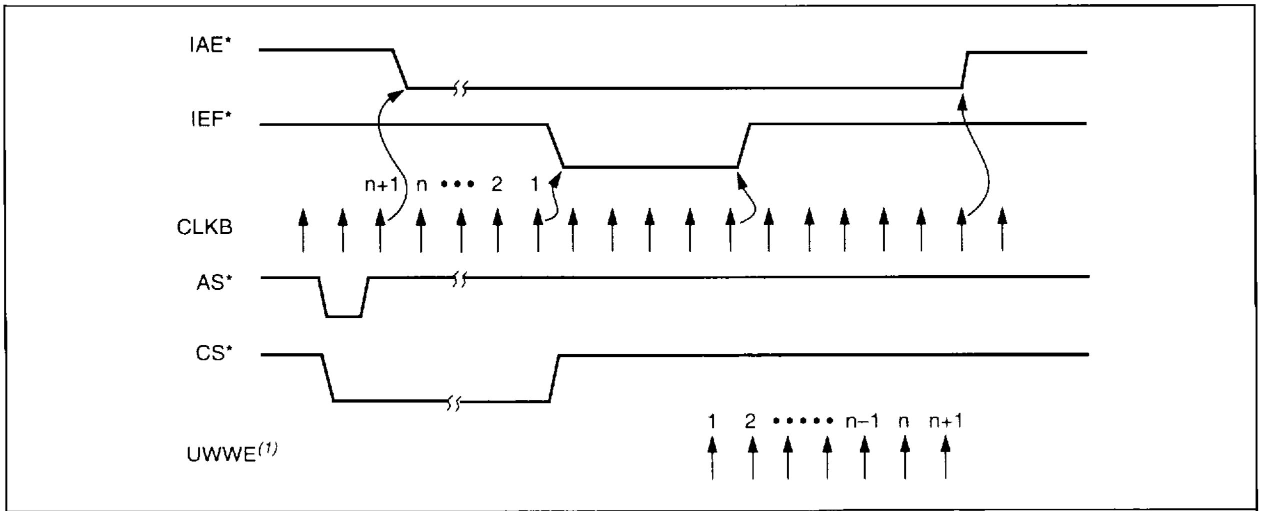
The interrupt clears when the status register is read. These checks occur even if bit 9 is not used for parity; in this case the status bits can be ignored and should not be enabled to cause interrupts. If Enable Input Parity Generation [EnInpParity; CRA.16] or Enable Output Parity Generation [EnOutParity; CRA.17] is set, then bit 9 of each byte is overwritten to a parity value calculated at that port input. Even or odd parity can be selected with the Select Even/Odd Parity [SelParity; CRA.18] control bit. A logic high selects even parity.

3.3.4 Buffer Flags

The full complement of flags is always present in Status Register A, bits 2 through 11. If the corresponding interrupt bit is not set, these bits will always reflect the current buffer status when read. If an interrupt is enabled, then an interrupt will occur whenever the appropriate flag changes state. The status bits will be latched until read. The almost empty/full flag offsets are common to bits 7 through 15 of Control Register A. The offset is binary encoded and has a range of 0 to 511.

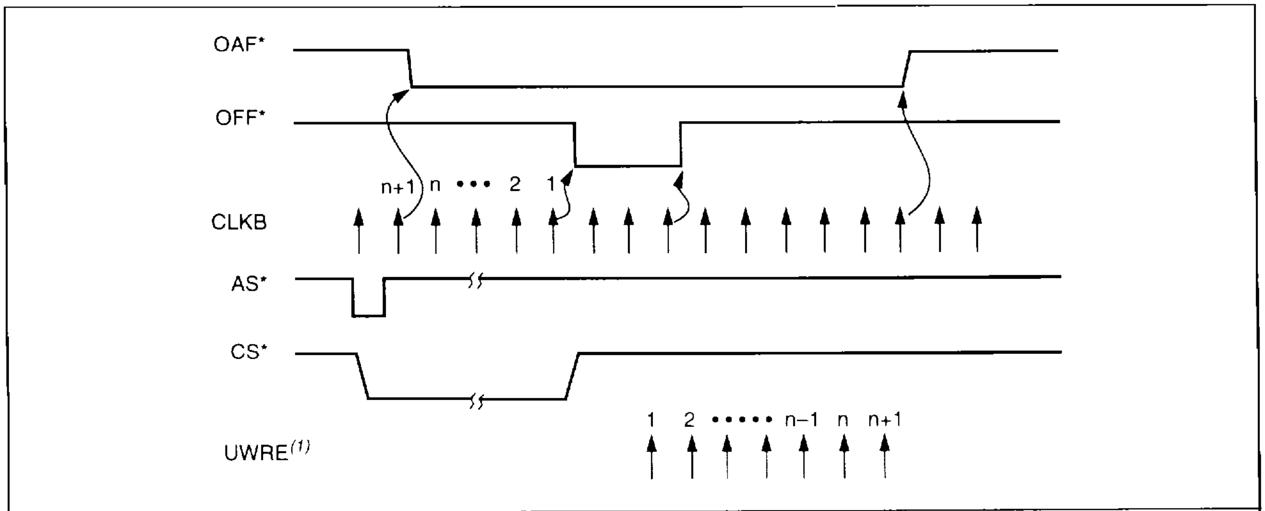
Figure 3-3, Figure 3-4, and Figure 3-5 show the operation of the bidirectional port flags. In all figures, n = offset value in the Control A Register. The unidirectional port flags are shown in Figures 2-28 through 2-33.

Figure 3-3. IAE Operation*



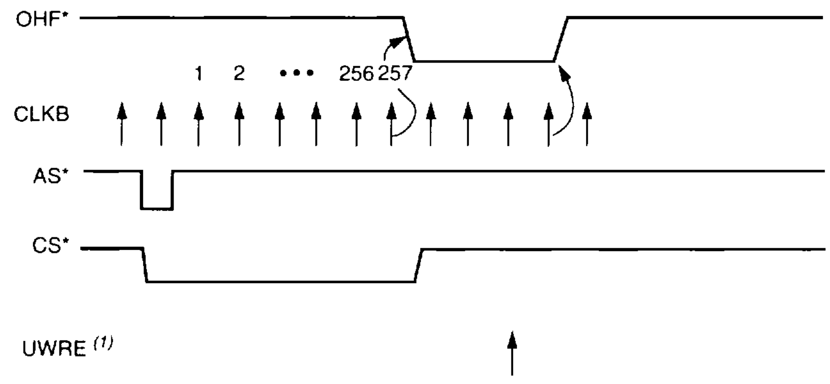
Notes: (1). Unidirectional Port Word Write Event.

Figure 3-4. OAF Operation*



Notes: (1). Unidirectional Port Word Read Event.

Figure 3-5. OHF Operation*



Notes: (1). Unidirectional Port Word Read Event.

3.4 32-Bit Fixed-Length Cell Processing

Broadcast, start-cell, and end-cell operations are all modes of the 32-bit cell processing operation. The address mapping for each of these modes is given in Table 3-1. Broadcast mapping can be used to implement a hub or switch. Start-cell or end-cell operation can be used to implement an endpoint station. The difference in these submodes is in the way that cell headers are processed.

Cell delineation for each submode is provided by an internal 37th bit of the buffer. The BiStat[3:0] bits are available for parity checking. Cell counters check the length of cells entering both input and output buffers when fixed-length cells are being processed. Synchronization circuitry at each buffer output will report an error if the delineation does not occur with the proper data and will realign to a cell boundary.

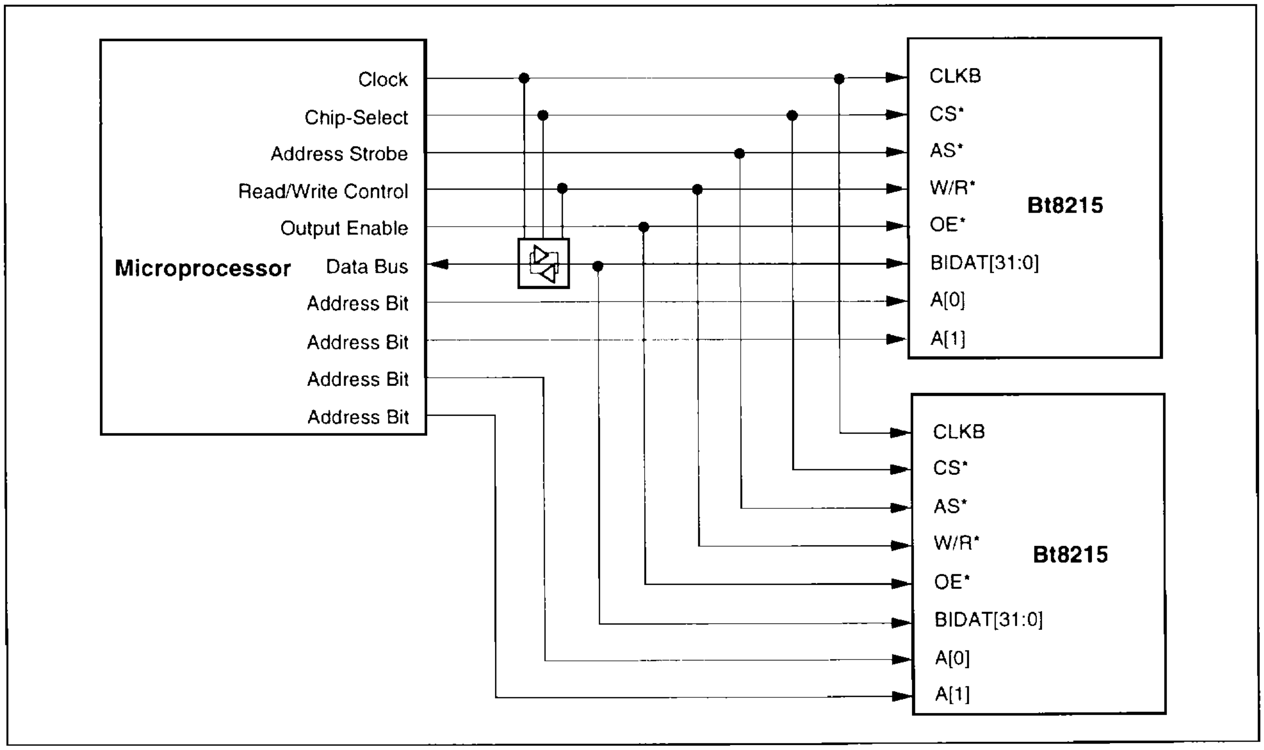
The operating modes for the microprocessor interface operate on fixed-length cells and allow the processing of these cells with one- and two-word headers. The cell length is defined by the Flag Offset [FlagOfst[8:0];CRA.15:7] and Pad Bytes [PadBytes[1,0];CRA.4,5] fields. An 11-bit counter is provided for the byte-wide input port. A 9-bit counter is provided for the bidirectional port to count the cell length. The cell size in bytes is four times the value of the FlagOfst[8:0] field plus the value of the PadBytes[1,0] field. The minimum cell size is 8 octets, the maximum is 2047 octets. The PadBytes[1,0] field does not reflect the number of pad bytes inserted into the last word, but rather indicates the number of active bytes present in the last word.

3.4.1 Bidirectional Port Operation

3.4.1.1 Broadcast Operation

Broadcast mapping (bits 21 and 22 of Control Register A set to 1 and 0, respectively) implements a broadcast algorithm. Each time a header is read by the microprocessor, the rest of the cell is autonomously read onto the output bus on the subsequent clock cycles and simultaneously transferred to the output buffers. If other bidirectional buffers are connected to this bus, they will be able to read the output data as well. This configuration is illustrated in Figure 3-6, where two Bt8215s are connected to a single microprocessor. The BICELL pins of the Bt8215s must be tied together with a pullup resistor.

Figure 3-6. Broadcast Application Connection



In this configuration, the microprocessor clock and control outputs are connected to every bidirectional port. The data is also bused. Each Bt8215 has individual address bit connections that allow different operations to be simultaneously performed on the devices connected to the microprocessor. The bidirectional transceiver isolates the bus from the microprocessor when the microprocessor has not selected any Bt8215 devices.

This broadcast operation reads a one- or two-word header from the source input buffer and then broadcasts the rest of the cell to all output buffers. After this transfer is complete, a header is written to the intended output buffer or buffers and the cell is deleted from all other output buffers. The address functions to accomplish this are given in Table 3-5

Table 3-5. Broadcast Operating Mode Address Map

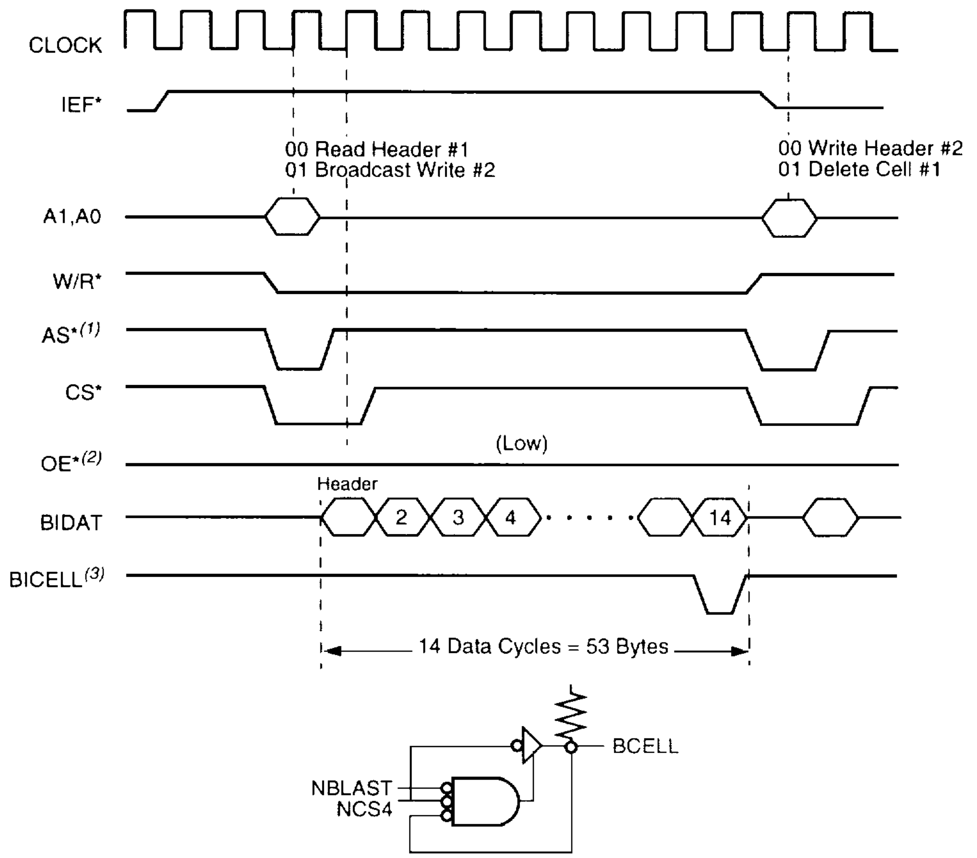
A[1] Pin 20	A[0] Pin 19	Read Commands	Write Commands
0	0	Read Header	Write Header
0	1	Broadcast Write	Delete Cell
1	0	Read Status	(Null Operation)
1	1	Read Control Register	Write Control Register

Cells are transferred from one input buffer to a selected group of output buffers in the following sequence (see Figure 3-7):

- At least one input buffer is detected that is not empty. This data is obtained from the IEF* or IAE* pins and indicates that a full cell is present in that input buffer. Upon reading the last cell in the input buffer, IEF* goes active only after the last word has been read, whereas IAE* goes active after approximately one-half of the cell has been read.
- A read operation is executed to all buffers. The address bus on the selected Bt8215 is set to 00 for a read cell operation. The address bus for each of the other Bt8215s is set to 01, initiating a cell transfer to each output buffer. This enables the entire cell to be copied to all output buffers. Note that this will occur even though the read operation takes but a single cycle.
- After the first word of the cell is read by the processor (En2WordHdr = 0), the transceiver isolates the bus for the rest of the cell-transfer clock cycles. This allows the processor to use its address and data bus to execute whatever program is necessary to determine which output buffers should retain the cell after it is transferred.
- After a new output header is calculated for the cell, a write header cycle is executed for each device that is to retain the transferred cell. For these devices the address bus is set to 00. The same operation can be a delete cell operation to output buffers that are not retaining the transferred cell; for this the address bus is set to 01. When multiple write header commands are required for different cells, the null operation can be used for unaffected buffers.

For the example shown in Figure 3-7, the FlagOffset = 0x0D (indicating 14 words, including Pad Bytes) and the PadBytes = 0x01 in Control Register A.

Figure 3-7. Broadcast Application Timing



Notes: (1). AS* input must be high during broadcast.
(2). OE* may be tied low unless default timing is not satisfactory.
(3). See bullet 4 of errata. Circuit used on evaluation board as shown above. Pullup resistor needed since open drain.

Synchronization between the input and output buffers is maintained by a delineation bit that is carried internally (37th bit). The read header operation will cause a read to the delineation bit that marks the end of the cell. A cell counter checks the number of bytes of data being broadcast and written to the output buffers. If the counter counts too many or too few octets being broadcast, the Input Cell Delineation Error [InputDelin;SRA.14] and Output Sync Error [OutputSync; SRA.12] status will be set and will cause an interrupt if so programmed. The output buffer pointer returns to the beginning of the cell. An output buffer may become full during the broadcast of a cell. In this case, the synchronization circuit will delete the partial cell even if a Write Header command is issued.

The empty and almost-empty flag information associated with writing the output buffer is updated after a valid complete cell is written to the output buffer. Either flag can, therefore, be used as a "cell present" indication. The almost-empty flag will transition active in the middle of the cell whereas the empty flag will transition at the end of the cell.

If Enable Two-Word Header [En2WordHdr;CRA.24] is set, then two read header operations are required. The buffer whose header is not being read must be addressed with broadcast write for two operations. Similarly, after the cell transfer, the write header address is written twice to the desired buffer(s) and the delete cell address is used for cells elsewhere.

The controller can determine that the cell transfer is complete in two ways. The Transfer Complete Interrupt Enable [EnXfrComplete;CRB.16] can be set, in which case the input buffer that is transmitting will interrupt when the message is done. Additionally, a logic low at the cell delineation bit on the BICELL pin indicates the last word of the cell is being read.

3.4.1.2 Start-Cell Operation

Start-cell operation provides a single point cell transfer operation between the Bt8215 and a bus controller. The address map for start-cell (and for End-Cell operation) is shown in Table 3-6. The cell header is written at the beginning of the cell. A cell delineation bit (37th bit) is created by the *Write Last Word* command.

Table 3-6. Start-Cell and End-Cell Operating Modes Address Map

A[1] Pin 20	A[0] Pin 19	Read Commands	Write Commands
0	0	Read Buffer	Write Buffer
0	1	Transfer Word	Write Last Word
1	0	Read Status	Null Operation
1	1	Read Control Register	Write Control Register

Each *Read Buffer* operation reads one word from the input buffer. If a cell delineation bit is read, marking the end of the cell, the Transfer Complete (XfrComplete;SRA.16) status bit will be set and, if enabled, an interrupt will occur. No further reads of the buffer will be allowed until the status register is read. If further *Read Buffer* commands occur before the status is read, the Input Cell Delineation Error bit [InputDelin;SRA.14] will be set and, if enabled, an interrupt will occur. Normal operation requires that there be a sufficient number of *Read Buffe*r commands to read a whole cell from the buffer followed by a *Read Status* command. If the read of the status detects a cell alignment error, Transfer Complete status bit is logic low or Input Cell Delineation Error is logic high, the host should discard the last cell read. If the read of the status detects that the Transfer Complete status bit is logic low, *Read Buffer* followed by *Read Status* commands could be executed until the Transfer Complete status bit is read logic high. This realigns the reading of the buffer to a cell boundary. If this active realignment is not desired, the next cell will also be in error but cell synchronization will be acquired after the second cell.

A "cell present" indication is obtained from either the IEF* or the IAE* pin. This indication means that a full cell is present in that input buffer. On a read of the last cell in the input buffer, IEF* goes active only after the last word has been read. On the other hand, IAE* activates after approximately half of the cell has been read.

Writing of cells is accomplished by the *Write Buffer* and *Write Last Word* commands. The functions of the two are identical except that the *Write Last Word* address will set the Input Cell Delineation Error bit to a logic low. Output buffer cell synchronization is maintained by a cell counter. If the counter detects too many or too few octets between *Write Last Word* commands, the Output Sync Error [OutputSync;SRA.12] status bit will be set and if enabled, an interrupt occurs and the output buffer returns to the beginning of the cell.

Data can be transferred from the input buffer to the output buffer by the *Transfer Word* command. If the last word of a cell is to be transferred, then the delineation bit from the input buffer will take the place of the Write Last Word command. The status register must be read after the whole cell is transferred to release the input buffer for further reads. Data can be read or written on consecutive clock cycles by using a microprocessor burst write operation.

The empty and almost-empty flag information associated with writing the output buffer is updated after a valid complete cell is written to the output buffer. Either flag can be used as a "cell present" indication. The almost-empty flag will transition active in the middle of the cell whereas the empty flag will transition at the end of the cell. For modulo 4 cell lengths, OAF* can be used to determine if a new cell will fit into the output buffer before the cell is transferred. For other cell lengths, OAF* need to be monitored during the cell transfer.

3.4.1.3 End-Cell Operation

End-cell operation provides a single-point cell transfer operation between the Bt8215 and a bus controller. The header is written after all of the other cell data but is written to the physical beginning of the cell. The address map for this mode is given in Table 3-6.

Reading of cells is the same as for start-cell operation. When writing cells, the cell data is written before the header, with the *Write Last Word* operation corresponding to the last word of the cell. The header word or words are then written.

One or two extra *Write Buffer* commands (depending upon the setting of the Enable Two-word Header bit [En2WordHeader;CRA.24]) must be issued at the beginning of each cell to reserve a buffer location for the header word or words. No data is transferred with these commands.

The empty flag information associated with writing the output buffer is updated after a valid complete cell is written to the output buffer. The empty flag can, therefore, be used as a "cell present" indication. If the buffer becomes full as a cell is written, the buffer returns to the beginning of the cell and further writing is prohibited until after a *Write Last Word* command. For modulo 4 cell lengths, OAF* can be used to determine if a new cell will fit into the output buffer before the cell is transferred. For other cell lengths, OAF* will need to be monitored during the cell transfer.

3.4.2 Unidirectional Port Operation

Unidirectional port operation selections are asynchronous, synchronous, and TAXI. They are identical in function to the stand-alone smart FIFO mode except for the cell delineation and synchronization control and status. In addition, two Bt8215s can be connected back-to-back to allow the interconnection of cell-processing buffers. In this configuration one of the Bt8215s is synchronous and one is configured as synchronous cascade.

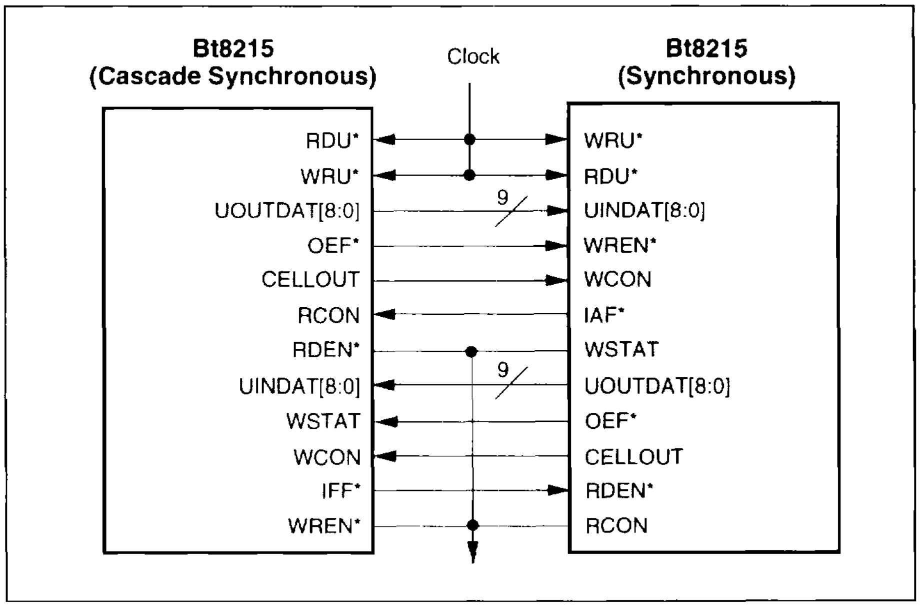
3.4.2.1 Asynchronous, Synchronous, and TAXI Operations

In the asynchronous, synchronous, and TAXI operations, the delineation signal is provided on the RCON and WCON input pins. These synchronization signals are active low. WCON must be present if the Disable Cell Counter bit [DisCellCtr;CRA.26] is a logic low. WCON and RCON may be tied to ground if not used. The WSTAT input provides the input buffer valid cell function for all three modes and is active low. An entire cell will be deleted if WSTAT is a logic high (indicating an invalid cell) and remains high through the last octet of the cell. For operation of WSTAT in the SMDS Header Mode, see subsection 3.4.2.3. If the HDLC FCS/TAXI Violation Interrupt Enable bit (EnTaxiViol;CRB.19) is set, an interrupt will occur when an invalid cell is received. In addition, a logic low on CELLOUT indicates the last octet of the cell.

3.4.2.2 Back-to-Back Operation

Back-to-back operation allows for autonomous transfer of data between Bt8215 devices through the unidirectional port, and can be used to cascade or interconnect broadcasting elements. Transfers occur whenever there is data in the output buffer and the destination buffer is not full. Back-to-back is configured by setting one Bt8215 to synchronous cascade and the other device to synchronous. Figure 3-8 illustrates this connection.

Figure 3-8. Back-to-Back Connection



3.4.2.3 SMDS Header Operation

The Enable SMDS Header [EnSmdsHdr;CRA.23] bit enables an octet repositioning algorithm for use with SMDS, IEEE 802.6, or ATM AAL3/4 cells. In these cell formats, the first 2 bytes of each cell represent a header and the last 2 bytes are a trailer, both with control and status information. In IEEE 802.6, the SMDS header and trailer are written into word 1. In ATM AAL3/4, the SMDS header and trailer are written into word 2; in this case, word 1 is the ATM header. The Enable SMDS Header control bit combines the header and the trailer in the second word of the cell and word-aligns the remaining information. The header realignment for n octet length cells is illustrated in Table 3-7 and Table 3-8.

Table 3-7. SMDS One-Word Header Map

Word 1	Byte 1	Byte 2	Byte n–1	Byte n
Word 2	Byte 3	Byte 4	Byte 5	Byte 6
:	:	:	:	:
Last Word	Byte n–5	Byte n–4	Byte n–3	Byte n–2

Table 3-8. SMDS Two-Word Header Map

Word 1	Byte 1	Byte 2	Byte 3	Byte 4
Word 2	Byte 5	Byte 6	Byte n–1	Byte n
Word 3	Byte 7	Byte 8	Byte 9	Byte 10
:	:	:	:	:
Last Word	Byte n–5	Byte n–4	Byte n–3	Byte n–2

Octet repositioning occurs on both the input and output buffers. This mode works only for modulo 4 octet cell lengths. Back-to-back operation does not work with SMDS header mode. If back-to-back operation is desired in a SMDS header switch, the data is transferred between the buffers with the octets repositioned; therefore, the Enable SMDS Header bit is not set in the back-to-back Bt8215 devices. WSTAT may go active during the second octet in the one-word mode and during the sixth octet in the two-word mode. Also note that 2 octets may be read from the output buffer after the OEF* flag goes active.

3.4.2.4 Cell Synchronization

The unidirectional port must be provided with a synchronization signal on the WCON input that marks the last octet of the cell. The cell counter checks that the proper number of octets are written between active synchronization pulses. If the counter check is valid, then the sync pulse will cause a cell delineation bit to be written and an end-of-write operation to pad out the word, if necessary. The location of the first word of the cell is stored in a register. If a synchronization signal occurs before the terminal count of the cell counter or the terminal count occurs before the sync, the buffer will back up to the beginning of the cell and inhibit writing of the buffer until after the next synchronization indication. If the Input Sync Interrupt Enable bit [EnInputSync;CRB.13] is set, the buffer will interrupt the microprocessor on an error. Only one error will be reported per synchronization failure.

The empty and almost empty flag information associated with writing the input buffer is updated after a valid complete cell is written to the input buffer. The empty flag can, therefore, be used as a "cell present" indication. If the buffer becomes full as a cell is written, the buffer backs up to the beginning of the cell and further writing is prohibited until after the next sync signal. The offset of the almost empty flag (IAE*) is set to the offset flag divided by 2 (binary right-shift).

The synchronization signal to the unidirectional output port is optional. This signal marks the last octet of the cell, and can be used to obtain cell alignment. The signal input is applied to the RCON pin; if not provided, this pin should be connected to ground.

The synchronization signal is sampled when the delineation bit is read and the byte read corresponds to the last octet of the cell as defined by the PadBytes[1,0] field in Control Register A. If the synchronization input is high when the delineation bit occurs, further reading is inhibited. If the Output Cell Delineation Interrupt Enable bit [EnOutputDelin;CRB.15] is set, an error interrupt is sent. When the synchronization bit is detected at a logic low, the read hold is released and the next 4 bytes read will be a header. The delineation bit acts as an end read command along with the PadBytes[1,0] field, providing the proper padding function.

3.5 Variable-Length Cells Processing

Variable-length cells can be accommodated by setting the Parity Inversion[Parity-Invert;CRA.25], Disable Cell Counters [DisCellCtr;CRA.26] and Enable Input Parity Generation [EnInputParity;CRA.16] bits. The first control bit will invert the polarity of the parity bit on the last octet of the cell when it is written to the input buffer. The microprocessor can then detect the parity inversion when it reads the input buffer. When the microprocessor writes the output buffer, it has to write the proper parity inversion. The *Write Last Word* command must be used to write the last word of a cell. The output buffer will then detect the parity inversion and terminate the cell. A logic low on CELLOUT indicates the last octet of the cell. Correct parity will be generated for the last octet. The second control bit turns off the cell counters on the write ports and disables the read port checks. Input buffer read checks are still performed in the start-cell and end-cell operations. A read of the status register must still be performed after reading a cell from the input buffer.

3.5.1 Bidirectional Port Operation

Bidirectional port operation is similar to the fixed-length cell mode. The broadcast, start-cell and end-cell modes of bidirectional port operation are supported. Differences are in parity and synchronization operation. Correct parity must be supplied on the BISTAT[3:0] pins when writing a word to the output buffer. This includes parity inversion of the last byte of the cell. The output sync error is disabled in all three modes and the input cell delineation error is disabled in the broadcast mode of operation.

3.5.2 Unidirectional Port Operation

In this mode, the unidirectional port supports the asynchronous, synchronous, and TAXI interfaces. Port operation is similar to the fixed-length cell mode. Bit 9 of each byte is reserved for parity. On the input buffer side, parity must either be supplied externally or generated internally. On the output buffer side, correct parity is always present on UOUTDAT[8]. The input sync error is disabled in all three modes.

3.6 64-Bit Cell Processing

The 64-bit cell processing operation uses two Bt8215 parts in a master-slave configuration to obtain a 64-bit bidirectional bus. This operation is controlled by bits 27 and 28 in Control Register A as shown in Table 3-9 and by tying the RTIN/SLAVE* (pin 22) input pin to the supply voltage for the master device and to ground for the slave device. The unidirectional ports are internally controlled to maintain a 9-bit unidirectional interface. The control interface of both ports is the same as the 32-bit mode. Cross-synchronization circuitry between the master and slave parts ensure buffer cell synchronization. Data is written to the input buffers as follows: The 4 header bytes of the cell are written to both input buffers. Bytes are then written alternately between the devices. If the cell has an odd number of bytes, the last byte is written to both master and slave devices. Each device stores the same number of octets per cell. The FlagOfst[8:0] and PadBytes[1,0] fields of Control Register A are set according to the following equations:

Odd Octets per Cell: (4* Flag Offset) + Pad Bytes = (((# octets/cell) –5)/2) +5)

Even Octets per Cell: (4* Flag Offset) + Pad Bytes = (((# octets/cell) –4/2) + 4)

Table 3-9. 64-Bit Mode Selection

En64Bit[1] CRA.28	En64Bit[0] CRA.27	Function
0	0	Mode 64 Off
1	0	Even Number of Octets per Cell
0	1	Odd Number Of Octets per Cell
1	1	64-Bit Back-to-Back

3.6.1 Bidirectional Port Operation

Bidirectional port operation works in the same manner as the 32-bit mode except that the first 64-bit word read contains a redundant 32-bit header. Data is read from the output buffers as follows: The 4 header bytes are read from both devices but only the master device drives the unidirectional output data bus. Bytes are then read alternately from the devices. If the cell length is odd, the last byte of the cell is read from both devices, but the master device drives the bus.

The microprocessor signals CLKB, CS*, AS*, W/R*, OE*, A[0], and A[1] are common to both the master and slave devices. The BICELL bidirectional pin must be connected to all other BICELL pins, both master and slave, and connected to an external pullup resistor. The OHF*, IHF*, IAF*, and OAF* signals on the master device must be tied to the same pin on the slave device to enable the cross-synchronization circuitry.

Each Bt8215 pair receives the same commands from the microprocessor. When writing the header to the output buffers, the header must be written to the master device. Any header value can be written to the slave device. This mode does not support the enable two-word header operation. The master and slave IEF* and IAE* flags should be logical ANDed for proper input buffer "cell present" indication.

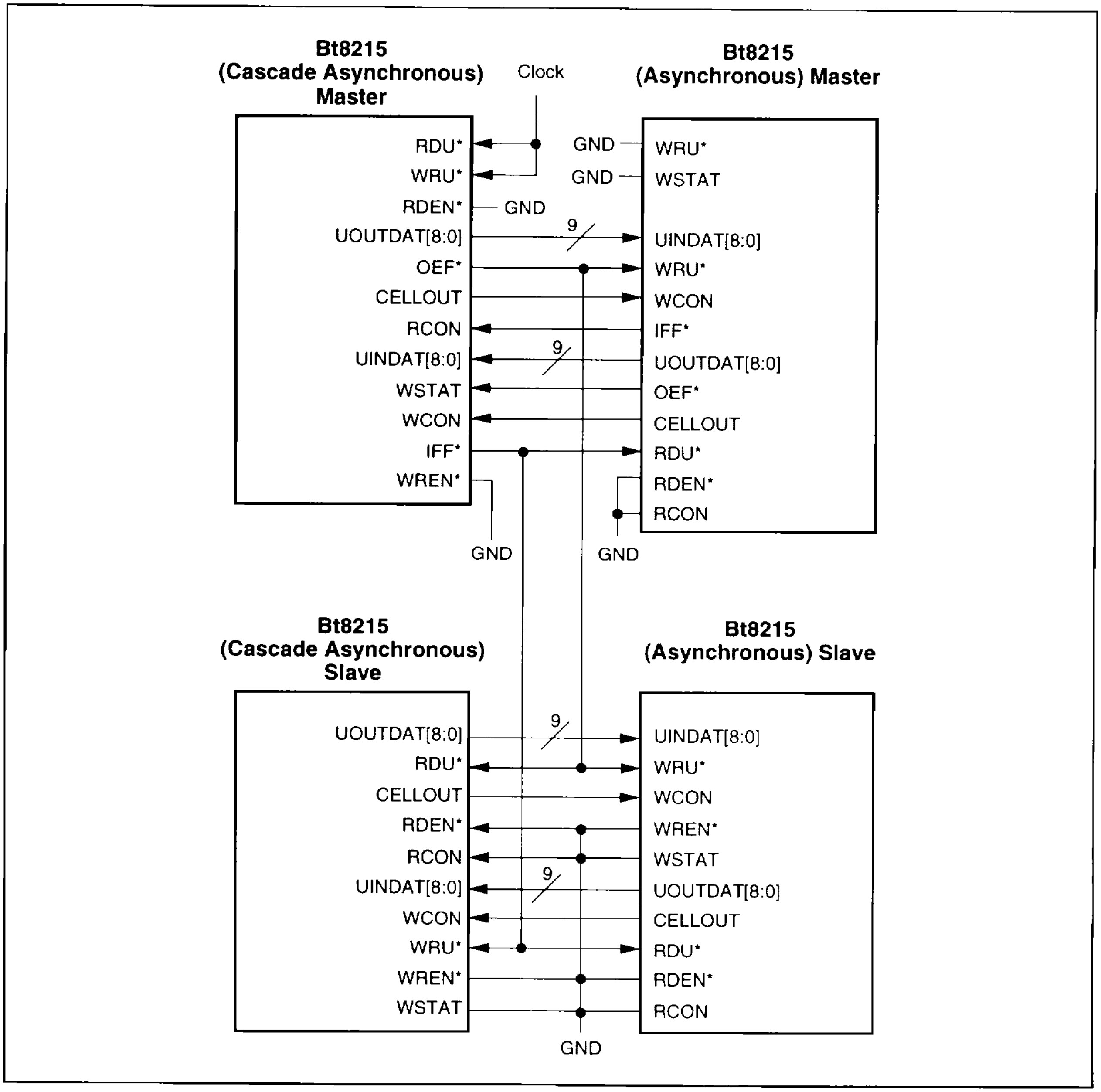
3.6.2 Unidirectional Port Operation

Unidirectional port operation supports the asynchronous and synchronous unidirectional port configurations. SMDS header operation is not supported in this mode. The WCON, WREN*, WSTAT, WRU*, RCON, RDEN*, RDU, and UINDAT[8:0] inputs are tied together and connected to the external unidirectional device in the same manner as the 32-bit mode. The UOUTDAT[8:0] outputs are tied together to form a 9-bit bus. The RTOUT* pins of the master and slave devices must be tied together. This allows the master device to control the UOUTDAT[8:0] bus of both the master and slave devices. The master and slave OEF* and OAE* flags should be logical ANDED for proper output buffer "cell present" indication.

3.6.2.1 Back-to-Back Operation

Figure 3-9 shows the back-to-back operation of the unidirectional port in 64-bit cell processing operation. Besides the connections shown, the RTOUT* pin of the master device must be tied to the RTOUT* pin of the slave device. To select a different unidirectional interface for the master and slave devices, separate address lines for the devices are required.

Figure 3-9. 64-Bit Mode Back-to-Back Connection



4.0 Registers

4.1 Register Overview

The Bt8215 contains two control registers and one status register as shown in Table 4-1. The two control registers occupy the same address but are accessed alternately.

Table 4-1. Bt8215 Registers

	Address	Label	Read/Write	Size (Bits)
Control Registers	0x00	CRA	R/W	32
	0x00	CRB	R/W	32
Status Register	0x10	SRA	R	32

4.2 Control Registers

Control Registers A and B are two 32-bit paged registers that share the same address. Access is controlled by a page bit in the registers. These registers are written on the clock cycle after the write operation is executed. This allows the device to decode the page identifier bit and write to the appropriate register. Reading of the control registers is performed in sequence. The last register that was written is read first; on subsequent read operations the registers are read alternately. The microprocessor can determine which register is being read by the value of the page identifier bit when read. A logic low on Page Identifier [PageID;CRA.31] will write to Control Register A and a logic high will write to Control Register B.

Parity will always be present on the BISTAT[3:0] pins when either Control Register A or B is read. The polarity of the parity is determined by Select Even/Odd Parity [SelParity;CRA.18].

4.2.1 0x00—Control Register A (CRA)

Bit	Field Size	Name	Description
31	1	PageID	Page Identification—Controls which register is to be written by the microprocessor. A logic low writes to Control Register A.
30	1	EnStatusRead	Enable Status Read—Enables a Read Status command to drive the value in the status register onto the BIDAT[31:0] bus.
29	1	ReTxInput	Retransmit In—Causes the read pointer of the input buffer to be reset to the physical beginning of the input buffer. This bit is unlatched, read as zero, and does not operate in the cell modes.
28, 27	2	En64Bit[1,0]	Enable 64-Bit Mode—Cell-based control that enables 64-bit operation in the bidirectional port interface. See Table 3-9.
26	1	DisCellCtr	Disable Cell Counter—Cell-based control that disables the cell counters and the read port checks.
25	1	ParityInvert	Parity Inversion Cell Delineation—Cell-based control that inverts the polarity of the parity bit on the last octet of a cell.
24	1	En2WordHdr	Enable Two-Word Header—Cell-based control that allows the processing of fixed-length cells with a two-word header.
23	1	EnSmdsHdr	Enable SMDS Header—Cell-based control that enables an octet repositioning algorithm for use in SMDS cells.
22, 21	2	AddrMap[1,0]	Address Map—Selects the bidirectional port address map (see Table 3-1).
20	1	RstOutput	Reset Output Buffer—Unlatched, reads as zero, and resets the output buffer.
19	1	RstInput	Reset Input Buffer—Unlatched, reads as zero, and resets the input buffer.
18	1	SelParity	Select Even/Odd Parity—Sets the polarity of parity generation and checking. If the bit is set to 1, parity is even.
17	1	EnOutParity	Enable Output Parity Generation—Generates parity to be carried through the output buffer.
16	1	EnInpParity	Enable Input Parity Generation—Generates parity to be carried through the input buffer.
15–7	8	FlagOfst [8:0]	Flag Offset—In stand-alone smart FIFO mode, this bit sets the offset value of all the "almost empty" and "almost full" flags. In the cell processing mode, this value multiplied by 4 indicates the cell size.
6	1	ReTxOutput	Retransmit Out—Causes the read pointer of the output buffer to be reset to the physical beginning of the output buffer. This bit is unlatched, read as 0, and does not operate in the cell modes.
5,4	2	PadBytes[1,0]	Pad Bytes—Selects the number of pad bytes inserted during a Write Last Word operation. In cell processing mode, this bit indicates the number of active bytes in the last word.
3	1	Rsvd	Reserved—Set to zero.
2–0	3	ByteMode[2:0]	Byte-Wide Function—Selects the unidirectional port functions (same as S[2:0] in stand-alone smart FIFO mode). Refer to Table 3-4.

4.2.2 0x00—Control Register B (CRB)

Bit	Field Size	Name	Description
31	1	EnPageID	Page Identification Interrupt Enable—Controls which register is to be written by the microprocessor. A logic high will write to Control Register B.
30–22	9	Rsvd	Reserved—Set to zero.
21	1	EnDelineation	Delineation Interrupt Enable—Causes an interrupt if one of the input buffer bidirectional status bits is a logic low when read.
20	1	EnHdlcExtAbort	HDLC External Abort Interrupt Enable—Reports error conditions in the HDLC receive status byte.
19	1	EnTaxiViol	HDLC FCS/TAXI Violation Interrupt Enable—Occurs if there is a code violation in TAXI.
18	1	EnHdlcAbort	HDLC Abort Interrupt Enable—Reports error conditions in the HDLC receive status byte.
17	1	RSVD	Reserved—Set to zero.
16	1	EnXfrComplete	Transfer Complete Interrupt Enable—Used in the cell mode. This bit indicates that the transfer of an entire cell has been completed.
15	1	EnOutputDelin	Output Cell Delineation Interrupt Enable—Used in the cell mode. This bit is used to maintain synchronization between the input and output buffers.
14	1	EnInputDelin	Input Cell Delineation Interrupt Enable—Used in the cell mode. This bit is used to maintain synchronization between the input and output buffers by marking the end of the cell.
13	1	EnInputSync	Input Sync Interrupt Enable—Used in the cell mode. This bit indicates that the cell counter has detected that either too many or too few octets have been written to the input buffer.
12	1	EnOutputSync	Output Sync Interrupt Enable—Used in the cell mode. This bit indicates the counter has detected that either too many or too few octets have been written in the output buffer.
11	1	EnOFF	Output Full Flag Interrupt Enable—Causes an interrupt if the Output Full Flag (OFF*) changes state.
10	1	EnOAF	Output Almost-Full Flag Interrupt Enable—Causes an interrupt if the Output Almost-Full Flag (OAF*) changes state.
9	1	EnOHF	Output Half-Full Flag Interrupt Enable—Causes an interrupt if the Output Half-Full Flag (OHF*) changes state.
8	1	EnOAE	Output Almost-Empty Flag Interrupt Enable—Causes an interrupt if the Output Almost-Empty Flag (OAE*) changes state.
7	1	EnOEF	Output Empty Flag Interrupt Enable—Causes an interrupt if the Output Empty Flag (OEF*) changes state.
6	1	EnIFF	Input Full Flag Interrupt Enable—Causes an interrupt if the Input Full Flag (IFF*) changes state.

Bit	Field Size	Name	Description
5	1	EnIAF	Input Almost-Full Flag Interrupt Enable—Causes an interrupt if the Input Almost-Full Flag (IAF*) changes state.
4	1	EnIHF	Input Half-Full Flag Interrupt Enable—Causes an interrupt if the Input Half-Full Flag (IHF*) changes state.
3	1	EnIAE	Input Almost-Empty Flag Interrupt Enable—Causes an interrupt if the Input Almost -Empty Flag (IAE*) changes state.
2	1	EnIEF	Input Empty Flag Interrupt Enable—Causes an interrupt if the Input Empty Flag (IEF*) changes state.
1	1	EnOuputParity	Output Parity Error Interrupt Enable—Allows a parity error at the byte-wide output port to cause an interrupt.
0	1	EnInputParity	Input Parity Error Interrupt Enable—Allows a parity error at the byte-wide input port to cause an interrupt.

4.3 Status Register

4.3.1 0x10—Status Register A (SRA)

Status Register A reports the status of the buffer and parity check operation. It is latched during a read to prevent changing data. All reserved bits are read as zero.

If any bits in Control Register B are set, the corresponding status bit will cause an interrupt. There are two types of interrupts: error and flag. Error interrupts occur on each occurrence of the error condition. Errors are latched until read and then cleared when read. Flag interrupts occur on changes of state. An interrupt will latch the value of the flag. Upon reading, the latch will be released; a subsequent read will indicate the current state of the flag. Bits 2 through 11 are flag interrupts. All others are error interrupts. The interrupt is level-generated, and remains present until the status register is read. This ensures that no interrupts will be missed. A read of the status register clears the interrupt; however, no interrupts are missed due to read operations.

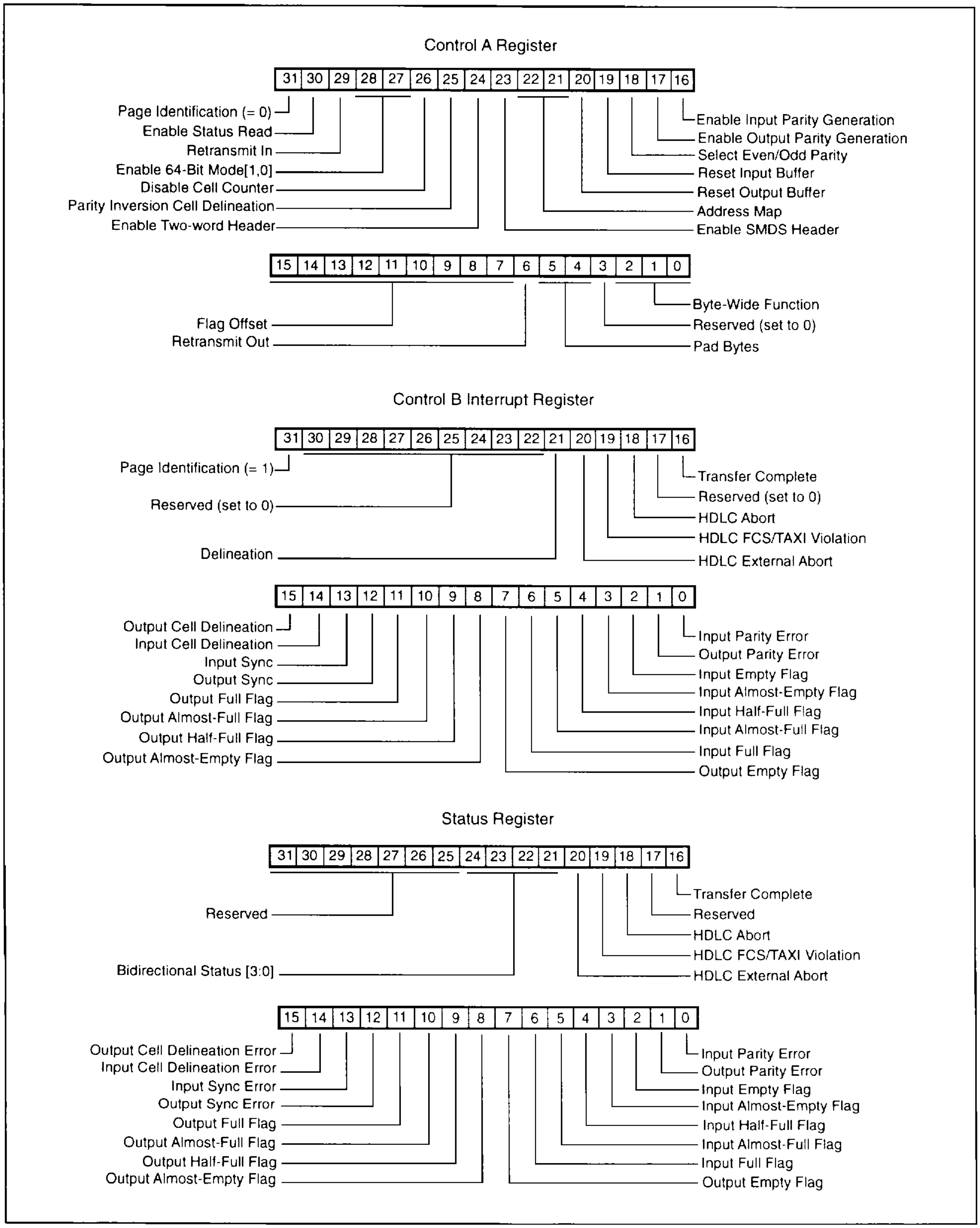
Parity is always be present on the BISTAT[3:0] pins when the control or status registers are read. The polarity of the parity is determined by the Select Even/Odd Parity bit [SelParity;CRA.18].

Bit	Field Size	Name	Description
31–25	7	Rsvd	Reserved—Set to zero.
24–21	4	BiStat[3:0]	Bidirectional Status—Corresponds to the BISTAT[3:0] pins and the respective 9th bits of the input and output buffers.
20	1	HdlcExtAbort	HDLC External Abort Interrupt—Reports error conditions in the HDLC receive status byte.
19	1	TaxiViol	HDLC FCS/TAXI Violation Interrupt—Occurs if there is a code violation in TAXI mode. Also serves as an invalid cell indication in the HDLC mode.
18	1	HdlcAbort	HDLC Abort Interrupt—Reports error conditions in the HDLC receive status byte.
17	1	RSVD	Reserved—Set to zero.
16	1	XfrComplete	Transfer Complete—Used in the cell mode. Indicates that the transfer of an entire cell has been completed
15	1	OutputDelin	Output Cell Delineation Error—Used in the cell mode. Maintains synchronization between the input and output buffers,
14	1	InputDelin	Input Cell Delineation Error—Used in the cell mode. Maintains synchronization between the input and output buffers by marking the end of the cell.
13	1	InputSync	Input Sync Error—Used in the cell mode. Indicates that the cell counter has detected that either too many or too few octets have been written to the input buffer.
12	1	OutputSync	Output Sync Error—Used in the cell mode. Indicates that the cell counter has detected that either too many or too few octets have been written to the output buffer.
11	1	OFF	Output Full Flag—Indicates an interrupt if the Output Full Flag (OFF*) changes state.

Bit	Field Size	Name	Description
10	1	OAF	Output Almost-Full Flag—Indicates an interrupt if the Output Almost-Full Flag (OAF*) changes state.
9	1	OHF	Output Half-Full Flag—Indicates an interrupt if the Output Half-Full Flag (OHF*) changes state.
8	1	OAE	Output Almost-Empty Flag—Indicates an interrupt if the Output Almost-Empty Flag (OAE*) changes state.
7	1	OEF	Output Empty Flag—Indicates an interrupt if the Output Empty Flag (OEF*) changes state.
6	1	IFF	Input Full Flag—Indicates an interrupt if the Input Full Flag (IFF*) changes state.
5	1	IAF	Input Almost-Full Flag—Indicates an interrupt if the Input Almost-Full Flag (IAF*) changes state.
4	1	IHF	Input Half-Full Flag—Indicates an interrupt if the Input Half-Full Flag (IHF*) changes state.
3	1	IAE	Input Almost-Empty Flag—Indicates an interrupt if the Input Almost-Empty Flag (IAE*) changes state.
2	1	IEF	Input Empty Flag—Indicates an interrupt if the Input Empty Flag (IEF*) changes state.
1	1	OutputParity	Output Parity Error—Indicates a parity error at the byte-wide output port to cause an interrupt.
0	1	InputParity	Input Parity Error—Indicates a parity error at the byte-wide input port to cause an interrupt.

4.4 Register Summary

Figure 4-1. Bt8215 Register Summary



5.0 Electrical and Mechanical Specifications

5.1 AC Characteristics

Table 5-1 and Figure 5-1 show the timing requirements for a microprocessor interface burst write cycle.

Table 5-1. Microprocessor Burst Write Timing

Parameter	Description	Min	Typ	Max
t_{as}	Address Setup Time to CLKB	1.5		
t_{ah}	Address Hold Time from CLKB	1.0		
t_{wrs}	W/R* Setup Time to CLKB	1.0		
t_{wrh}	W/R* Hold Time from CLKB	1.5		
t_{ass}	Address Strobe Setup Time to CLKB	7.0		
t_{ash}	Address Strobe Hold Time from CLKB	1.5		
t_{css}	Chip Select Setup Time to CLKB	7.0		
t_{csh}	Chip Select Hold Time from CLKB	1.0		
t_{ds}	Bidirectional Data Setup Time to CLKB	8.0		
t_{dh}	Bidirectional Data Hold Time from CLKB	2.0		
t_{ps}	Data Setup Time to CLKB with Internal Parity Generator Enabled	11.0		
t_{ss}	BISTAT[3:0] Setup Time to CLKB	9.5		
t_{cyc}	Minimum Clock Period	30		
t_{ch}	CLKB High Pulse Width	12		
t_{cl}	CLKB Low Pulse Width	12		

Figure 5-1. Microprocessor Burst Write Cycle

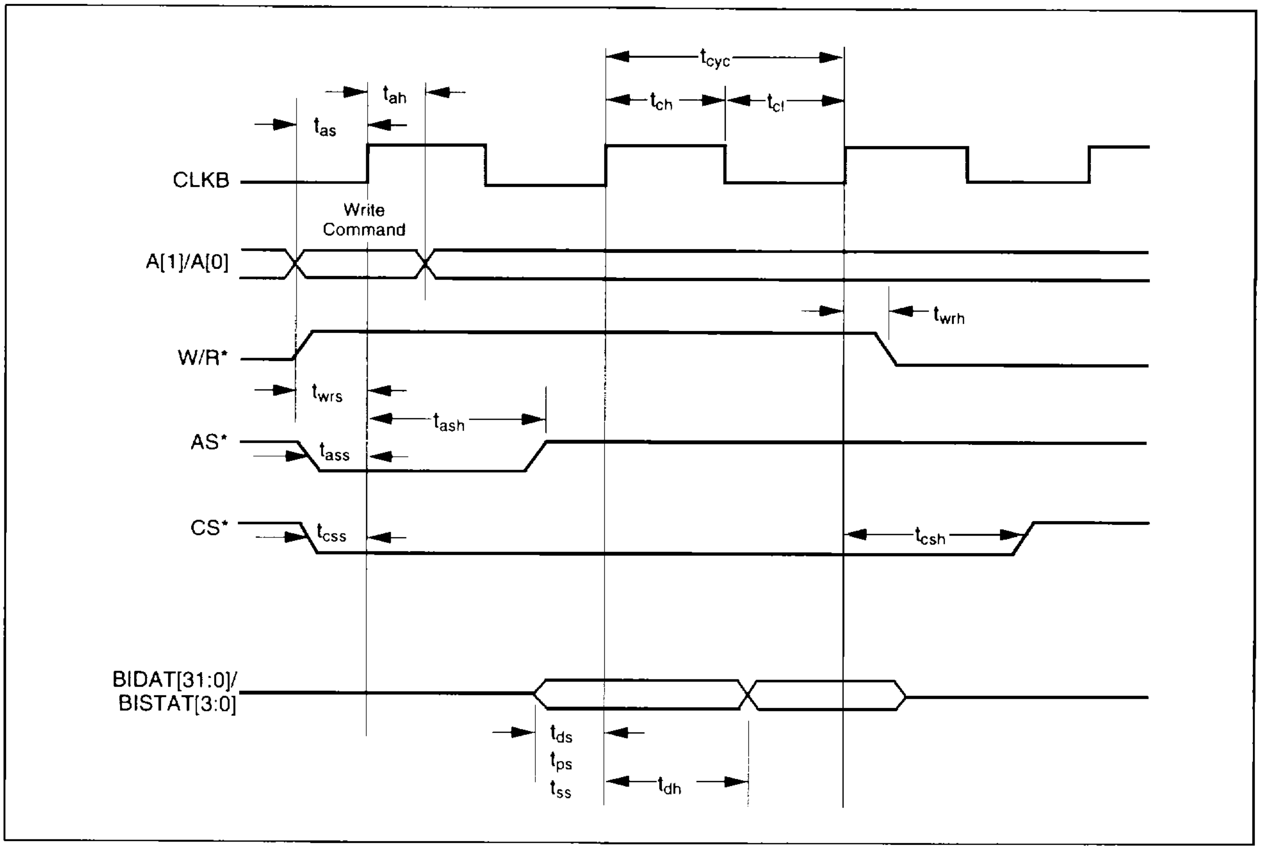


Table 5-2 and Figure 5-2 show the timing requirements for a microprocessor interface burst read cycle. All times are measured with 50 pF on the output pins.

Table 5-2. Microprocessor Burst Read Timing

Parameter	Description	Min	Typ	Max
t_d	Data Change from CLKB			15
t_v	Data Valid at Beginning of Read Cycle			20
t_{izd}	Data Driven to High Z from CLKB			18
t_{ezd}	Data Driven to High Z from OE*			14
t_{idz}	Data Driven to High Z from CS*			19
t_{edz}	Data Driven to High Z from OE*			16

Figure 5-2. Microprocessor Burst Read Cycle

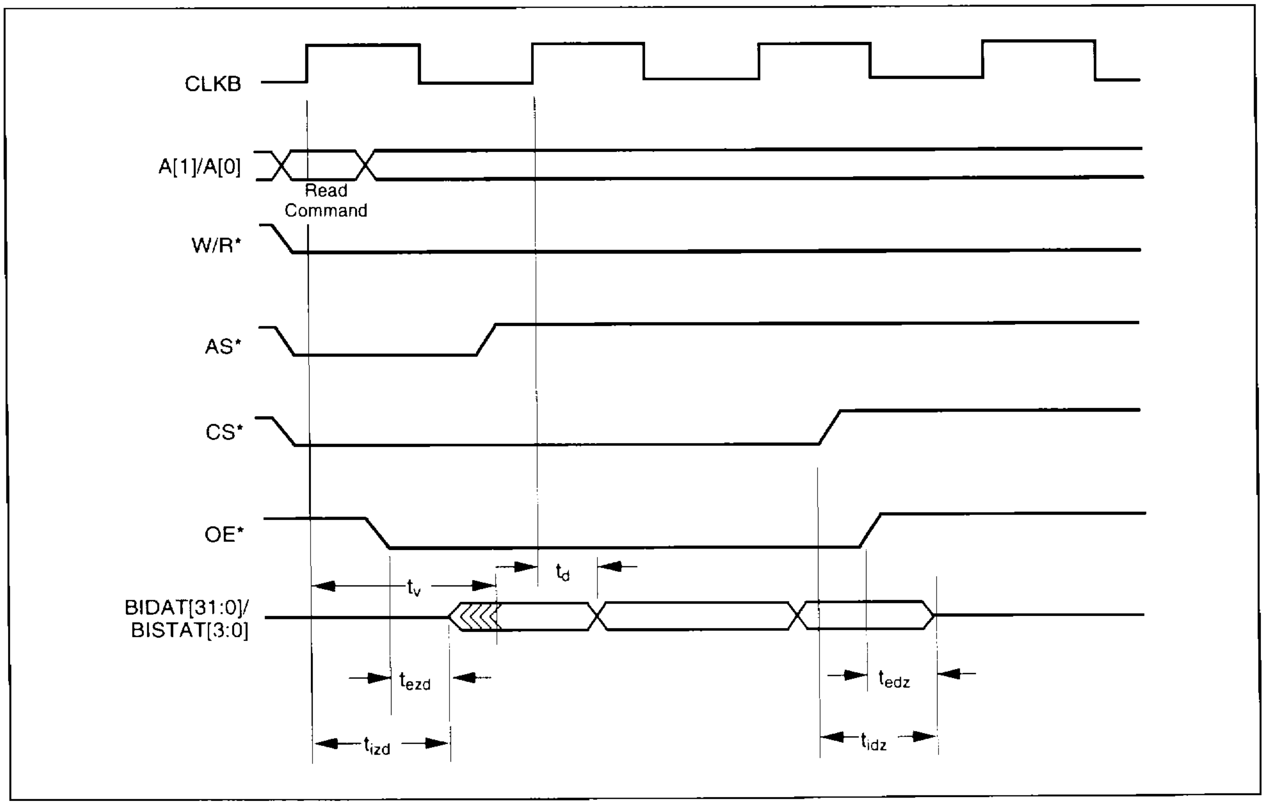


Table 5-3 and Figure 5-3 show the timing of the bidirectional port for asynchronous timing operation. All times are measured with 50 pF on the output pins.

Table 5-3. Bidirectional Asynchronous Port Timing

Parameter	Description	Min	Typ	Max
t_{cyc}	Minimum Strobe Period	35		
t_{ch}	Strobe High Pulse Width	12		
t_{cl}	Strobe Low Pulse Width	12		
t_{su}	Data Setup Time to WRB*	9.5		
t_h	Data Hold Time from WRB*	2.0		
t_{accb}	Data Access Time from RDB*			35
t_{zdb}	Data Driven to High Z from RDB*			13
t_{dzb}	Data Driven to High Z from RDB*			15

Figure 5-3. Bidirectional Asynchronous Port

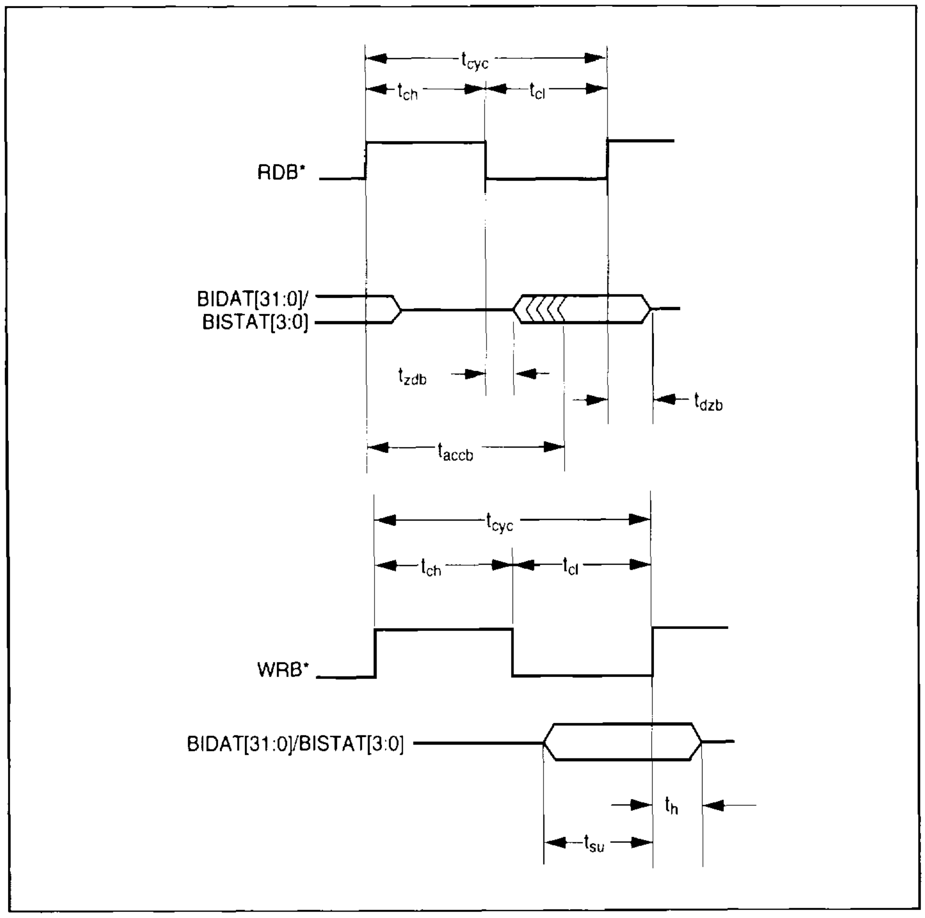


Table 5-4 and Figure 5-4 and show the timing of the bidirectional port in the synchronous mode. All times are measured with 50 pF on the output pins.

Table 5-4. Bidirectional Synchronous Port Timing

Parameter	Description	Min	Typ	Max
t_{cyc}	Minimum Clock Period	30		
t_{ch}	Clock High Pulse Width	12		
t_{cl}	Clock Low Pulse Width	12		
t_{su}	Data Setup Time to WRB*	9.5		
t_h	Data Hold Time from WRB*	2.0		
t_{sur}	Read Enable Setup Time	6.0		
t_{hr}	Read Enable Hold Time	0.5		
t_{suw}	Write Enable Setup Time	7.0		
t_{hw}	Write Enable Hold Time	0.0		
t_{zd}	Data Driven to High Z			15.5
t_d	Data Valid			15
t_{dz}	Data Driven to High Z			16.5

Figure 5-4. Bidirectional Synchronous Port

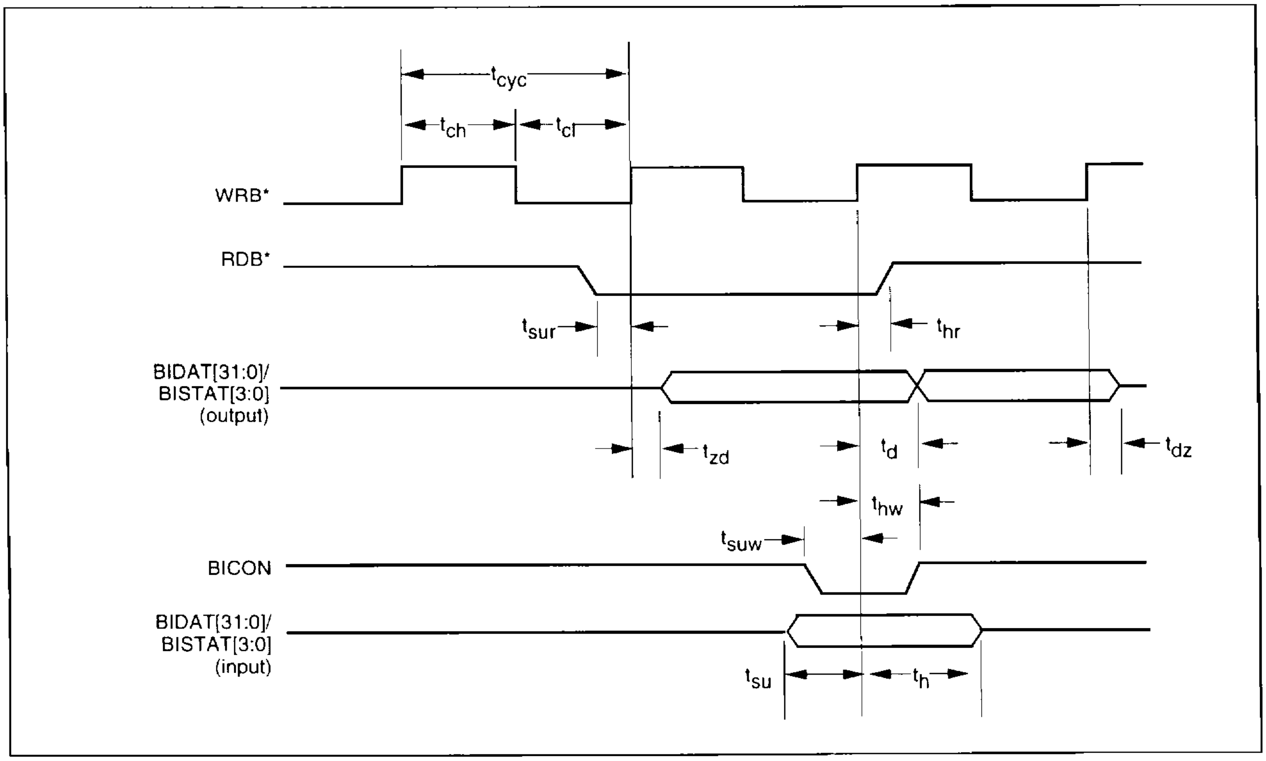


Table 5-5, Table 5-6. Table 5-7, Table 5-8, and Table 5-9 give propagation delays for the output signals. The output signal timing is relative to the listed edge of the clock or signal. Input signals should have setup and hold times with respect to the listed edge of the given input clock. All output signals are measured with 20 pF loading. Figure 5-5 shows the clock and data relationships for the unidirectional input and output signals.

Table 5-5. Unidirectional Port Clock Timing

Symbol	Min
Low Pulse Width - t_{pwl}	20
High Pulse Width - t_{pwh}	20
Cycle Time - t_{cyc}	50

Table 5-6. Unidirectional Port Input Setup and Hold Timing

Input Signal	Input Clock - Edge	T_{SU} Min	T_{HD} Min
WCON	WRU* - Rising	5.0	1.0
WCON	WRU* - Rising	5.0	1.0
WCON in HDLC Mode	WRU* - Rising	13.0	1.0
WCON in Cell Mode	WRU* - Rising	11.0	1.0
WREN*	WRU* - Rising	2.0	1.0
WSTAT	WRU* - Rising	6.0	1.0
WSTAT in HDLC Mode	WRU* - Rising	13.0	1.0
UINDAT[8:0]	WRU* - Rising	14.0	1.0
RDEN*	RDU* - Rising	6.0	1.0
RCON	RDU* - Rising	5.0	1.0

Table 5-7. Propagation Delays—Unidirectional Port Asynchronous Timing Operation

Symbol - Async mode	Parameter	Min	Max
t_{zd}	Data Driven to High Z		9.0
t_{dz}	Data Driven to High Z		11.0
t_{pd}	Data Change		34
t_{pd}	CELL_OUT Prop Delay		21

Table 5-8. Propagation Delays —Unidirectional Port Modes, No Asynchronous Timing

Symbol - Modes other than Async	Parameter	min	max
t_{zd}	Data Driven to High Z		13.0
t_{dz}	Data Driven to High Z		13.0
t_{pd}	Data Change		12
t_{pd}	CELL_OUT Prop Delay		15

Table 5-9. Other Propagation Delays—Unidirectional Port

Output Signal	Input Signal - Edge	Min	Max
IFF* in HDLC Mode	RDU* - Rising		11.0
OEF* in HDLC Mode	RDU* - Rising		11.0
CELL_OUT Rising in TAXI Mode	RDU* - Falling		12.0
CELL_OUT Falling in TAXI Mode	RDU* - Rising		13.0
OEF* Rising in CAS-A Mode	RDU* - Falling		10.0
OEF* Falling in CAS-A Mode	RDU* - Rising		9.0
OEF* in CAS-S Mode	RDU* - Rising		12.0
IFF* Rising in CAS-A Mode	WRU* - Rising		8.0
IFF* Falling in CAS-A Mode	WRU* - Falling		8.0
IFF* Rising in CAS-S Mode	WRU* - Falling		13.0
IFF* Rising in CAS-S Mode	WSTAT - Falling		10.0
IFF* Falling in CAS-S Mode	WRU* - Rising		11.0

Figure 5-5. Unidirectional Port Timing

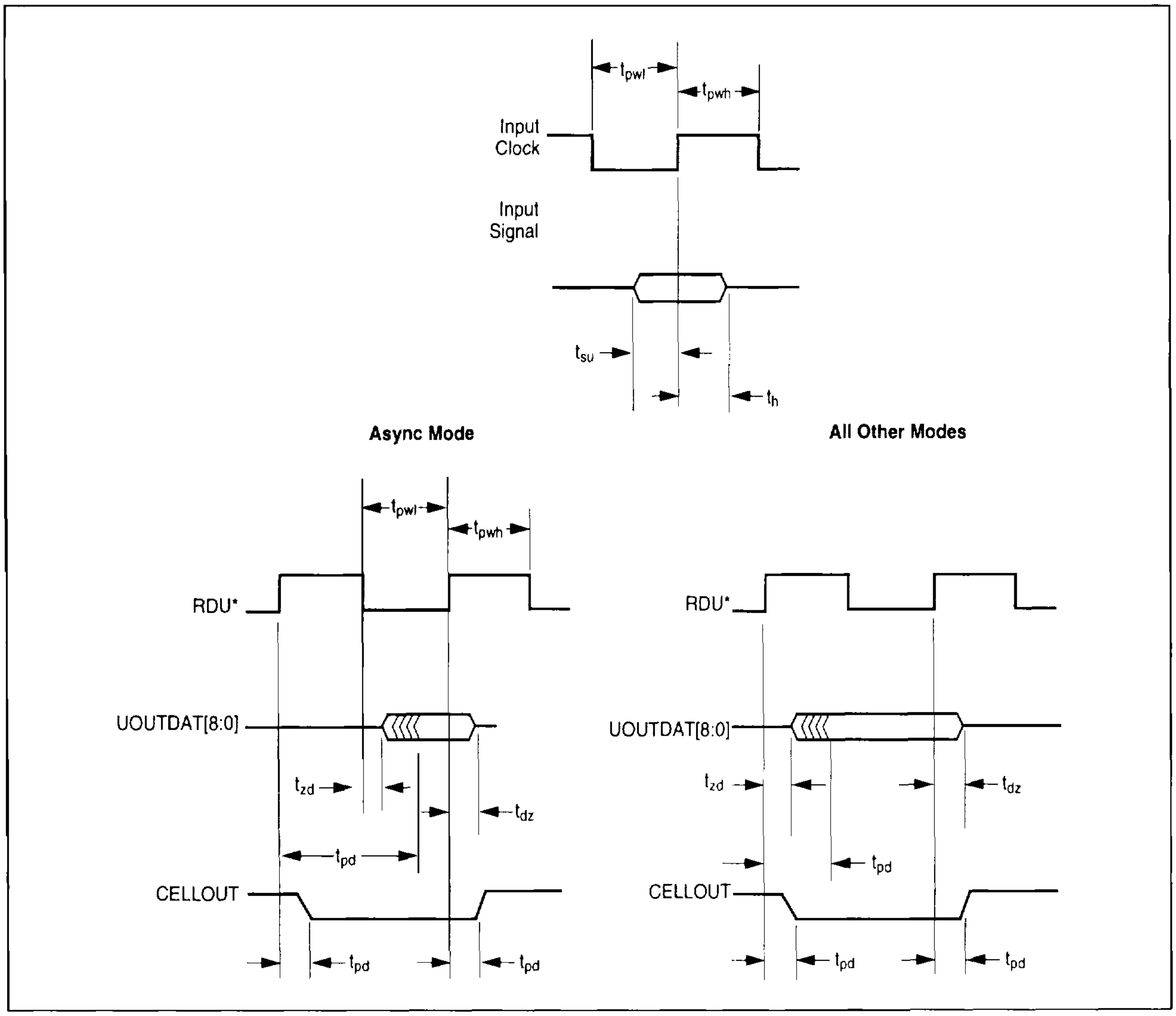


Table 5-10 and Table 5-11 specify the propagation delay of the buffer flags in asynchronous and synchronous operation. The IEF*, IAE*, OHF*, OAF*, and OFF* flags are controlled by the bidirectional port mode. When the bidirectional port is in default asynchronous timing operation, the flags are asynchronous. In all other modes they are synchronous. The IHF*, IAF*, IFF*, OEF*, and OAE* flags are controlled by the unidirectional port mode. When the unidirectional port is in asynchronous timing operation, the flags are asynchronous. In all other modes they are synchronous. All flag outputs are measured with 20 pF loading.

Table 5-10. Propagation Delays—Asynchronous Flags

Signal	Clock Edge	T_{PD} Min	T_{PD} Max
IEF* — Rising	WRU* — Rising		21.0
IEF* — Falling	RDB* — Falling		13.0
IAE* — Rising	WRU* — Rising		28.0
IAE* — Falling	RDB* — Falling		23.0
IHF* — Rising	RDB* — Rising		26.0
IHF* — Falling	WRU* — Falling		23.8
IAF* — Rising	RDB* — Rising		28.0
IAF* — Rising	WRU* — Falling		27.0
IFF* — Rising	RDB* — Rising		19.0
IFF* — Falling	WRU* — Falling		12.0
IFF* — Falling	WCON — Falling		12.0(1)
OEF* — Rising	WRB* — Rising		23.0
OEF* — Falling	RDU* — Falling		13.0
OEF* — Falling	RCON — Falling		13.0(2)
OAE* — Rising	WRB* — Rising		29.0
OAE* — Falling	RDU* — Falling		23.0
OHF* — Rising	RDU* — Rising		27.0
OHF* — Falling	WRB* — Falling		27.0
OAF* — Rising	RDU* — Rising		29.0
OAF* — Rising	WRB* — Falling		30.0
OFF* — Rising	RDU* — Rising		19.0
OFF* — Falling	WRB* — Falling		14.0

Notes: (1). If padding occurs when the last word is written to the input buffer, IFF* goes active when both WCON and WRU* are logic low.

(2). If padding occurs when the last word is read from the output buffer, OEF* goes active when both RCON and RDU* are logic low.

Table 5-11. Propagation Delays—Synchronous Flags

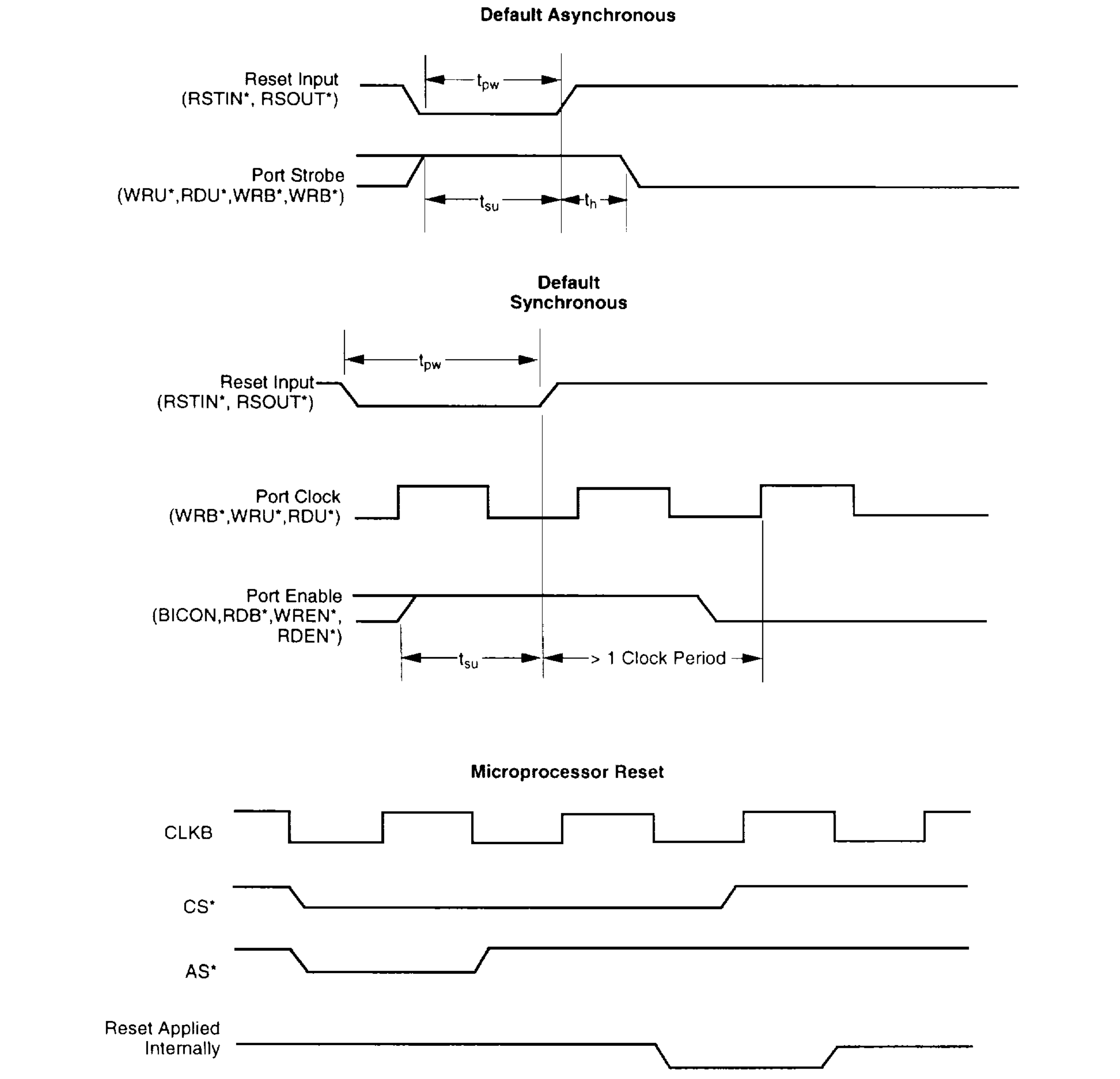
Signal	Clock Edge	T_{PD} Min	T_{pd} Max
IEF* — Rising	WRB* — Rising		14.0
IEF* — Falling	WRB* — Rising		13.0
IAE* — Rising	WRB* — Rising		12.0
IAE* — Falling	WRB* — Rising		11.0
IHF* — Rising	WRU* — Rising		13.0
IHF* — Falling	WRU* — Rising		13.0
IAF* — Rising	WRU* — Rising		13.0
IAF* — Rising	WRU* — Rising		13.0
IFF* — Rising	WRU* — Rising		12.0
IFF* — Falling	WRU* — Rising		12.0
OEF* — Rising	RDU* — Rising		13.0
OEF* — Falling	RDU* — Rising		13.0
OAE* — Rising	RDU* — Rising		12.0
OAE* — Falling	RDU* — Rising		11.0
OHF* — Rising	WRB* — Rising		15.0
OHF* — Falling	WRB* — Rising		14.0
OAF* — Rising	WRB* — Rising		14.0
OAFIHF* — Rising	WRB* — Rising		15.0
OFF* — Rising	WRB* — Rising		13.0
OFF* — Falling	WRB* — Rising		13.0

There are three modes of reset timing: default asynchronous, default synchronous, and microprocessor. The first two modes use dedicated input pins to reset the input and output buffers. The third uses the microprocessor interface.Table 5-12 and Figure 5-6 show the timing for all three cases. The retransmit timing is the same as the reset timing.

Table 5-12. Reset Timing

Symbol	Parameter	Min	Typ	Max
T_{pw}	Reset Pulse Width	10		
T_{su}	Control Signal Setup to End of Reset	10		
T_H	Control Signal Hold from End of Reset	10		

Figure 5-6. Reset Timing


Default Asynchronous
Reset Input (RSTIN*, RSOUT*)
t_{pw}
Port Strobe (WRU*,RDU*,WRB*,WRB*)
t_{su}
t_h
Default Synchronous
t_{pw}
Reset Input (RSTIN*, RSOUT*)
Port Clock (WRB*,WRU*,RDU*)
Port Enable (BICON,RDB*,WREN*, RDEN*)
t_{su}
> 1 Clock Period
Microprocessor Reset
CLKB
CS*
AS*
Reset Applied Internally

Note: Default reset timing applies to the unidirectional port with respect to the internally applied reset signal shown in this figure.

5.2 Environmental Conditions

5.2.1 Power Requirements and Temperature Range

Stresses above those listed in Table 5-13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-13. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	Volts
Input Voltage	V_{IN}	–0.3 to Vcc +0.3	Volts
Output Voltage	V_{OUT}	–0.3 to Vcc +0.3	Volts
Operating Temperature	TA	–40 to 85	°C
Storage Temperature	T_{STG}	–55 to +150	°C
Operating Supply Voltage	V_{CC}	4.75 to 5.25	Volts
Maximum Current @ 33 MHz	I_{CC}	70	mA

5.3 Electrical Characteristics

5.3.1 DC Characteristics

DC characteristics are given in Table 5-14. All inputs and bidirectional signals have input thresholds compatible with TTL drive levels. WCON, RCON, JTRES*, JTMS, and JTDI pins have pullup resistors. Their input leakage current is 10 µA max. at logic high and 350 µA max. at logic low. All other pins have an input leakage current less than 10 µA in any state. All outputs have drive current I_{OL} = 4 mA at 0.4 V and I_{OH} = –4 mA at 2.4 V. All outputs are CMOS drive levels and can be used with CMOS or TTL logic.

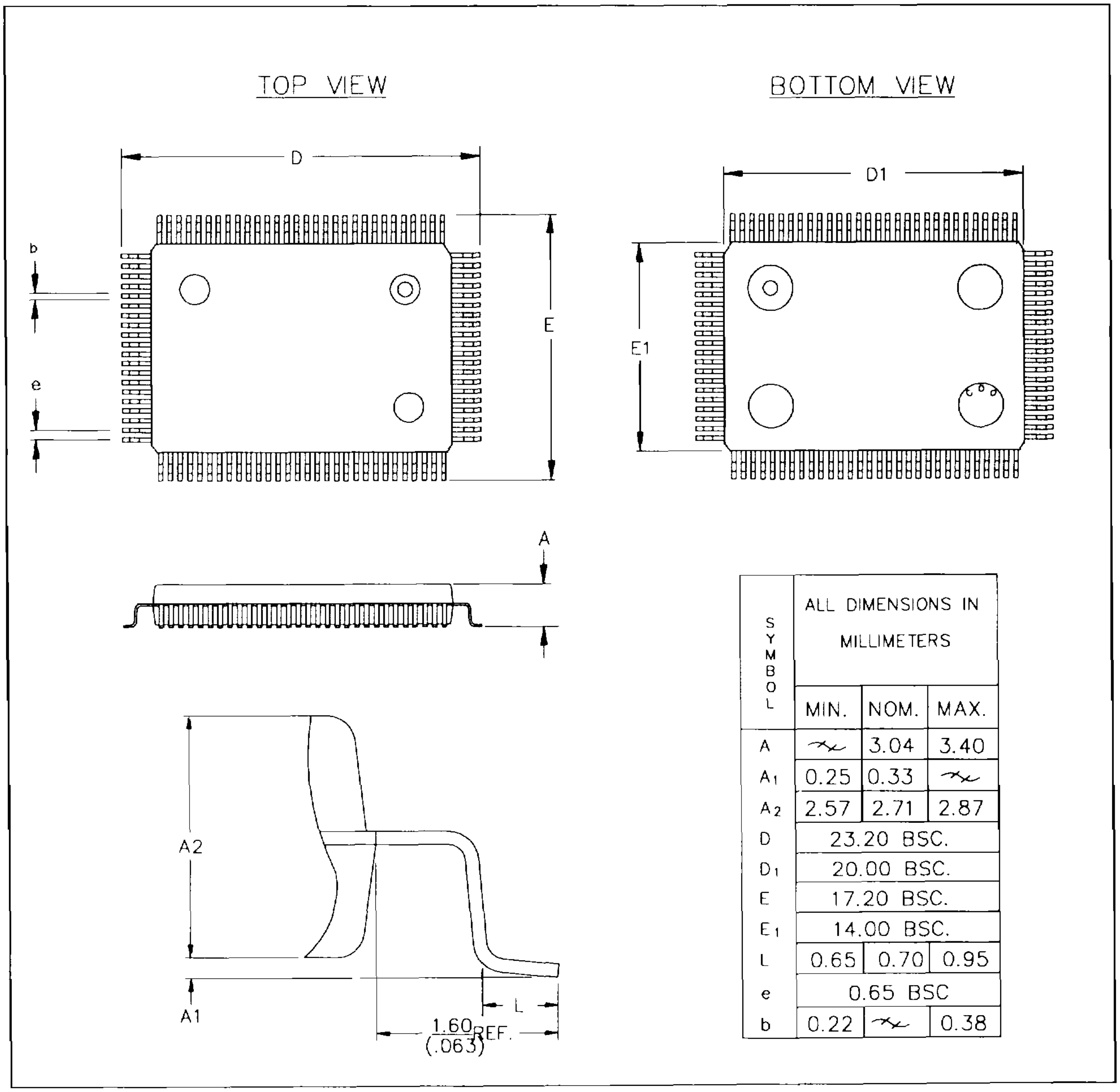
Table 5-14. DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.75	5.00	5.25	Volts
V_{OH}	All Outputs, AD[7:0]	I_{OH} = –4mA	2.4	4.5		Volts
V_{OL}	All Outputs, AD[7:0]	I_{OH} = –4mA		0.2	0.4	Volts
V_{IH}	Input Voltage High	V_{DD} = 5.0 V	2.0			Volts
V_{IL}	Input Voltage Low	V_{DD} = 5.0 V			0.8	Volts
I_{DD}*	Supply Current	V_{DD} = 5.0 V @ 33 MHz			70	mA
I_{IL}	Input Leakage Current	0V≥V_{IN}≥V_{CC}		±1.0	±10	µA
I_{OL}	Output Leakage Current	0V≥V_{IN}≥V_{CC}		±1.0	±1.0	µA
I_{OS}	Output Short Circuit Current	V_O = V_{CC} VO = VSS(1)	37 –117		140 –40	mA
C_{IN}	Input Capacitance	All Inputs and Bidirectional			3.0	pF
C_{OUT}	Output Capacitance	All Outputs			3.0	pF
V_{CC}	Operating Supply Voltage		4.75		5.25	Volts
	ESD Protection	MIL-STD-883C Method 3015	2	>3		kVolts
	Latch-up Input	JEDEC JC-40.2	150	>400		mA

Notes: (1). WCON, RCON, JTRES*, JTMS, and JTDI pins have internal pullup resistors. For these inputs, the input leakage current is 350 microamp max at logic low.

5.4 Mechanical Specifications

Figure 5-7. 100-Pin Plastic Quad Flat Pack (PQFP)



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	3.04	3.40
A_1	0.25	0.33	~
A_2	2.57	2.71	2.87
D	23.20 BSC.		
D_1	20.00 BSC.		
E	17.20 BSC.		
E_1	14.00 BSC.		
L	0.65	0.70	0.95
e	0.65 BSC		
b	0.22	~	0.38

5.5 Pin Descriptions

The Bt8215 Bidirectional Cell Buffer is packaged in a 100-pin Plastic Quad Flat Pack (PQFP). Figure 5-8 illustrates a package pinout diagram for this device, including dual function pins. Pin assignments for both stand-along smart FIFO and microprocessor modes are listed in numerical order in Table 5-15.

Figure 5-8. Bidirectional Cell Buffer Pinout Diagram

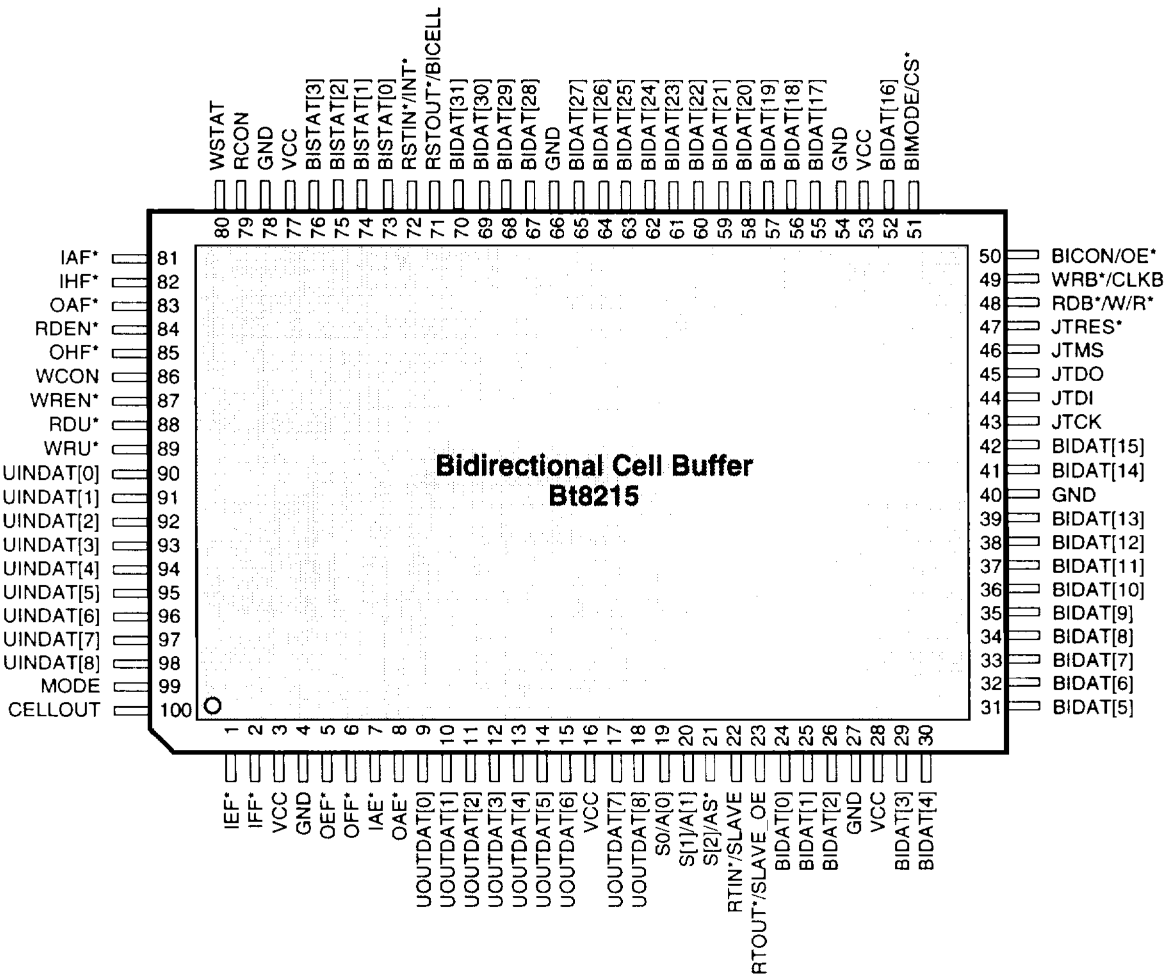


Table 5-15. Bt8215 Pin Assignments

Pin	Pin Label	I/O
1	IEF*	O
2	IFF*	O
3	V_{CC}	I
4	GND	I
5	OEF*	O
6	OFF*	O
7	IAE*	O
8	OAE*	O
9	UOUTDAT[0]	O
10	UOUTDAT[1]	O
11	UOUTDAT[2]	O
12	UOUTDAT[3]	O
13	UOUTDAT[4]	O
14	UOUTDAT[5]	O
15	UOUTDAT[6]	O
16	V_{CC}	I
17	UOUTDAT[7]	O
18	UOUTDAT[8]	O
19	S[0]/A[0]	I
20	S[1]/A[1]	I
21	S[2]/AS*	I
22	RTIN*/SLAVE*	I
23	RTOUT*/ SLAVE_OE	I/O
24	BIDAT[0]	I/O
25	BIDAT[1]	I/O
26	BIDAT[2]	I/O
27	GND	I
28	V_{CC}	I
29	BIDAT[3]	I/O
30	BIDAT[4]	I/O
31	BIDAT[5]	I/O
32	BIDAT[6]	I/O
33	BIDAT[7]	I/O
34	BIDAT[8]	I/O
35	BIDAT[9]	I/O
36	BIDAT[10]	I/O
37	BIDAT[11]	I/O
38	BIDAT[12]	I/O
39	BIDAT[13]	I/O
40	GND	I
41	BIDAT[14]	I/O
42	BIDAT[15]	I/O
43	JTCK	I
44	JTDI	I
45	JTDO	O
46	JTMS	I
47	JTRES*	I
48	RDB*/W/R*	I
49	WRB/CLKB	I
50	BICON/OE*	I
51	BIMODE/CS*	I
52	BIDAT[16]	I/O
53	V_{CC}	I
54	GND	I
55	BIDAT[17]	I/O
56	BIDAT[18]	I/O
57	BIDAT[19]	I/O
58	BIDAT[20]	I/O
59	BIDAT[21]	I/O
60	BIDAT[22]	I/O
61	BIDAT[23]	I/O
62	BIDAT[24]	I/O
63	BIDAT[25]	I/O
64	BIDAT[26]	I/O
65	BIDAT[27]	I/O
66	GND	I
67	BIDAT[28]	I/O
68	BIMODE/CS*	I
69	BIDAT[30]	I/O
70	BIDAT[31]	I/O
71	RSTOUT*/BICELL	I
72	RSTIN*/INT*	I
73	BISTAT[0]	I/O
74	BISTAT[1]	I/O
75	BISTAT[2]	I/O
76	BISTAT[3]	I/O
77	V_{CC}	I
78	GND	I
79	RCON	I
80	WSTAT	I
81	IAF*	O
82	IHF*	O
83	OAF*	O
84	RDEN*	I
85	OHF*	O
86	WCON	I
87	WREN*	I
88	RDU*	I
89	WRU*	I
90	UINDAT[0]	I
91	UINDAT[1]	I
92	UINDAT[2]	I
93	UINDAT[3]	I
94	UINDAT[4]	I
95	UINDAT[5]	I
96	UINDAT[6]	I
97	UINDAT[7]	I
98	UINDAT[8]	I
99	MODE	I
100	CELLOUT	O

Appendix A

Using the Bt8215 as a Bt8210 SCARF Host Buffer, AN-8212

Introduction

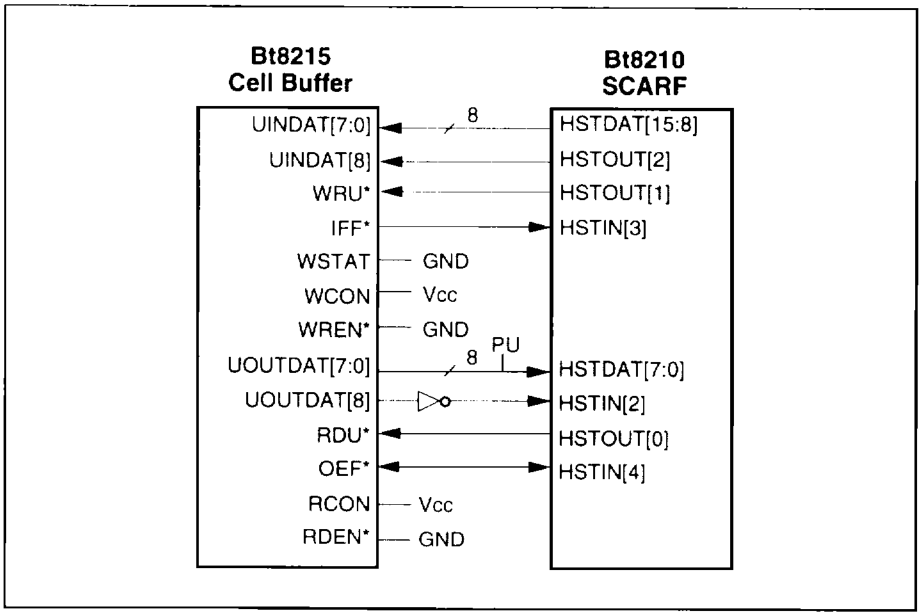
The Bt8215 Bidirectional Cell Buffer consolidates the interface circuitry for a 32-bit buffer interface to the Bt8210 or B8209 SMDS Control and Reassembly Formatters. The Bt8215 provides cell-based transfer capabilities to simplify host access to the Bt8210 at speeds up to 33 MHz.

This application note describes the required interconnection and configuration of both the Bt8215 and Bt8210 for the Bt8215 to provide a buffer function between the Bt8210 and a host bus. In bidirectional microprocessor, synchronous, and asynchronous applications, the Bt8210 host circuitry needs to be configured in the 32-bit octet expansion mode. This is accomplished by setting bits 0 through 7 of the HSTCTRL Register in the Bt8210 to 0xD1. The BISTAT[3:0] bus provides message delineation for the BIDAT[31:0] bus. BISTAT[3] covers BIDAT[31:24], BISTAT[2] covers BIDAT[23:16], BISTAT[1] covers BIDAT[15:8], and BISTAT[0] covers BIDAT[7:0]. The system clock of the Bt8210 chip may operate at the maximum of 33 MHz.

Bidirectional Microprocessor Interface

This mode allows the Bt8215 bidirectional bus to be connected directly to a 32-bit synchronous microprocessor bus. Each bit of the BISTAT[3:0] bidirectional bus needs to be tied to a pullup resistor. The unidirectional port to Bt8210 connection is shown in Figure A-1.

Figure A-1. Bt8210 to Bt8215 Connection



This connection requires an external inverting gate that inverts the mark bit to the polarity required by the Bt8210. Pullup resistors on the UOUTDAT[8:0] bus are suggested since the outputs are three-stated when the RDU* input is a logic high. The Bt8215 device must be configured through Control Register A for an asynchronous unidirectional interface and a normal bidirectional address map.

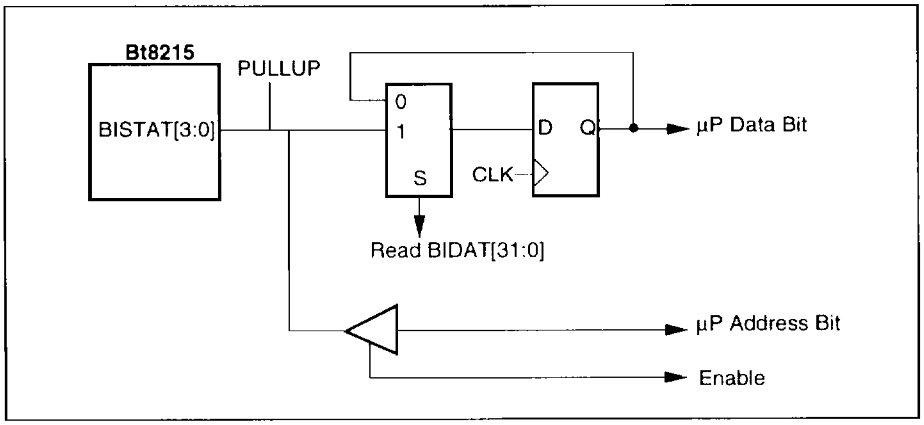
To write a message to the output buffer, the Write Buffer and Write Last Word address decoded commands are used. Write Last Word is used with the last word of a message to internally set the delineation bit to a logic low. Write Buffer is used to write the other words of the message. The byte position of the delineation bit is controlled by the Pad Bytes[1,0] field in Control Register A. Before using Write Last Word, this field must correspond to the last byte of a word. For example, if only the most significant byte of the word is active, the field is set to 3.

Read Buffer and Read Status commands are used to read a message from the output buffer. Read Buffer is used to read the contents of the output buffer and Read Status is used to read the BISTAT[3:0] values. The status register must be read after every read of the input buffer to determine end of message delineation. If any BISTAT[3:0] bit, bits 22 through 24 of the status register, are a logic low, then the current word is the end of a message. The most significant bit with a logic low determines the last byte of a word. If BISTAT[3] is a logic low, then there is only one valid byte in the current word. This byte is BIDAT[31:24].

Bidirectional Default Interface

The bidirectional default interface allows generic FIFO control circuitry to connect with the Bt8215 bidirectional port. Message delineation is provided on the BISTAT[3:0] pins. Special circuitry is needed to read and write to the BISTAT[3:0] pins. BISTAT[3:0] external circuitry is shown in Figure A-2. The unidirectional connection to the Bt8210 chip is the same as shown in Figure A-1 except that the inverting gate is not needed.

Figure A-2. BISTAT[3:0] External Circuitry



Address bits are used to write the message delineation bit to the output buffer. The value of the BISTAT[3:0] bit corresponding to the last byte of a message must be a logic high. All other bits must be a logic low. For example, BISTAT[3:0] bus has a value of 0xF for all words except the last word and 0x8 on the last word of a message if only 1 byte is valid. The ENABLE signal is active only when the output buffer is being written.

As in the microprocessor interface, the BISTAT[3:0] bus must be read after every read of the input buffer to determine message delineation. The above circuit stores the value of the BISTAT[3:0] bus during a read of the input buffer for later reading by the microprocessor. A logic high on a BISTAT[3:0] bit delineates a message on a byte boundary.

Performance Enhancements

A burst read interface to the Bt8215 can be created in external logic. This will reduce the number of processor cycles required to transfer data from the Bt8215. The logic for this function fits easily into an external programmable logic device. External logic eliminates the need for the processor to read the message buffer and then poll the status register to check for message encoding. This is accomplished with a simple state machine that does the polling for the microprocessor.

Appendix B

VPI/VCI Translation Engine for the Bt8215 Switch Fabric

Introduction

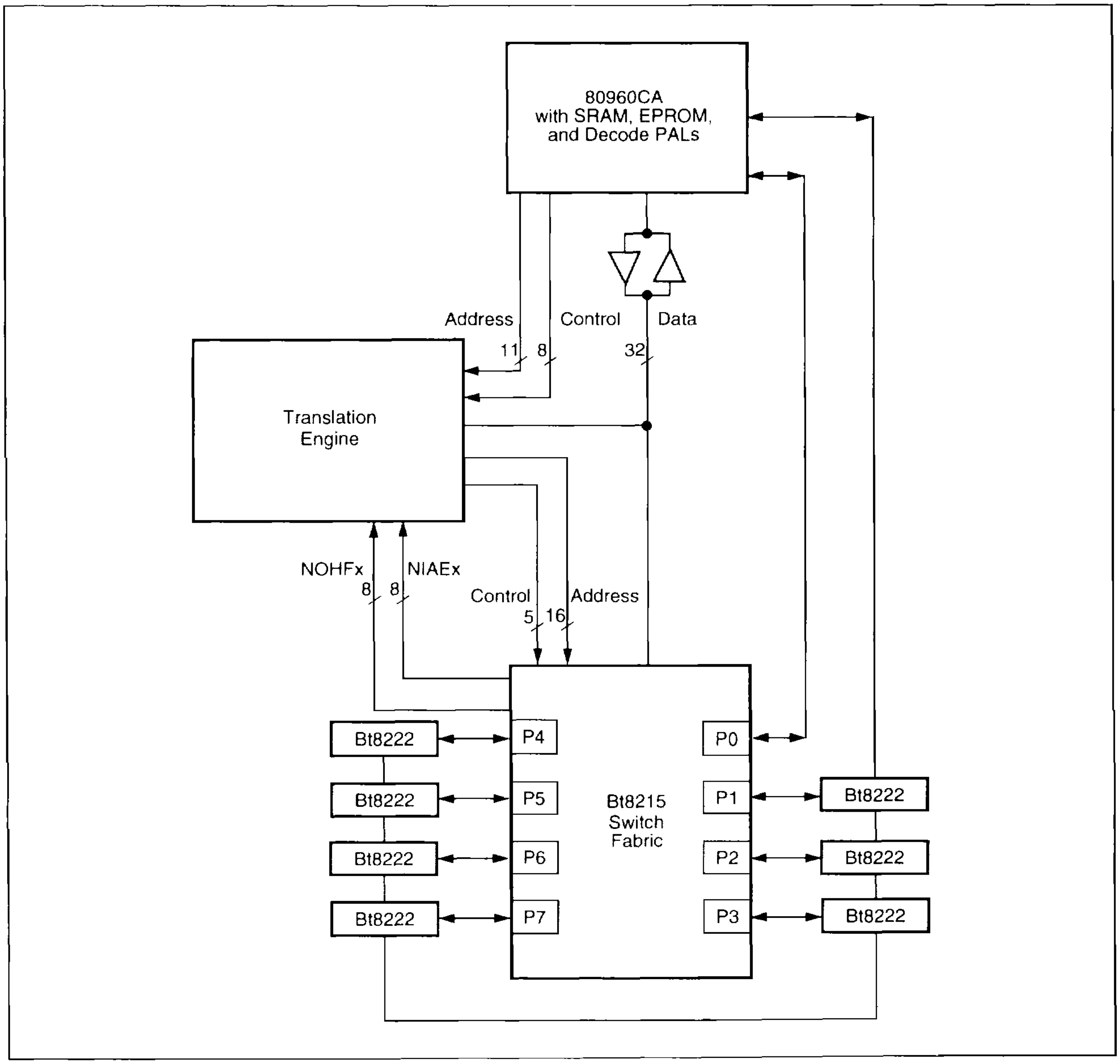
Brooktree's Bt8215 Bidirectional Cell Buffer implements an ATM switch when used with the appropriate VPI/VCI translation engine. The translation engine may be used in two ways: in software, as on the Bt8215 EVM-S; or in hardware, using an FPGA with Content Addressable Memory (CAM) or Static RAM (SRAM). This application note describes the hardware external implementation. Refer to the Switch Evaluation Board User's Guide for the software description. Requirements for switched virtual circuit operation through microprocessor access to one of the switch fabric ports are also described herein. A block diagram of the switch is illustrated in Figure B-1.

The switch fabric consists of eight Bt8215 devices. Seven of the ports are connected to a Bt8222 to supply the physical layer. The VPI/VCI translation takes place while the data is being transferred from input to output buffer. To implement an Switched Virtual Circuit (SVC), the eighth port is connected to the microprocessor. This allows the switch to receive/transmit management messages and process call setup/teardown information. The translation engine offloads the switching functionality from the microprocessor. It reads a source header from the switch fabric, translates the VPI/VCI, and writes a destination header or headers (in the case of broadcast) to the switch fabric. The translation engine can be implemented with an FPGA using either CAM or SRAM memory.

A hardware translation engine is desirable in high-speed ATM switching applications since the header translation must take place in 13 clock cycles to have no affect on throughput. Additionally, a translation engine allows the microprocessor to perform supervisory functions instead of only switching functions. This includes the ability to control all the Bt8222 devices for statistics gathering and to process SVC management messages. The translation engine also performs congestion reporting and mitigation. Congestion is reported by modifying the PTI field in the ATM header; mitigation is performed when needed by deleting cells that have their CLP bit set (refer to the Bt8230 datasheet).

Two translation engine architectures are described in this application note: CAM-based lookup and SRAM-based hash table lookup. The SRAM-based architecture has a faster multicast/broadcast algorithm than the CAM-based design. However, with the CAM-based design the FPGA circuitry is simpler and less memory is required for the full VPI/VCI field to be translated.

Figure B-1. Switch Block Diagram



Overall Design

The microprocessor block controls the translation engine through the address and control signals, and consists of an Intel 80960CA microprocessor, EPROM, SRAM, and PALS for address decoding. The control signals are NCS_XLAT, NCS_SFABRIC, NCS_FPGA, NAS, WNR, NWAIT, NBLAST, and PCLK. The translation engine controls the switch fabric through a separate set of address and control signals. The control signals to the switch fabric are NCS, NAS, WNR, NCELL, and CLK. The translation engine and the switch fabric share a common data bus that is separated from the microprocessor block by transceivers. This allows the microprocessor block to access the Bt8222 and P0 switch port while the translation engine is switching cells. The transceivers can be controlled by the DTNR and NDEN signals from the 80960CA. The microprocessor block can read and write the Bt8215 devices through the translation engine block, allowing the microprocessor block to initialize the switch fabric upon power-up or reset.

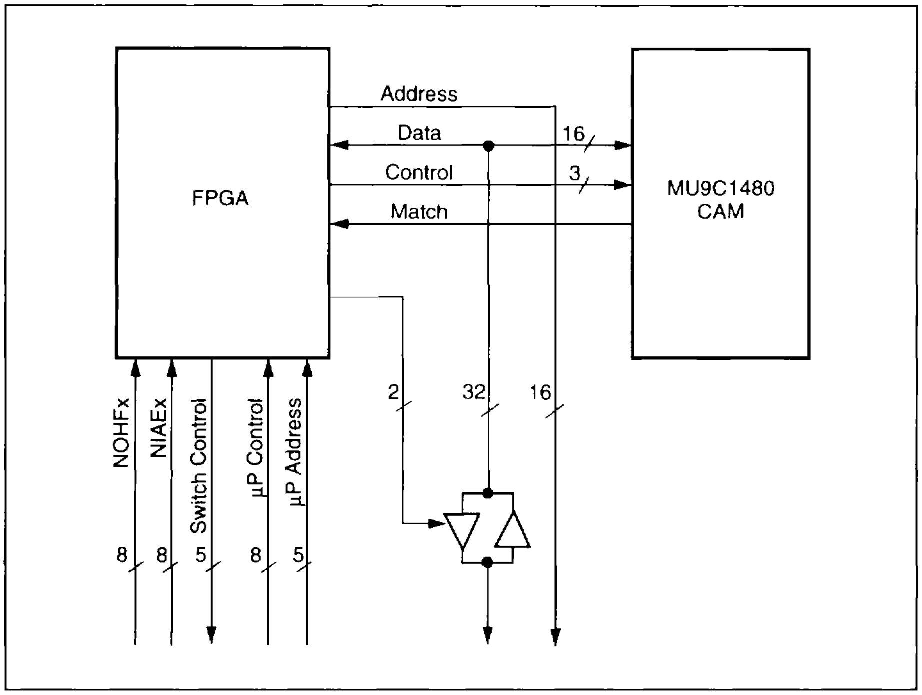
The NIAEx signals are used by the translation engine to determine which input port to read from. The translation engine may implement a priority scheme to determine the next read port. The NOHFx signals are used for congestion indication and control. If an output port is more than half full, all PTI fields written to the port are modified to indicate congestion. If the CLP bit is set, the cell is deleted from the output port.

The microprocessor block is connected to the P0 port of the switch fabric. This interface is an 8-bit interface. The unidirectional output data bus is tied to the unidirectional input data bus to implement an 8-bit bidirectional bus. The microprocessor block supplies the appropriate write sync, write strobe, and read strobe signals. The 80960CA can be internally configured for 8-bit port operation. This access to the switch allows the microprocessor block to perform call setup and teardown by modifying the contents of the memory in the translation engine. The microprocessor block is also directly connected to the Bt8222 device, allowing statistics gathering on a port-by-port basis and reporting of the statistics via management messages.

CAM-Based Translation Engine

Figure B-2 depicts a CAM-based translation engine. Using a Music Semiconductor CAM, Mu9C1480, the CAM can be configured for 32 bits of associative data (CAM) and 32 bits of associated data (RAM). This allows lookup of a source VPI/VCI port and return of a destination VPI/VCI port. The CAM has special instructions to handle multiple matches. These instructions allow simple multicast/broadcast operation. The design requires transceivers on the data bus to allow the switch fabric to transmit cells while the translation engine is generating the destination VPI/VCI port. FPGA controls the CAM and transceivers.

Figure B-2. CAM-Based Translation Engine



The microprocessor block has access to the switch fabric through the FPGA controller. Microprocessor control signals generate the switch control signals that allow reading and writing of the switch fabric through the 32-bit data bus. The five address lines into the FPGA consist of 2 switch address bits and 3 port address bits. During a read cycle, the desired port is addressed with the value of the switch address; other ports are addressed with a read status address. To prevent bus contention, the non-desired ports must be set up to disable status. During a write cycle, the desired port is addressed with the value of the switch address; other ports are addressed with a No Operation (NOP) address. This access is used mainly to initialize the Control Register A of the switch fabric at power-up or reset. For normal 52-octet cell operation, each register is written with a 0x005a0680.

The CAM is controlled by the /E, /CM and /W signals. The /E signal is a strobe, /CM is a command/data qualifier, and the /W signal is a read/write indication. The microprocessor block can access the CAM indirectly through the FPGA controller. Since the CAM currently has a 16-bit data bus, the FPGA controller must multiplex the µP data bus into the CAM data bus. Music Semiconductor is currently considering a 32-bit data version of the CAM. The CAM chip select and 5 address bits from the microprocessor block to the FPGA control the write and read cycles to and from the CAM. This access is used mainly for initialization of the CAM and writing and modifying of the address translation table. Reference the MU9C1480 LANCAM Handbook from Music Semiconductor for detailed information about the CAM device.

When initializing the CAM, the acronyms used are by Music semiconductor and are in their handbook except for cw, cr, dw, and dr. These mean command write cycle, command read cycle, data write cycle and data read cycle, respectively. The CAM can be initialized as follows:

```
cw      0000H
cw      TCO DS; disable device select feature
cw      FFFFH
cw      TCO PA; set page address to zero
cw      0000H
cw      TCO CT; reset
cw      0000H
cw      TCO CT; setup for 16 CAM, 16 RAM, and Mask with Mask 1
cw      8098H
cw      TCO SC; set destination for four segments and source for two segments
cw      1840H
cw      TCO DS; set Device Select Register equal to Page Register to enable read
cw      0000H
cw      SPD MR1; write to Mask 1 Register
dw      0001H
dw      0000h
cw      SPD M@NF, E; setup for writing translation table xlat_init_loop
dw      value; write translation table if more entries, goto xlat_init_loop
cw      TCO SC; setup for translation operation
cw      5C10H; write to segments 2 and 3, read from segments 0 and 1
cw      SPD CR
cw      SPS M@HM
```

Once the switch fabric and CAM are initialized, the FPGA controller may start the switch loop. The NIAEx inputs determine which input port(s) contain cells. Priority circuitry in the FPGA determines which port will be read. A cell header is read from the source port by addressing it with READ HEADER and the other ports with BROADCAST WRITE. The header is stored in the FPGA. The header is then written to the CAM with bits 1 through 3 modified to indicate the source port value. Bit 0 is masked in the CAM. If a match occurs, as indicated by the /MF output of the CAM, the destination VPI/VCI port is read from the CAM. Bit 0 is a multicast/broadcast indication. The destination VPI/VCI from the CAM is combined with the source PTI and CLP fields to generate a destination header.

The PTI fields may be modified to indicate congestion if the output port NOHF flag is active. The new header is written to the destination port by addressing it with WRITE HEADER and all other ports with DELETE CELL. If the CLP bit is set, the cell could also be deleted from the destination output port. If the multicast/broadcast bit is set, the destination port is addressed with a WRITE HEADER and the others with a NOP.

The CAM is read for the next destination VPI/VCI port and the new header written to the destination port. The CAM is read until the multicast/broadcast bit is not set. On the last header write, the destination port is written with a WRITE HEADER, previous destination ports of same cell with a NOP and all other ports with a DELETE CELL. The FPGA controls the CAM with the following state machine loop:

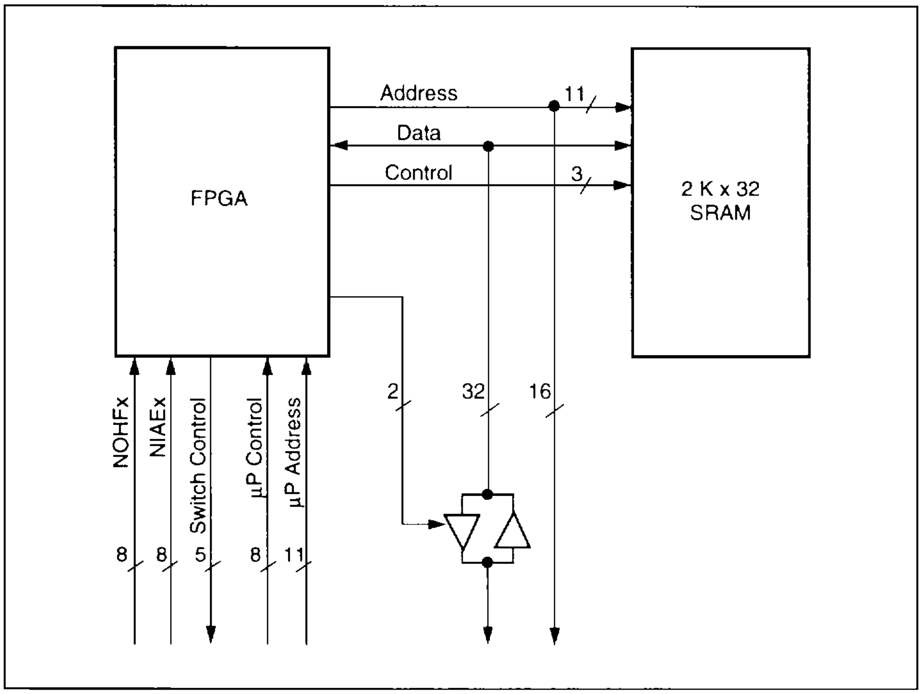
```
xlat_loop:
  Read Header from Switch Fabric
  dw  header bits 0-15; write to cam
  dw  header bits 16-31; write to cam
  IF  /MF = 0  THEN
    next_header:
       dr  header bits 0-15; read from cam
       dr  header bits 16-31; read from cam
       write new header to switch fabric
       IF multicast/broadcast bit set THEN
dw  VBC  HM , S; set skip bit
if   /MF = 0  THEN GOTO next_header
dw  CMP  S; mark all skips
dw  VBC  ALM , V; set all skip bits to valid
  GOTO xlat_loop
```

Currently, each access to/from the CAM is 90 nsec or three clock cycles with a 33 MHz bus. For a single port translation, the time is 12 cycles, which corresponds to the time it takes the switch fabric to transmit a cell to the output buffers. Each additional output port takes nine clock cycles to translate the header and two clock cycles are needed at the end of a multicast operation to clear the skip bits. Contact Music Semiconductor about their 32-bit version which improves this timing considerably.

SRAM-Based Translation Engine

The disadvantage of the CAM-based translation engine is that the multicast routine takes more than nine clock cycles per active output port. An SRAM-based engine is much faster, but is at the expense of FPGA complexity and increased memory size. A hashing algorithm is used to look up the destination header in SRAM. FPGA complexity is increased due to the hashing function. Memory size is increased to reduce the number of addresses per bin and to store the source VPI/VCI port. Figure B-3 depicts the SRAM-based design. Because the SRAM is addressed directly, the number of microprocessor address bits to the FPGA is increased. This section briefly describes the requirements for a SRAM design. With 25 nsec SRAM, this multicast routine requires less than four cycles per active output port.

Figure B-3. SRAM-Based Translation Engine



The memory size requirement for a hashing table is based on the number of active translation addresses. Assuming eight active addresses per port and eight ports, the translation table requires 64 active addresses. To keep the probability of no more than two addresses per hash bin above 95%, 1024 bins are needed. Each bin must store the source VPI/VCI port, destination VPI/VCI port, Next Link Address (NLA), and a couple of status bits. This design uses a 64-bit word per bin that requires a 2 K x 32 bit memory array. This table allows up to 18 bits of VPI/VCI and 3 bits of port information to be translated. A larger VPI/VCI field can be processed with a larger bin width.

The hashing circuitry performs a 10-bit CRC calculation on the source VPI/VCI port. The output of the CRC function becomes the hash table index. The bin pointed to by the hash table index is read and the source VPI/VCI port in the hash bin is compared against the source VPI/VCI port stored in the FPGA. If they compare and the Beginning Link Indicator (BLI) is set, the destination VPI/VCI port is used as a destination header/port. If they do not compare, and NLA is not the same as the current bin address, then the bin at the NLA is read. If the BLI in the first bin of the link list is not set then there is no link list active and therefore no comparison for the source VPI/VCI port. If the Broadcast Indicator (BI) is set, then there is another active header. The Next Broadcast Address (NBA) is used to determine the address of the next bin. Multicast continues until the BI bit is zero.

A 21-bit hashing offset register is provided in the FPGA to randomize the 10-bit CRC hashing function. This reduces the number of VPI/VCI port values per bin. The value of this offset register is added to the source VPI/VCI port value and processed with a 10-bit CRC function. The value of the offset register is determined by the microprocessor block during table initialization.

Figure B-4 shows the bin bit assignment map for single and multicast bins.

Figure B-4. Hash Bin Bit Map

Single Bin

3	1	2	6	4	12	4	# of Bits
SPT	BLI	NLA	SVP	NLA	SVC	NLA	LSW
DPT	BI	x	DVP	x	DVC	x	MSW

Multicast Bin

SPT	BLI	NLA	SVP	NLA	SVC	NLA	LSW
DPT	BI	NBA	DVP	NBA	DVC	NBA	MSW

where

SPT	Source Port
BLI	Beginning Link Indicator
NLA	Next Link Address
SVP	Source VPI
SVC	Source VCI
DPT	Destination Port
BI	Broadcast Indicator
DVP	Destination VPI
DVC	Destination VCI
NBA	Next Broadcast Index

Circuitry in the FPGA must detect if inactive bits in the VPI/VCI are set and discard the cell. Generation of a destination header is the same as in the CAM based engine. The source CLP and PTI fields are used with appropriate congestion modification with the destination VPI/VCI to generate a destination header.

Reference

MUSIC Semiconductors
1150 Academy Park Loop, Suite 202
Colorado Springs, CO 80910
719-570-1550

Appendix C

JTAG Overview

The Boundary Scan section of the Bt8215 provides access to all external I/O signals of the chip for board and system level testing. This circuitry conforms to IEEE Std 1149.1-1990.

The boundary scan test logic is accessed through five dedicated pins on the Bt8215. These pins are listed in Table C-1.

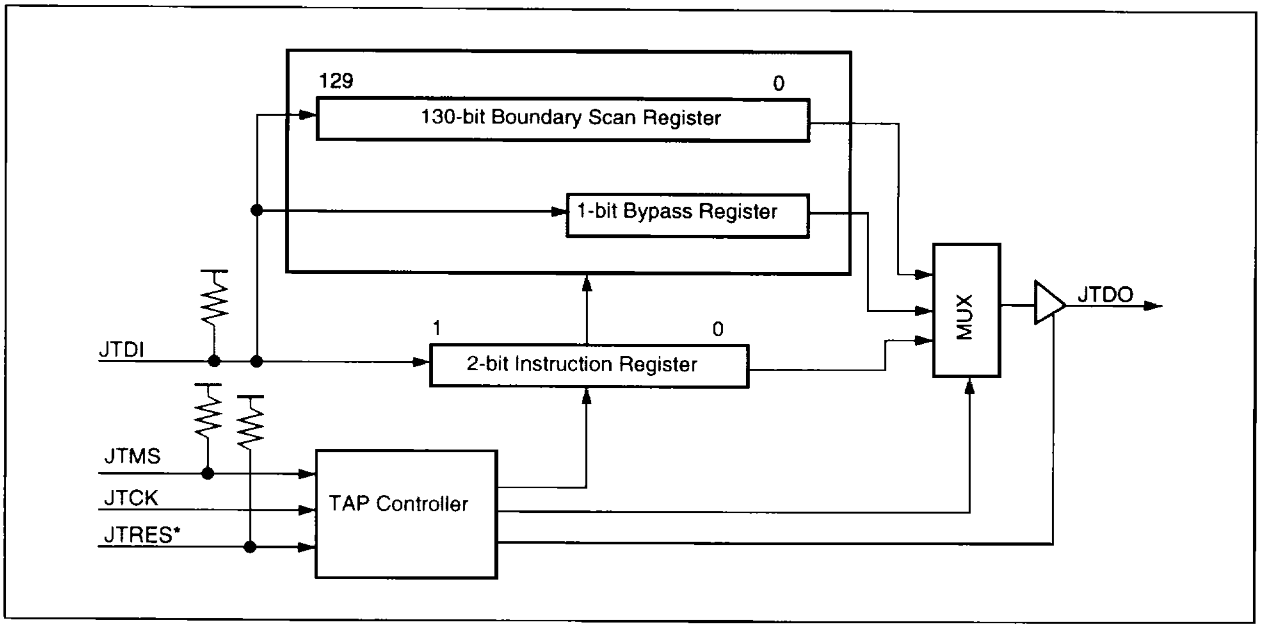
Table C-1. Boundary Scan Signals

Pin Name	Signal Name	I/O	Definition
JTRES*	Test Logic Reset	In	When at a logic low, this signal asynchronously resets the boundary scan test circuitry and puts the test controller into the reset state. This state allows normal system operation.
JTCK	Test Clock	In	Generated externally by the system board or by the tester. JTCK can be stopped in either the high state or low state.
JTMS	Test Mode Select	In	Decoded to control test operations.
JTDO	Serial Test Data Output	Out	Outputs serial test pattern data.
JTDI	Serial Test Data Input	In	Input for serial test pattern data.

The test circuitry includes a Bypass Register, an Instruction Register, a Boundary Scan Register, and the Test Access Port (TAP) Controller. Figure C-1 illustrates the test circuitry block diagram.

NOTE: If the boundary scan circuitry of the Bt8215 is not being used, tie the JTMS, JTDI, JTCK, and JTRES* to ground.

Figure C-1. Test Circuitry Block Diagram



Instruction Register

The Instruction Register (IR) is a 2-bit register with no parity. When the boundary scan circuitry is reset, the IR is loaded with the binary value 11 which is equivalent to the BYPASS Instruction. The instructions include the three IEEE 1149.1 mandatory public instructions (BYPASS, EXTEST, and SAMPLE/PRELOAD) and are listed in Table C-2. Bit 0 (LSB) is shifted into the instruction register first.

Table C-2. IEEE Std. 1149.1 Instructions

Bit 1	Bit 0	Instruction	Register Accessed
0	0	EXTEST	Boundary Scan
0	1	BYPASS	Bypass
1	0	SAMPLE/PRELOAD	Boundary Scan
1	1	BYPASS	Bypass

Bypass Register

The Bypass Register is a 1-bit shift register to pass JTDI data to JTDO to facilitate the testing of other devices in the scan path without having to shift the data patterns through the complete Boundary Scan Register of the Bt8215.

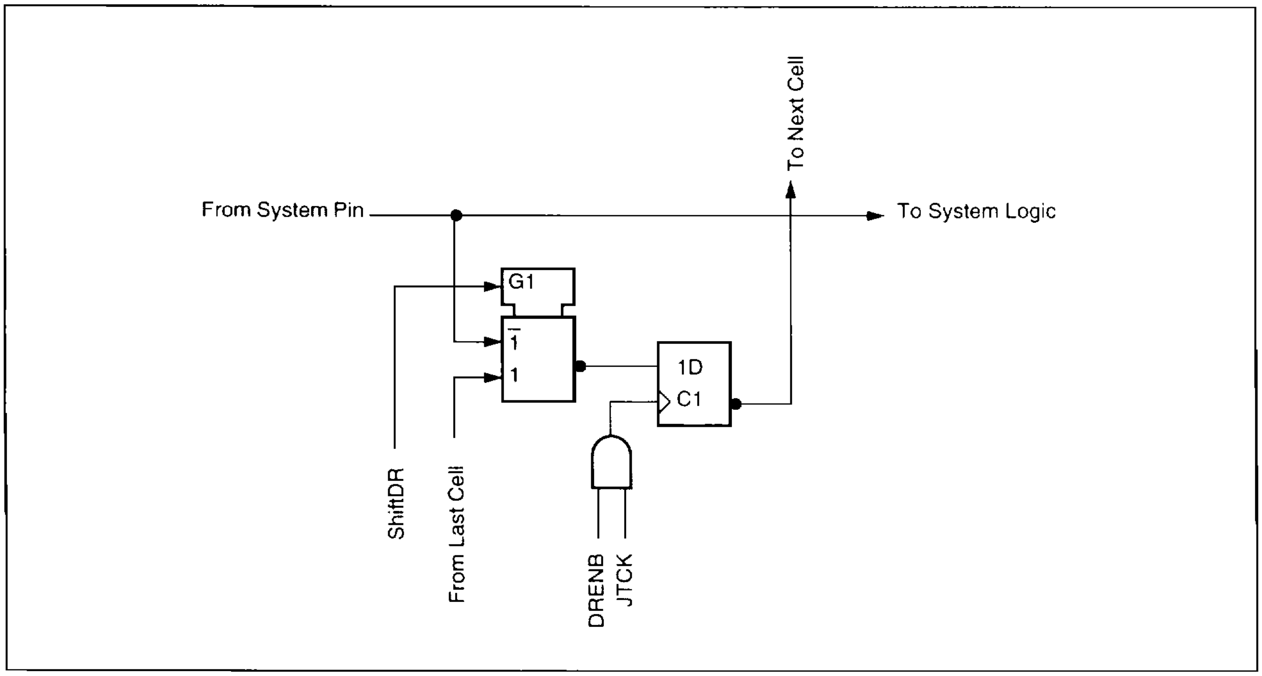
Boundary Scan Register

The Boundary Scan Register consists of two types of registers, Input-Observe and Output-Both. These registers correspond to IEEE 1149.1-1990 attributes and definitions.

Input-Observe

(IEEE 1149.1-1990 STD_1149_1_1990 Standard Boundary Cell name BC_4)
This cell captures an input value. The input-observe diagram is illustrated in Figure C-2.

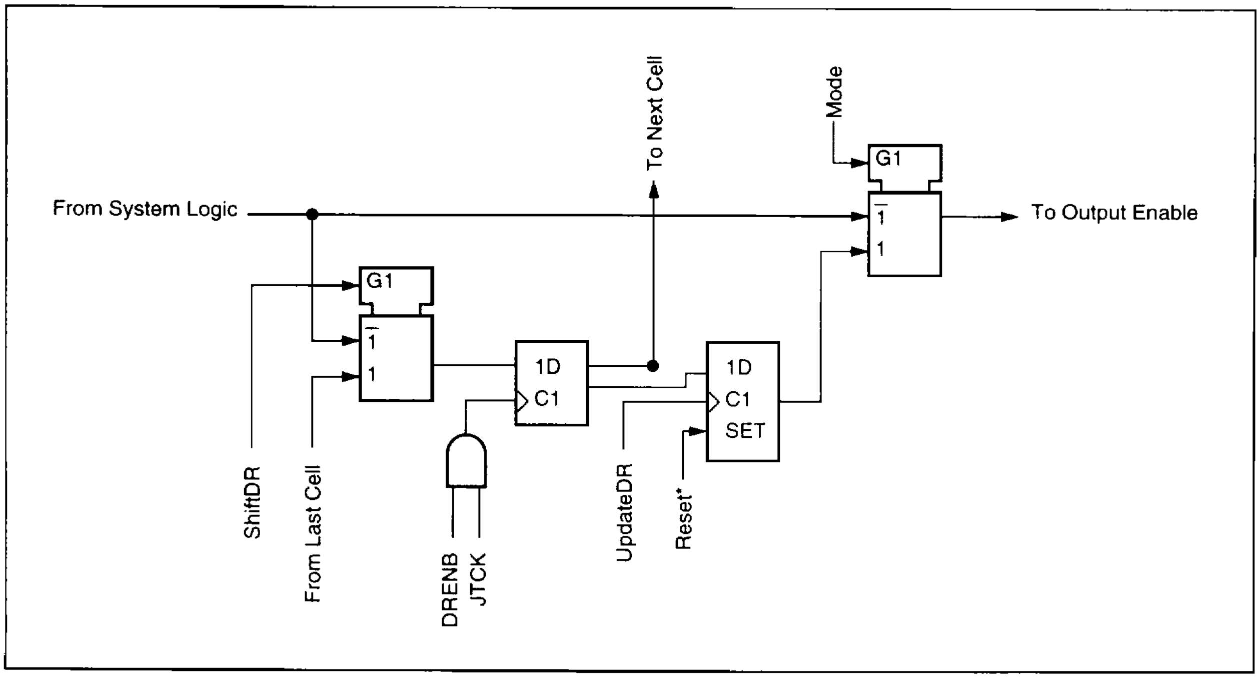
Figure C-2. Input-Observe Cell Diagram



Output-Both

(IEEE 1149.1-1990 STD_1149_1_1990 Standard Boundary Cell name BC_1) This cell is used as both a 3-s output control cell and a system output cell. As a control cell, it passes the system logic controlled output enable to the output I/O cell or controls the output enable of the output I/O cell during EXTEST. As an output cell, it passes the system logic controlled output to the output cell, or controls the output of the output cell during EXTEST. Note that the Reset*, which is controlled by the TAP Controller, will set the Update register to a high state because the Bt8215 uses active low enables for the I/O cells. The output-both cell diagram is shown in Figure C-3.

Figure C-3. Output-Both Cell Diagram



Boundary Scan Register Cells

Table C-3 defines the Boundary Scan Register cells.
Cell 0 is closest to JTDO in the chain.
Cell type definitions are:

- output3 = Output-Both (either the output cell of a bidirectional output or a three-state output)
- output2 = Output-Both (bi-state output)
- input = Input-Observe
- control = Output-Both

All controlling cells put their respective output cell into the inactive state with a value of 1.

Table C-3. Boundary Scan Register Cells

Cell	Related Pin Name	Cell Type	Controlling Cell
0	*	control	
1	*	control	
2	RSTIN*	output2	2
3	RSTOUT*	output2	3
4	*	control	
5	*	control	
6	CELL_OUT	output2	
7	UOUTDAT-8	output3	0
8	UOUTDAT-7	output3	0
9	UOUTDAT-6	output3	0
10	UOUTDAT-5	output3	0
11	UOUTDAT-4	output3	0
12	UOUTDAT-3	output3	0
13	UOUTDAT-2	output3	0
14	UOUTDAT-1	output3	0
15	UOUTDAT-0	output3	0
16	WRU*	input	
17	RDU*	input	
18	RSTIN*	input	
19	RSTOUT*	input	
20	OHF*	output3	4
21	OHF*	input	
22	RDEN*	input	
23	OAF*	output3	4
24	OAF*	input	
25	IHF*	output3	4
26	IHF*	input	
27	IAF*	output3	4
28	IAF*	input	
29	MODE	input	
30	BICON	input	
31	WSTAT	input	
32	WCON	input	
33	RCON	input	
34	WREN*	input	
35	WRB*	input	
36	RDB*	input	
37	BSTAT-3	output3	5
38	BSTAT-3	input	
39	BSTAT-2	output3	5
40	BSTAT-2	input	
41	BSTAT-1	output3	5
42	BSTAT-1	input	
43	BSTAT-0	output3	5
44	BSTAT-0	input	
45	BIMODE	input	
46	BIDAT-31	output3	5
47	BIDAT-31	input	
48	BIDAT-30	output3	5
49	BIDAT-30	input	
50	BIDAT-29	output3	5
51	BIDAT-29	input	
52	BIDAT-28	output3	5
53	BIDAT-28	input	
54	BIDAT-27	output3	5
55	BIDAT-27	input	
56	BIDAT-26	output3	5
57	BIDAT-26	input	
58	BIDAT-25	output3	5
59	BIDAT-25	input	
60	BIDAT-24	output3	5
61	BIDAT-24	input	
62	BIDAT-23	output3	5
63	BIDAT-23	input	
64	BIDAT-22	output3	5
65	BIDAT-22	input	

Table C-3. Boundary Scan Register Cells

Cell	Related Pin Name	Cell Type	Controlling Cell
66	BIDAT-21	output3	5
67	BIDAT-21	input	
68	BIDAT-20	output3	5
69	BIDAT-20	input	
70	BIDAT-19	output3	5
71	BIDAT-19	input	
72	BIDAT-18	output3	5
73	BIDAT-18	input	
74	BIDAT-17	output3	5
75	BIDAT-17	input	
76	BIDAT-16	output3	5
77	BIDAT-16	input	
78	BIDAT-15	output3	5
79	BIDAT-15	input	
80	BIDAT-14	output3	5
81	BIDAT-14	input	
82	BIDAT-13	output3	5
83	BIDAT-13	input	
84	BIDAT-12	output3	5
85	BIDAT-12	input	
86	BIDAT-11	output3	5
87	BIDAT-11	input	
88	BIDAT-10	output3	5
89	BIDAT-10	input	
90	BIDAT-9	output3	5
91	BIDAT-9	input	
92	BIDAT-8	output3	5
93	BIDAT-8	input	
94	BIDAT-7	output3	5
95	BIDAT-7	input	
96	BIDAT-6	output3	5
97	BIDAT-6	input	
98	BIDAT-5	output3	5
99	BIDAT-5	input	
100	BIDAT-4	output3	5
101	BIDAT-4	input	
102	BIDAT-3	output3	5
103	BIDAT-3	input	
104	BIDAT-2	output3	5
105	BIDAT-2	input	
106	BIDAT-1	output3	5
107	BIDAT-1	input	
108	BIDAT-0	output3	5
109	BIDAT-0	input	
110	RTOUT*	output3	1
111	RTOUT*	input	
112	RTIN*	input	
113	UINDAT-8	input	
114	UINDAT-7	input	
115	UINDAT-6	input	
116	UINDAT-5	input	
117	UINDAT-4	input	
118	UINDAT-3	input	
119	UINDAT-2	input	
120	UINDAT-1	input	
121	UINDAT-0	input	
122	OAE*	output2	
123	IAE*	output2	
124	OFF*	output2	
125	OEF*	output2	
126	S-2	input	
127	S-1	input	
128	S-0	input	
129	IFF*	output2	
130	IEF*	output2	

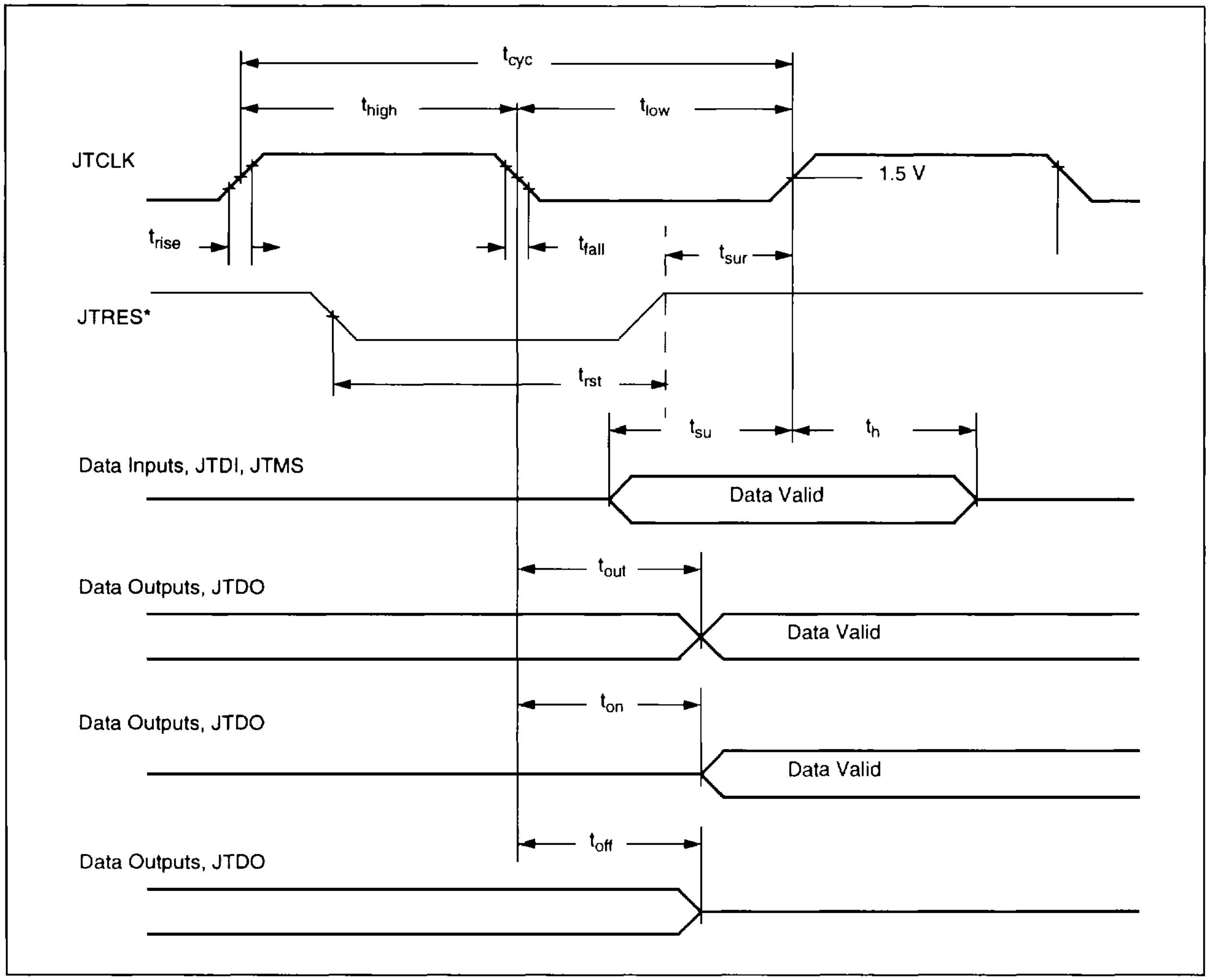
Electrical Characteristics

Timing Specifications

Table C-4. Timing Specifications

Symbol	Description	Min	Max	Unit
	JTCK Frequency	0	10	Mhz
t_{cyc}	JTCK Cycle	100	–	nsec
t_{high}	JTCK High Pulse Width	40	–	nsec
t_{low}	JTCK Low Pulse Width	40	–	nsec
t_{rise}	JTCK Rise	0	4	nsec
t_{fall}	JTCK Fall	0	4	nsec
t_{sur}	JTRES* Setup to JTCK Rising Edge	10	–	nsec
t_{rst}	JTRES* Active	1 t_{cyc}	–	
t_{su}	JTMS with respect to JTCK rising edge	1.0	–	nsec
t_h	JTMS with respect to JTCK rising edge	2.0	–	nsec
t_{su}	JTDI with respect to JTCK rising edge	1.0	–	nsec
t_h	JTDI with respect to JTCK rising edge	3.4	–	nsec
t_{out}	JTDO and Data Outputs Valid with respect to JTCK falling edge	–	15	nsec
t_{on}	JTDO and Data Outputs Float to Valid High	–	15	nsec
t_{off}	JTDO and Data Outputs Valid to Float High	–	15	nsec

Figure C-4. Timing Diagram



Boundary Scan Description Language (BSDL)

An electronic copy of this file can be obtained from a Brooktree Applications Engineer (1-800-2-BT-APPS or apps@brooktree.com).

```
-- BSDL File created/edited by AT&T BSD Editor
--
--BSDE: Revision: Rev. 1
--BSDE: Description: Bidirectional Cell Buffer

entity Bt8215 is

generic (PHYSICAL_PIN_MAP : string := "PQFP_100" );

port (
    BICON: in bit;
    BIDAT: inout bit_vector (0 to 31);
    BIMODE: in bit;
    BISTAT: inout bit_vector (0 to 3);
    CELL_OUT: out bit;
    GND: linkage bit_vector (0 to 5);
    IAE_NEG: out bit;
    IAF_NEG: inout bit;
    IEF_NEG: out bit;
    IFF_NEG: out bit;
    IHF_NEG: inout bit;
    MODE: in bit;
    OAE_NEG: out bit;
    OAF_NEG: inout bit;
    OEF_NEG: out bit;
    OFF_NEG: out bit;
    OHF_NEG: inout bit;
    RCON: in bit;
    RDB_NEG: in bit;
    RDEN_NEG: in bit;
    RDU_NEG: in bit;
    RSTIN_NEG: inout bit;
    RSTOUT_NEG: inout bit;
    RTIN_NEG: in bit;
    RTOUT_NEG: inout bit;
    S: in bit_vector (0 to 2);
    JTCK: in bit;
    JTDI: in bit;
    JTDO: out bit;
    JTMS: in bit;
    JTRES: in bit;
    UINDAT: in bit_vector (0 to 8);
    UOUTDAT: out bit_vector (0 to 8);
    VCC: linkage bit_vector (0 to 4);
    WCON: in bit;
    WRB_NEG: in bit;
    WREN_NEG: in bit;
    WRU_NEG: in bit;
    WSTAT: in bit
);

use STD_1149_1_1990.all;

attribute PIN_MAP of Bt8215 : entity is PHYSICAL_PIN_MAP;

constant PQFP_100: PIN_MAP_STRING:=
    "BICON:50," &
    "BIDAT:(24,25,26,29,30,31,32,33,34,35," &
    "36,37,38,39,41,42,52,55,56,57," &
    "58,59,60,61,62,63,64,65,67,68," &
    "69,70)," &
    "BIMODE:51," &
    "BISTAT:(73,74,75,76)," &
    "CELL_OUT:100," &
    "GND:(4,27,40,54,66,78)," &
    "IAE_NEG:7," &
    "IAF_NEG:81," &
    "IEF_NEG:1," &
    "IFF_NEG:2," &
    "IHF_NEG:82," &
    "MODE:99," &
    "OAE_NEG:8," &
    "OAF_NEG:83," &
    "OEF_NEG:5," &
    "OFF_NEG:6," &
    "OHF_NEG:85," &
    "RCON:79," &
    "RDB_NEG:48," &
    "RDEN_NEG:84," &
    "RDU_NEG:88," &
    "RSTIN_NEG:72," &
    "RSTOUT_NEG:71," &
    "RTIN_NEG:22," &
    "RTOUT_NEG:23," &
    "S:(19,20,21)," &
    "JTCK:43," &
    "JTDI:44," &
    "JTDO:45," &
    "JTMS:46," &
    "JTRES:47," &
    "UINDAT:(90,91,92,93,94,95,96,97,98)," &
    "UOUTDAT:(9,10,11,12,13,14,15,17,18)," &
    "VCC:(3,16,28,53,77)," &
    "WCON:86," &
    "WRB_NEG:49," &
    "WREN_NEG:87," &
    "WRU_NEG:89," &
    "WSTAT:80";

attribute TAP_SCAN_IN  of JTDI : signal is true;
attribute TAP_SCAN_OUT of JTDO : signal is true;
attribute TAP_SCAN_MODE of JTMS : signal is true;
attribute TAP_SCAN_CLOCK of JTCK : signal is (1.00e+06, BOTH);
attribute TAP_SCAN_RESET of JTRES : signal is true;

attribute INSTRUCTION_LENGTH of Bt8215 : entity is 2;

attribute INSTRUCTION_OPCODE of Bt8215 : entity is
    " BYPASS ( 01, 11)," &
     "EXTEST ( 00)," &
    " SAMPLE ( 10)" ;

attribute INSTRUCTION_CAPTURE of Bt8215 : entity is "01";

attribute REGISTER_ACCESS of Bt8215 : entity is
    " BYPASS ( BYPASS)," &
    " BOUNDARY ( EXTEST, SAMPLE)";

attribute BOUNDARY_CELLS of Bt8215 : entity is
    " BC_1, BC_4";

attribute BOUNDARY_LENGTH of Bt8215 : entity is 131;

attribute BOUNDARY_REGISTER of Bt8215 : entity is
    "   0 (BC_1, *, control, 1)," &
    "   1 (BC_1, *, control, 1)," &
    "   2 (BC_1, RSTIN_NEG, output2, 1, 2, 1, Weak1)," &
    "   3 (BC_1, RSTOUT_NEG, output2, 1, 3, 1, Weak1)," &
    "   4 (BC_1, *, control, 1)," &
    "   5 (BC_1, *, control, 1)," &
    "   6 (BC_1, CELL_OUT, output2, X)," &
    "   7 (BC_1, UOUTDAT(8), output3, X, 0, 1, Z)," &
    "   8 (BC_1, UOUTDAT(7), output3, X, 0, 1, Z)," &
    "   9 (BC_1, UOUTDAT(6), output3, X, 0, 1, Z)," &
    "  10 (BC_1, UOUTDAT(5), output3, X, 0, 1, Z)," &
    "  11 (BC_1, UOUTDAT(4), output3, X, 0, 1, Z)," &
    "  12 (BC_1, UOUTDAT(3), output3, X, 0, 1, Z)," &
    "  13 (BC_1, UOUTDAT(2), output3, X, 0, 1, Z)," &
    "  14 (BC_1, UOUTDAT(1), output3, X, 0, 1, Z)," &
    "  15 (BC_1, UOUTDAT(0), output3, X, 0, 1, Z)," &
    "  16 (BC_4, WRU_NEG, input, X)," &
    "  17 (BC_4, RDU_NEG, input, X)," &
    "  18 (BC_4, RSTIN_NEG, input, X)," &
    "  19 (BC_4, RSTOUT_NEG, input, X)," &
" 20 (BC_1, OHF_NEG, output3, X, 4, 1, Z)," &
" 21 (BC_4, OHF_NEG, input, X)," &
" 22 (BC_4, RDEN_NEG, input, X)," &
" 23 (BC_1, OAF_NEG, output3, X, 4, 1, Z)," &
" 24 (BC_4, OAF_NEG, input, X)," &
" 25 (BC_1, IHF_NEG, output3, X, 4, 1, Z)," &
" 26 (BC_4, IHF_NEG, input, X)," &
" 27 (BC_1, IAF_NEG, output3, X, 4, 1, Z)," &
" 28 (BC_4, IAF_NEG, input, X)," &
" 29 (BC_4, MODE, input, X)," &
" 30 (BC_4, BICON, input, X)," &
" 31 (BC_4, WSTAT, input, X)," &
" 32 (BC_4, WCON, input, X)," &
" 33 (BC_4, RCON, input, X)," &
" 34 (BC_4, WREN_NEG, input, X)," &
" 35 (BC_4, WRB_NEG, input, X)," &
" 36 (BC_4, RDB_NEG, input, X)," &
" 37 (BC_1, BISTAT(3), output3, X, 5, 1, Z)," &
" 38 (BC_4, BISTAT(3), input, X)," &
" 39 (BC_1, BISTAT(2), output3, X, 5, 1, Z)," &
" 40 (BC_4, BISTAT(2), input, X)," &
" 41 (BC_1, BISTAT(1), output3, X, 5, 1, Z)," &
" 42 (BC_4, BISTAT(1), input, X)," &
" 43 (BC_1, BISTAT(0), output3, X, 5, 1, Z)," &
" 44 (BC_4, BISTAT(0), input, X)," &
" 45 (BC_4, BIMODE, input, X)," &
" 46 (BC_1, BIDAT(31), output3, X, 5, 1, Z)," &
" 47 (BC_4, BIDAT(31), input, X)," &
" 48 (BC_1, BIDAT(30), output3, X, 5, 1, Z)," &
" 49 (BC_4, BIDAT(30), input, X)," &
" 50 (BC_1, BIDAT(29), output3, X, 5, 1, Z)," &
" 51 (BC_4, BIDAT(29), input, X)," &
" 52 (BC_1, BIDAT(28), output3, X, 5, 1, Z)," &
" 53 (BC_4, BIDAT(28), input, X)," &
" 54 (BC_1, BIDAT(27), output3, X, 5, 1, Z)," &
" 55 (BC_4, BIDAT(27), input, X)," &
" 56 (BC_1, BIDAT(26), output3, X, 5, 1, Z)," &
" 57 (BC_4, BIDAT(26), input, X)," &
" 58 (BC_1, BIDAT(25), output3, X, 5, 1, Z)," &
" 59 (BC_4, BIDAT(25), input, X)," &
" 60 (BC_1, BIDAT(24), output3, X, 5, 1, Z)," &
" 61 (BC_4, BIDAT(24), input, X)," &
" 62 (BC_1, BIDAT(23), output3, X, 5, 1, Z)," &
" 63 (BC_4, BIDAT(23), input, X)," &
" 64 (BC_1, BIDAT(22), output3, X, 5, 1, Z)," &
" 65 (BC_4, BIDAT(22), input, X)," &
" 66 (BC_1, BIDAT(21), output3, X, 5, 1, Z)," &
" 67 (BC_4, BIDAT(21), input, X)," &
" 68 (BC_1, BIDAT(20), output3, X, 5, 1, Z)," &
" 69 (BC_4, BIDAT(20), input, X)," &
" 70 (BC_1, BIDAT(19), output3, X, 5, 1, Z)," &
"  71 (BC_4, BIDAT(19), input, X)," &
"  72 (BC_1, BIDAT(18), output3, X, 5, 1, Z)," &
"  73 (BC_4, BIDAT(18), input, X)," &
"  74 (BC_1, BIDAT(17), output3, X, 5, 1, Z)," &
"  75 (BC_4, BIDAT(17), input, X)," &
"  76 (BC_1, BIDAT(16), output3, X, 5, 1, Z)," &
"  77 (BC_4, BIDAT(16), input, X)," &
"  78 (BC_1, BIDAT(15), output3, X, 5, 1, Z)," &
"  79 (BC_4, BIDAT(15), input, X)," &
"  80 (BC_1, BIDAT(14), output3, X, 5, 1, Z)," &
"  81 (BC_4, BIDAT(14), input, X)," &
"  82 (BC_1, BIDAT(13), output3, X, 5, 1, Z)," &
"  83 (BC_4, BIDAT(13), input, X)," &
"  84 (BC_1, BIDAT(12), output3, X, 5, 1, Z)," &
"  85 (BC_4, BIDAT(12), input, X)," &
"  86 (BC_1, BIDAT(11), output3, X, 5, 1, Z)," &
"  87 (BC_4, BIDAT(11), input, X)," &
"  88 (BC_1, BIDAT(10), output3, X, 5, 1, Z)," &
"  89 (BC_4, BIDAT(10), input, X)," &
"  90 (BC_1, BIDAT(9), output3, X, 5, 1, Z)," &
"  91 (BC_4, BIDAT(9), input, X)," &
"  92 (BC_1, BIDAT(8), output3, X, 5, 1, Z)," &
"  93 (BC_4, BIDAT(8), input, X)," &
"  94 (BC_1, BIDAT(7), output3, X, 5, 1, Z)," &
"  95 (BC_4, BIDAT(7), input, X)," &
"  96 (BC_1, BIDAT(6), output3, X, 5, 1, Z)," &
"  97 (BC_4, BIDAT(6), input, X)," &
"  98 (BC_1, BIDAT(5), output3, X, 5, 1, Z)," &
"  99 (BC_4, BIDAT(5), input, X)," &
" 100 (BC_1, BIDAT(4), output3, X, 5, 1, Z)," &
" 101 (BC_4, BIDAT(4), input, X)," &
" 102 (BC_1, BIDAT(3), output3, X, 5, 1, Z)," &
" 103 (BC_4, BIDAT(3), input, X)," &
" 104 (BC_1, BIDAT(2), output3, X, 5, 1, Z)," &
" 105 (BC_4, BIDAT(2), input, X)," &
" 106 (BC_1, BIDAT(1), output3, X, 5, 1, Z)," &
" 107 (BC_4, BIDAT(1), input, X)," &
" 108 (BC_1, BIDAT(0), output3, X, 5, 1, Z)," &
" 109 (BC_4, BIDAT(0), input, X)," &
" 110 (BC_1, RTOUT_NEG, output3, X, 1, 1, Z)," &
" 111 (BC_4, RTOUT_NEG, input, X)," &
" 112 (BC_4, RTIN_NEG, input, X)," &
" 113 (BC_4, UINDAT(8), input, X)," &
" 114 (BC_4, UINDAT(7), input, X)," &
" 115 (BC_4, UINDAT(6), input, X)," &
" 116 (BC_4, UINDAT(5), input, X)," &
" 117 (BC_4, UINDAT(4), input, X)," &
" 118 (BC_4, UINDAT(3), input, X)," &
" 119 (BC_4, UINDAT(2), input, X)," &
" 120 (BC_4, UINDAT(1), input, X)," &
" 121 (BC_4, UINDAT(0), input, X)," &
```

```
    " 122 (BC_1, OAE_NEG, output2, X)," &
    " 123 (BC_1, IAE_NEG, output2, X)," &
    " 124 (BC_1, OFF_NEG, output2, X)," &
    " 125 (BC_1, OEF_NEG, output2, X)," &
    " 126 (BC_4, S(2), input, X)," &
    " 127 (BC_4, S(1), input, X)," &
    " 128 (BC_4, S(0), input, X)," &
    " 129 (BC_1, IFF_NEG, output2, X)," &
    " 130 (BC_1, IEF_NEG, output2, X)";

end Bt8215;
```

The
Chips
Behind
The
Network™

Brooktree

Brooktree Corporation
9868 Scranton Road
San Diego, CA 92121-3707
(619) 452-7580
1 (800) 2-BT-APPS
FAX (619) 452-1249
Internet: apps@brooktree.com
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