

GD54/74LS646

OCTAL BUS TRANSCEIVERS AND REGISTERS

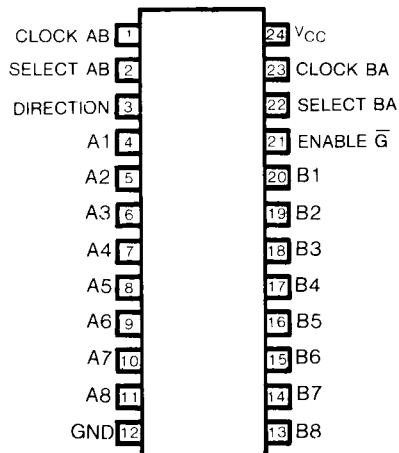
Features

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs

Description

These devices consist of bus transceiver circuits with 3-state circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control \bar{G} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in the B register and/or B data may be stored in the A register.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package

When an output function is disabled, the input function is still enabled, and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

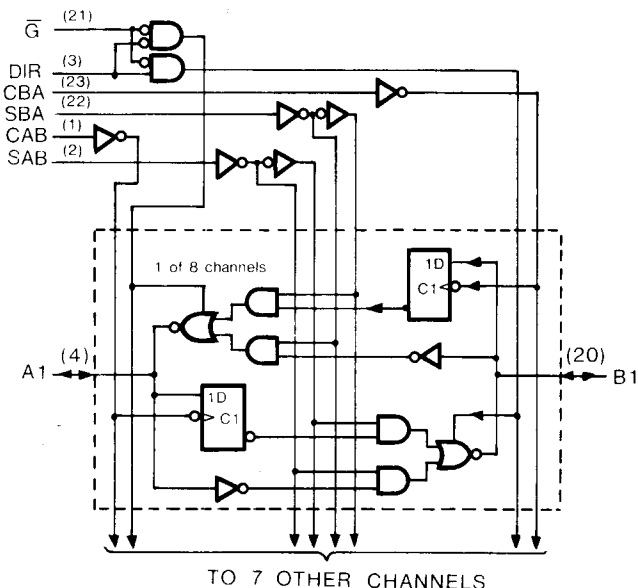
Function Table

INPUTS				DATA I/O		OPERATION OR FUNCTION
\bar{G}	DIR	CAB	CBA	SAB	SBA	'LS646
H	X	H or L	H or L	X	X	Isolation
H	X	↑	↑	X	X	Store A and B Data
L	L	X	X	X	L	Real Time B Data to A Bus
L	L	X	X	X	H	Stored B Data to A Bus
L	H	X	X	L	X	Real Time A Data to B Bus
L	H	H or L	X	H	X	Stored A Data to B Bus

H=high level L=low level X=Irrelevant ↑=low-to-high-level transition

- The data output function may be enabled or disabled by various signals at the \bar{G} and DIR Inputs. Data input function are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Function Block Diagram



Absolute Maximum Ratings at 25°C Free-air Temperature (Unless Otherwise Noted)

- Supply voltage, V_{CC} (see Note 1) 7V
- Input voltage (Control Inputs) 7V
- Off-state Output Voltage (A and B Ports) 5.5V
- Operating free-air temperature range 54LS -55°C to 125°C
- 74LS 0°C to 70°C
- Storage temperature range -65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			-12	mA
		74			-15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
t_w	Width of any input pulse		20			ns
t_{su}	Clear inactive-state set up time	Bus to clock	20			ns
t_{th}	Data hold time	Bus from clock	0			ns
T_A	Operating free-air temperature	54	-55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		TYP (Note 1)		UNIT
				MIN	MAX	
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage			54	0.5	V
				74	0.6	
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC} = \text{Min}$		54	0.1 0.4	V
				74	0.2 0.4	
V_{OH}	High-level output voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min}$ $V_{IL} = \text{Max}$	$I_{OH} = -3 \text{ mA}$	54, 74	2.4 3.4	V
			$I_{OH} = \text{Max}$	54, 74	2	
V_{OL}	Low-level output voltage	$V_{CC} = \text{Min}$ $V_{IL} = \text{Max}$ $V_{IH} = \text{Min}$	$I_{OL} = 12 \text{ mA}$	54, 74	0.25 0.4	V
			$I_{OL} = 24 \text{ mA}$	74	0.35 0.5	
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{Max}, V_O = 2.7 \text{ V}$			-20	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{Max}, V_O = 0.4 \text{ V}$			-400	μA
I_I	Input current at maximum input voltage	A or B	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$	$V_I = 5.5 \text{ V}$		0.1
		All others		$V_I = 7 \text{ V}$		0.1
I_{IH}	High-level input current	$V_{CC} = \text{Max}, V_I = 2.7 \text{ V}$			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			-0.4	mA
I_{OS}	Short-circuit output current	$V_{CC} = \text{Max}$ (Note 2)			-40	-255
I_{CC}	Supply Current	Output high	$V_{CC} = 5.25 \text{ V}$ Outputs open		91	145
		Outputs low			103	165
		Outputs at Hi-z			103	165

Note 1: All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LS646		UNIT
				MIN	TYP MAX	
t_{PLH}	Clock	Bus	$R_L = 667 \Omega$ $C_L = 45 \text{ pF}$	15	25	ns
t_{PHL}				23	35	ns
t_{PLH}	Bus	Bus		12	18	ns
t_{PHL}				13	20	ns
t_{PLH}	Select, with bus input high†	Bus		26	40	ns
t_{PHL}				21	35	ns
t_{PLH}	Select, with bus input low†	Bus		33	50	ns
t_{PHL}				14	25	ns
t_{PZH}	Enable	Bus		33	55	ns
t_{PZL}				42	65	ns
t_{PZH}	Direction	Bus	28	45	ns	
t_{PZL}			39	60	ns	
t_{PHZ}	Enable	Bus	$R_L = 667 \Omega$ $C_L = 5 \text{ pF}$	23	35	ns
t_{PLZ}				22	35	ns
t_{PHZ}	Direction	20		30	ns	
t_{PLZ}		19		30	ns	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.