TM4EJ64KPU, TM4EJ64NPU, TM4FJ64KPU, TM4FJ64NPU, 4194304 BY 64-BIT
TM8EJ64KPU, TM8EJ64NPU, TM8FJ64KPU, TM8FJ64NPU, 8388608 BY 64-BIT
EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM

SMMS693A − AUGUST 1997 − REVISED NOVEMBER 1997

- **Organization**
  - **TM4xJ64xPU-xx . . . 4194304 × 64 Bits**
  - **TM8xJ64xPU-xx . . . 8388608 × 64 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **JEDEC 144-Pin Small-Outline Dual-In-Line Memory Module (SODIMM) Without Buffer for Use With Socket**
- **TM4xJ64xPU-xx — Utilizes Four 64M-Bit High-Speed (4M×16-Bit) Dynamic RAMs**
- **TM4xJ64xPU-xx — Utilizes Eight 64M-Bit High-Speed (4M×16-Bit) Dynamic RAMs**
- **High-Speed, Low-Noise LVTTL Interface**
- **High-Reliability 50-Lead 400-Mil-Wide Surface-Mount Thin Small-Outline Package (TSOP) (DGE Suffix)**
- **3-State Output**
- **Gold-Plated Contacts**
- **Long Refresh Periods:**
  - **TMxEJ64KPU: 64 ms (4096 Cycles)**
  - **TMxEJ64NPU: 64 ms (8192 Cycles)**
  - **TMxFJ64KPU: 128 ms (4096 Cycles)**
  - **TMxFJ64NPU: 128 ms (8192 Cycles)**
- **Extended Data Out (EDO) Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Serial Presence-Detect (SPD) Using EEPROM**
- **Ambient Temperature Range 0°C to 70°C**
- **Performance Ranges**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	EDO CYCLE t_{HPC} (MIN)
'xxJ64xPU-40	40 ns	11 ns	20 ns	16 ns
'xxJ64xPU-50	50 ns	13 ns	25 ns	20 ns
'xxJ64xPU-60	60 ns	15 ns	30 ns	25 ns

PRODUCT PREVIEW

description

The TM4xJ64KPU is a 32M-byte, 144-pin, small-outline dual-in-line memory module (SODIMM). The SODIMM is composed of four TMS465169/P, 4194304 × 16-bit 4K normal or low-power battery-backup refresh EDO dynamic random-access memory (DRAM) devices, each in a 400-mil, 50-pin plastic thin small-outline package (TSOP) (DGE suffix) package mounted on a substrate with decoupling capacitors. See the TMS465169/P data sheet (literature number SMHS566).

The TM4xJ64NPU is a 32M-byte, 144-pin SODIMM. The SODIMM is composed of four TMS464169/P, 4194304 × 16-bit 8K normal or low-power battery-backup refresh EDO DRAMs, each in a 400-mil, 50-pin plastic TSOP (DGE suffix) mounted on a substrate with decoupling capacitors. See the TMS464169/P data sheet (literature number SMHS566).

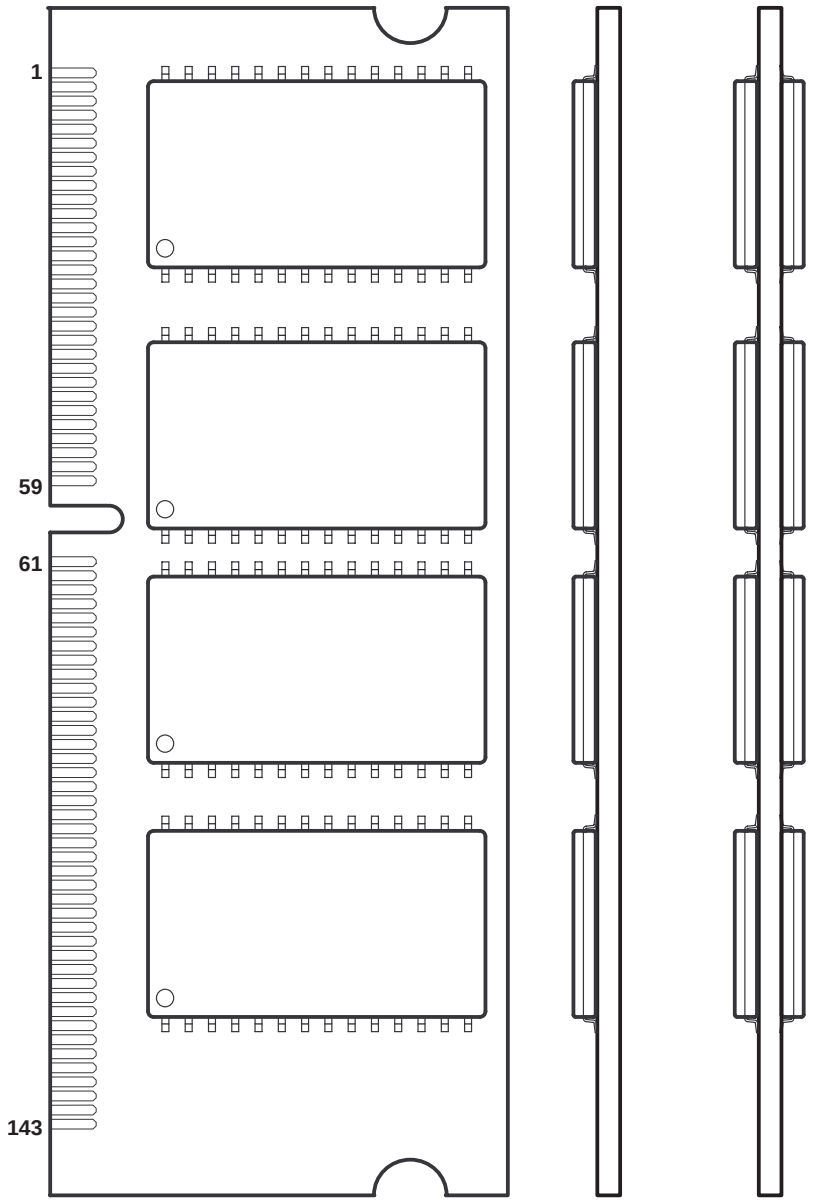
The TM8xJ64KPU is a 64M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS465169/P, 4194304 × 16-bit 4K normal or low-power battery-backup refresh EDO DRAMs, each in a 400-mil, 50-pin plastic TSOP (DGE suffix) mounted on a substrate with decoupling capacitors.

The TM8xJ64NPU is a 64M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS464169/P, 4194304 × 16-bit 8K normal or low-power battery-backup refresh EDO DRAMs, each in a 400-mil, 50-pin plastic TSOP (DGE suffix) mounted on a substrate with decoupling capacitors.

operation

The TM4xJ64xPU operates as four TMS46x169/Ps that are connected as shown in the TMxxJ64xPU functional block diagram. The TM8xJ64xPU operates as eight TMS46x169/Ps that are connected as shown in the TMxxJ64xPU functional block diagram.

DUAL-IN-LINE MEMORY MODULE (TOP VIEW) | **TM4xJ64xPU (SIDE VIEW)** | **TM8xJ64xPU (SIDE VIEW)**



PIN NOMENCLATURE − TMxxJ64KPU

A[0:11]	Row Address Inputs
A[0:9]	Column Address Inputs
$\overline{\text{DQ}}$[0:63]	Data In/Data Out
$\overline{\text{CAS}}$[0:7]	Column-Address Strobe
$\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$	Row-Address Strobe
$\overline{\text{WE0}}$	Write Enable
$\overline{\text{OE0}}$	Output Enable
SDA	Serial PD Address/Data
SCL	Serial PD Clock
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

PIN NOMENCLATURE − TMxxJ64NPU

A[0:12]	Row Address Inputs
A[0:8]	Column Address Inputs
$\overline{\text{DQ}}$[0:63]	Data In/Data Out
$\overline{\text{CAS}}$[0:7]	Column-Address Strobe
$\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$	Row-Address Strobe
$\overline{\text{WE0}}$	Write Enable
$\overline{\text{OE0}}$	Output Enable
SDA	Serial PD Address/Data
SCL	Serial PD Clock
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

Pin Assignments

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	37	DQ8	73	$\overline{OE0}$	109	A9
2	V_{SS}	38	DQ40	74	NC	110	A12
3	DQ0	39	DQ9	75	V_{SS}	111	A10
4	DQ32	40	DQ41	76	V_{SS}	112	NC
5	DQ1	41	DQ10	77	NC	113	V_{DD}
6	DQ33	42	DQ42	78	NC	114	V_{DD}
7	DQ2	43	DQ11	79	NC	115	$\overline{CAS2}$
8	DQ34	44	DQ43	80	NC	116	$\overline{CAS6}$
9	DQ3	45	V_{DD}	81	V_{DD}	117	$\overline{CAS3}$
10	DQ35	46	V_{DD}	82	V_{DD}	118	$\overline{CAS7}$
11	V_{DD}	47	DQ12	83	DQ16	119	V_{SS}
12	V_{DD}	48	DQ44	84	DQ48	120	V_{SS}
13	DQ4	49	DQ13	85	DQ17	121	DQ24
14	DQ36	50	DQ45	86	DQ49	122	DQ56
15	DQ5	51	DQ14	87	DQ18	123	DQ25
16	DQ37	52	DQ46	88	DQ50	124	DQ57
17	DQ6	53	DQ15	89	DQ19	125	DQ26
18	DQ38	54	DQ47	90	DQ51	126	DQ58
19	DQ7	55	V_{SS}	91	V_{SS}	127	DQ27
20	DQ39	56	V_{SS}	92	V_{SS}	128	DQ59
21	V_{SS}	57	NC	93	DQ20	129	V_{DD}
22	V_{SS}	58	NC	94	DQ52	130	V_{DD}
23	$\overline{CAS0}$	59	NC	95	DQ21	131	DQ28
24	$\overline{CAS4}$	60	NC	96	DQ53	132	DQ60
25	$\overline{CAS1}$	61	NC	97	DQ22	133	DQ29
26	$\overline{CAS5}$	62	NC	98	DQ54	134	DQ61
27	V_{DD}	63	V_{DD}	99	DQ23	135	DQ30
28	V_{DD}	64	V_{DD}	100	DQ55	136	DQ62
29	A0	65	NC	101	V_{DD}	137	DQ31
30	A3	66	NC	102	V_{DD}	138	DQ63
31	A1	67	$\overline{WE0}$	103	A6	139	V_{SS}
32	A4	68	NC	104	A7	140	V_{SS}
33	A2	69	$\overline{RAS0}$	105	A8	141	SDA
34	A5	70	NC	106	A11	142	SCL
35	V_{SS}	71	$\overline{RAS1}$	107	V_{SS}	143	V_{DD}
36	V_{SS}	72	NC	108	V_{SS}	144	V_{DD}

PRODUCT PREVIEW

small-outline dual-in-line memory module and components

The small-outline dual-in-line memory module and components include:

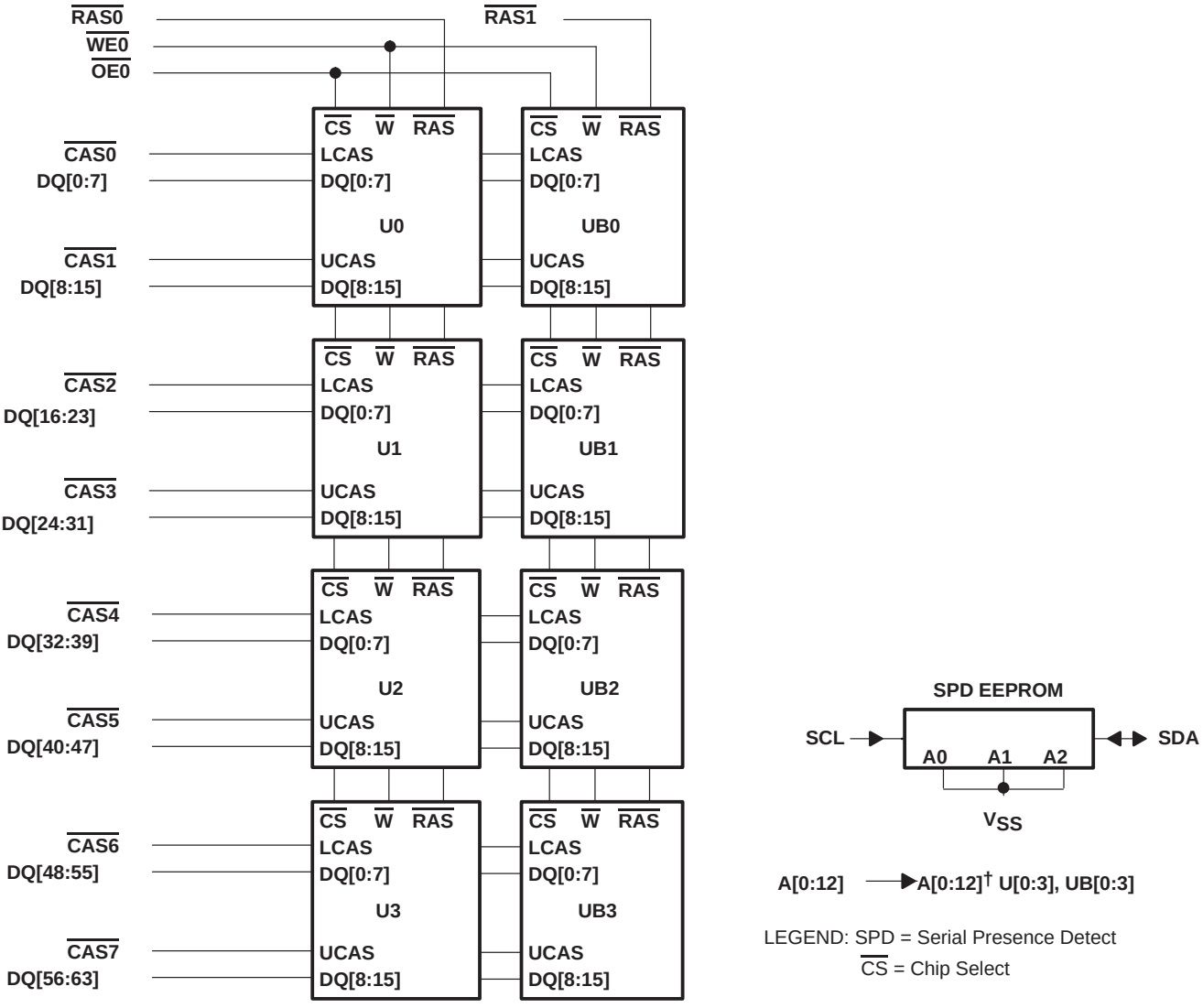
- PC substrate: 1,10 ± 0,1 mm (0.04 inch) nominal thickness
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

The following table shows the SODIMM modules and devices (Ux/UBx) that are used.

Table 1. Component Table

MODULE	DEVICES USED
TM4xJ64xPU	U[0:3]
TM8xJ64xPU	U[0:3], UB[0:3]

functional block diagram for the TMxxJ64xPU



† A12 is not used in TM4xJ64KPU, TM8xP64KPU

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . − 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM4xJ64xPU . . . . . 4 W
TM8xJ64xPU . . . . . 8 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . − 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH}-SPD	High-level input voltage for the SPD device	2		5.5	V
V_{IL}	Low-level input voltage	−0.3		0.8	V
T_A	Ambient temperature	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TM4xJ64KPU

PARAMETER		TEST CONDITIONS†		'4xJ64KPU-40 MIN	'4xJ64KPU-40 MAX	'4xJ64KPU-50 MIN	'4xJ64KPU-50 MAX	'4xJ64KPU-60 MIN	'4xJ64KPU-60 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD}−0.2		V_{DD}−0.2		V_{DD}−0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CASx}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			640		520		440	mA
I_{CC2}	Average standby current	V_{IH} = 2 V LVTTL), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			4		4		4	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high	'4EJ64KPU		2		2		2	mA
			'4FJ64KPU		.6		.6		.6	
I_{CC3}§	$\overline{RASx}$-only refresh, average refresh curren	V_{DD} = 3.6 V, $\overline{RASx}$ cycling, Minimum cycle, $\overline{CASx}$ high			640		520		440	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, $\overline{RASx}$ low, t_{HPC} = MIN, $\overline{CASx}$ cycling			600		480		400	mA
I_{CC5}	Average CBR refresh current	V_{DD} = 3.6 V, Minimum cycle, $\overline{RASx}$ low after $\overline{CASx}$ low			640		520		440	mA
I_{CC6}#	Average self-refresh current	$\overline{CASx}$ < 0.2 V, $\overline{RASx}$ < 0.2 V, Measured after t_{RASS} min			1.2		1.2		1.2	mA
I_{CC10}#	Average battery back-up operating current, CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{DD} − 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{WE0}$ and $\overline{OE0}$ = V_{IH}, Address and data stable			1.6		1.6		1.6	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RASx}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}
# For TM4FJ64KPU only

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM4xJ64NPU

PARAMETER		TEST CONDITIONS†		'4xJ64NPU-40		'4xJ64NPU-50		'4xJ64NPU-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD}−0.2		V_{DD}−0.2		V_{DD}−0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CASx}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			540		440		400	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			4		4		4	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high	'4EJ64NPU		2		2		2	mA
			'4FJ64NPU		.6		.6		.6	
I_{CC3}§	$\overline{RASx}$-only refresh, average refresh curren	V_{DD} = 3.6 V, $\overline{RASx}$ cycling, Minimum cycle, $\overline{CASx}$ high			540		440		400	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, $\overline{RASx}$ low, t_{HPC} = MIN, $\overline{CASx}$ cycling			560		440		360	mA
I_{CC5}	Average CBR refresh current	V_{DD} = 3.6 V, Minimum cycle, $\overline{RASx}$ low after $\overline{CASx}$ low			640		520		440	mA
I_{CC6}#	Average self-refresh current	$\overline{CASx}$ < 0.2 V, $\overline{RASx}$ < 0.2 V, Measured after t_{RASS} min			1.2		1.2		1.2	mA
I_{CC10}#	Average battery back-up operating current, CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{DD} − 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{WE0}$ and $\overline{OE0}$ = V_{IH}, Address and data stable			1.6		1.6		1.6	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RASx}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}
# For TM4FJ64NPU only

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM8xJ64KPU

PARAMETER		TEST CONDITIONS†		'8xJ64KPU-40		'8xJ64KPU-50		'8xJ64KPU-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD}−0.2		V_{DD}−0.2		V_{DD}−0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CAS}$x high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			644		524		444	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high			8		8		8	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high	'8EJ64KPU		4		4		4	mA
			'8FJ64KPU		1.2		1.2		1.2	
I_{CC3}§	$\overline{RAS}$x-only refresh, average refresh curren	V_{DD} = 3.6 V, $\overline{RAS}$x cycling, Minimum cycle, $\overline{CAS}$x high			644		524		444	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, $\overline{RAS}$x low, t_{HPC} = MIN, $\overline{CAS}$x cycling			604		484		404	mA
I_{CC5}	Average CBR refresh current	V_{DD} = 3.6 V, Minimum cycle, $\overline{RAS}$x low after $\overline{CAS}$x low			644		524		444	mA
I_{CC6}#	Average self-refresh current	$\overline{CAS}$x < 0.2 V, $\overline{RAS}$x < 0.2 V, Measured after t_{RASS} min			2.4		2.4		2.4	mA
I_{CC10}#	Average battery back-up operating current, CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{DD} − 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{WE0}$ and $\overline{OE0}$ = V_{IH}, Address and data stable			3.2		3.2		3.2	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$x = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}
# For TM8FJ64KPU only

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM8xJ64NPU

PARAMETER		TEST CONDITIONS†		'8xJ64NPU-40		'8xJ64NPU-50		'8xJ64NPU-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD}−0.2		V_{DD}−0.2		V_{DD}−0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CAS}$x high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			544		444		404	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high			8		8		8	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high	'8EJ64NPU		4		4		4	mA
			'8FJ64NPU		1.2		1.2		1.2	
I_{CC3}§	$\overline{RAS}$x-only refresh, average refresh curren	V_{DD} = 3.6 V, $\overline{RAS}$x cycling, Minimum cycle, $\overline{CAS}$x high			544		444		404	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, $\overline{RAS}$x low, t_{HPC} = MIN, $\overline{CAS}$x cycling			564		444		364	mA
I_{CC5}	Average CBR refresh current	V_{DD} = 3.6 V, Minimum cycle, $\overline{RAS}$x low after $\overline{CAS}$x low			644		524		444	mA
I_{CC6}#	Average self-refresh current	$\overline{CAS}$x < 0.2 V, $\overline{RAS}$x < 0.2 V, Measured after t_{RASS} min			2.4		2.4		2.4	mA
I_{CC10}#	Average battery back-up operating current, CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{DD} − 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{WE0}$ and $\overline{OE0}$ = V_{IH}, Address and data stable			3.2		3.2		3.2	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}
# For TM8FJ64NPU only

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		'4xJ64xPU		'8xJ64xPU		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0−A12		22		42	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE0}$		16		30	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CASx}$		9		9	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RASx}$		16		16	pF
$C_{i(W)}$	Input capacitance, $\overline{WE0}$		16		30	pF
C_o	Output capacitance		9		16	pF
$C_{i/o(SDA)}$	Input/output capacitance, SDA input		9		9	pF
$C_{i(SPD)}$	Input capacitance,SPD inputs (except SDA)		7		7	pF

NOTE 2: V_{DD} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 3)

PARAMETER		'xxJ64xPU-40		'xxJ64xPU-50		'xxJ64xPU-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		20		25		30	ns
t_{CAC}	Access time from $\overline{CASx}$ (see Note 4)		11		13		15	ns
t_{CPA}	Access time from $\overline{CASx}$ precharge (see Note 4)		22		28		35	ns
t_{RAC}	Access time from $\overline{RASx}$ (see Note 4)		40		50		60	ns
t_{OEA}	Access time from $\overline{OE0}$ (see Note 4)		11		13		15	ns
t_{CLZ}	Delay time, $\overline{CASx}$ to output in the low-impedance state	0		0		0		ns
t_{OEZ}	Output buffer turnoff delay from $\overline{OE0}$ (see Note 5)	3	11	3	13	3	15	ns
t_{REZ}	Output buffer turnoff delay from $\overline{RASx}$ (see Note 5)	3	11	3	13	3	15	ns
t_{CEZ}	Output buffer turnoff delay from $\overline{CASx}$ (see Note 5)	3	11	3	13	3	15	ns
t_{WEZ}	Output buffer turnoff delay from $\overline{WE0}$ (see Note 5)	3	11	3	13	3	15	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
4. Access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. The MAX specifications of t_{REZ}, t_{CEZ}, t_{WEZ} and t_{OEZ} are specified when the output is no longer driven. Data-in should not be driven until one of the applicable maximum specifications is satsified.

EDO timing requirements (see Note 3)

		'xxJ64xPU-40		'xxJ64xPU-50		'xxJ64xPU-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	16		20		25		ns
t_{PRWC}	Cycle time, EDO read-write	47		57		68		ns
t_{CSH}	Delay time, $\overline{RASx}$ active to $\overline{CASx}$ precharge	32		40		48		ns
t_{CHO}	Hold time, $\overline{OE0}$ from $\overline{CASx}$	5		5		5		ns
t_{DOH}	Hold time, output from $\overline{CASx}$ active	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{CASx}$ active (see Note 6)	6	10000	8	10000	10	10000	ns
t_{WPE}	Pulse duration, $\overline{WE0}$ (output disable only)	5		5		5		ns
t_{CP}	Pulse duration, $\overline{CASx}$ precharge	6		8		10		ns
t_{OCH}	Setup time, $\overline{OE0}$ before $\overline{CASx}$	5		5		5		ns
t_{OEP}	Precharge time, $\overline{OE0}$ (output disable only)	5		5		5		ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
6. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.

ac timing requirements (see Note 3)

		’xxJ64xPU-40		’xxJ64xPU-50		’xxJ64xPU-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	69		84		104		ns
t_{RWC}	Cycle time, read-write	92		111		135		ns
t_{RASP}	Pulse duration, $\overline{RAS}$x active, page mode (see Note 7)	40	100 000	50	100 000	60	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$x active, nonpage mode (see Note 7)	40	10 000	50	10 000	60	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$x precharge	25		30		40		ns
t_{WP}	Pulse duration, write command	6		8		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 8)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$x precharge	6		8		10		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$x precharge	6		8		10		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$x active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, write before $\overline{RAS}$x active (CBR refresh only)	5		5		5		ns
t_{CSR}	Setup time, $\overline{CAS}$x referenced to $\overline{RAS}$x (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	6		8		10		ns
t_{DH}	Hold time, data in (see Note 8)	6		8		10		ns
t_{RAH}	Hold time, row address	6		8		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$x (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$x (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$x active (early-write only)	6		8		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$x active from $\overline{CAS}$x precharge	22		28		35		ns
t_{OEH}	Hold time, $\overline{OE0}$ command	11		13		15		ns
t_{ROH}	Hold time, $\overline{RAS}$x referenced to $\overline{OE0}$	6		8		10		ns
t_{WRH}	Hold time, write after $\overline{RAS}$x active (CBR refresh only)	6		8		10		ns
t_{CHS}	Hold time, $\overline{CAS}$x active after $\overline{RAS}$x precharge (self-refresh)	− 50		− 50		− 50		ns
t_{AWD}	Delay time, column address to write command (read-write only)	35		42		49		ns
t_{CHR}	Delay time, $\overline{CAS}$x referenced to $\overline{RAS}$x (CBR refresh only)	6		8		10		ns
t_{CRP}	Delay time, $\overline{CAS}$x precharge to $\overline{RAS}$x	5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$x to write command (read-write operation only)	26		30		34		ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. Referenced to the later of $\overline{CAS}$x or $\overline{WE0}$ in write operations
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

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ac timing requirements (see Note 3) (continued)

			’xxJ64xPU-40		’xxJ64xPU-50		’xxJ64xPU-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{OED}	Delay time, $\overline{OE0}$ to data in		11		13		15		ns
t_{RAD}	Delay time, $\overline{RAS}$x to column address (see Note 10)		8	20	10	25	12	30	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$x precharge		20		25		30		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$x precharge		12		15		18		ns
t_{RCD}	Delay time, $\overline{RAS}$x to $\overline{CAS}$x (see Note 10)		10	29	12	37	14	45	ns
t_{RPC}	Delay time, $\overline{RAS}$x precharge to $\overline{CAS}$x		5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$x active to $\overline{RAS}$x precharge		6		8		10		ns
t_{RWD}	Delay time, $\overline{RAS}$x active to write command (read-write only)		55		67		79		ns
t_{CPW}	Delay time, $\overline{CAS}$x precharge to write command (read-write only)		37		45		54		ns
t_{RASS}	Pulse duration, $\overline{RAS}$x active, self-refresh (see Note 11)		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$x precharge after self refresh		70		90		110		ns
t_{REF}	Refresh time interval	’xEJ64xPU		64		64		64	ms
		’xFJ64xPU		128		128		128	ms
t_T	Transition time		1	50	1	50	1	50	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
10. The maximum value is specified only to assure access time.
11. During the period of 10 µs ≤ t_{RASS} ≤ 100 µs, the device is in transition state from normal operational mode to self-refresh mode.

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serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, DRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 2—TM4EJ64KPU Table 3—TM4EJ64NPU
Table 4—TM8EJ64KPU Table 5—TM8EJ64NPU
Table 6—TM4FJ64KPU Table 7—TM4FJ64NPU
Table 8—TM8FJ64KPU Table 9—TM8FJ64NPU

Table 2. Serial-Presence-Detect Data for the TM4EJ64KPU

BYTE NO.	FUNCTION DESCRIBED	’4EJ64KPU-40		’4EJ64KPU-50		’4EJ64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0−62	38	26h	50	32h	62	3Eh

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serial presence detect (continued)

Table 2. Serial-Presence-Detect Data for the TM4EJ64KPU (Continued)

BYTE NO.	FUNCTION DESCRIBED	'4EJ64KPU-40		'4EJ64KPU-50		'4EJ64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
64−71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer's part number	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

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serial presence detect (continued)

Table 3. Serial-Presence-Detect Data for the TM4EJ64NPU

BYTE NO.	FUNCTION DESCRIBED	’4EJ64NPU-40		’4EJ64NPU-50		’4EJ64NPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	13	0Dh	13	0Dh	13	0Dh
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0−62	38	26h	50	32h	62	3Eh
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

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serial presence detect (continued)

Table 4. Serial-Presence-Detect Data for the TM8EJ64KPU

BYTE NO.	FUNCTION DESCRIBED	'8EJ64KPU-40		'8EJ64KPU-50		'8EJ64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{RAS}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{CAS}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0−62	39	27h	51	33h	63	3Fh
64−71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 5. Serial-Presence-Detect Data for the TM8EJ64NPU

BYTE NO.	FUNCTION DESCRIBED	8EJ64NPU-40		’8EJ64NPU-50		’8EJ64NPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	13	0Dh	13	0Dh	13	0Dh
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0−62	39	27h	51	33h	63	3Fh
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

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serial presence detect (continued)

Table 6. Serial-Presence-Detect Data for the TM4FJ64KPU

BYTE NO.	FUNCTION DESCRIBED	'4FJ64KPU-40		'4FJ64KPU-50		'4FJ64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 banks	01h	1 banks	01h	1 banks	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{RAS}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{CAS}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0−62	166	A6h	178	B2h	190	BEh
64−71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 7. Serial-Presence-Detect Data for the TM4FJ64NPU

BYTE NO.	FUNCTION DESCRIBED	’4FJ64NPU-40		’4FJ64NPU-50		’4FJ64NPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	13	0Dh	13	0Dh	13	0Dh
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0−62	166	A6h	178	B2h	190	BEh
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

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serial presence detect (continued)

Table 8. Serial-Presence-Detect Data for the TM8FJ64KPU

BYTE NO.	FUNCTION DESCRIBED	'8FJ64KPU-40		'8FJ64KPU-50		'8FJ64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{RAS}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{CAS}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0−62	167	A7h	179	B3h	191	BFh
64−71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 9. Serial-Presence-Detect Data for the TM8FJ64NPU

BYTE NO.	FUNCTION DESCRIBED	8FJ64NPU-40		’8FJ64NPU-50		’8FJ64NPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	13	0Dh	13	0Dh	13	0Dh
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{RAS}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{CAS}$x access time of module	t_{CAC} = 19 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h	15.6 µs/self-refresh	80h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 − 62	167	A7h	179	B3h	191	BFh
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

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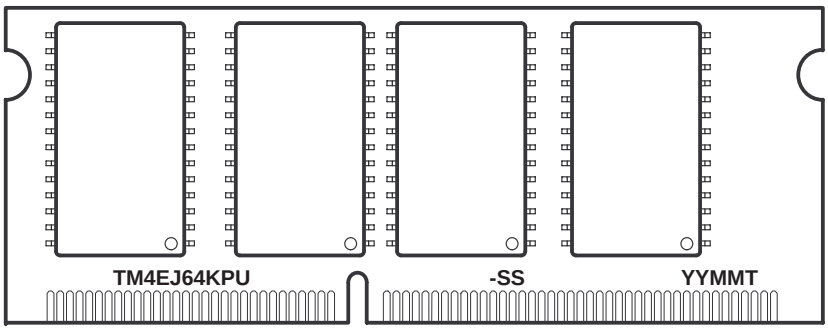
device symbolization (TM4EJ64KPU illustrated)



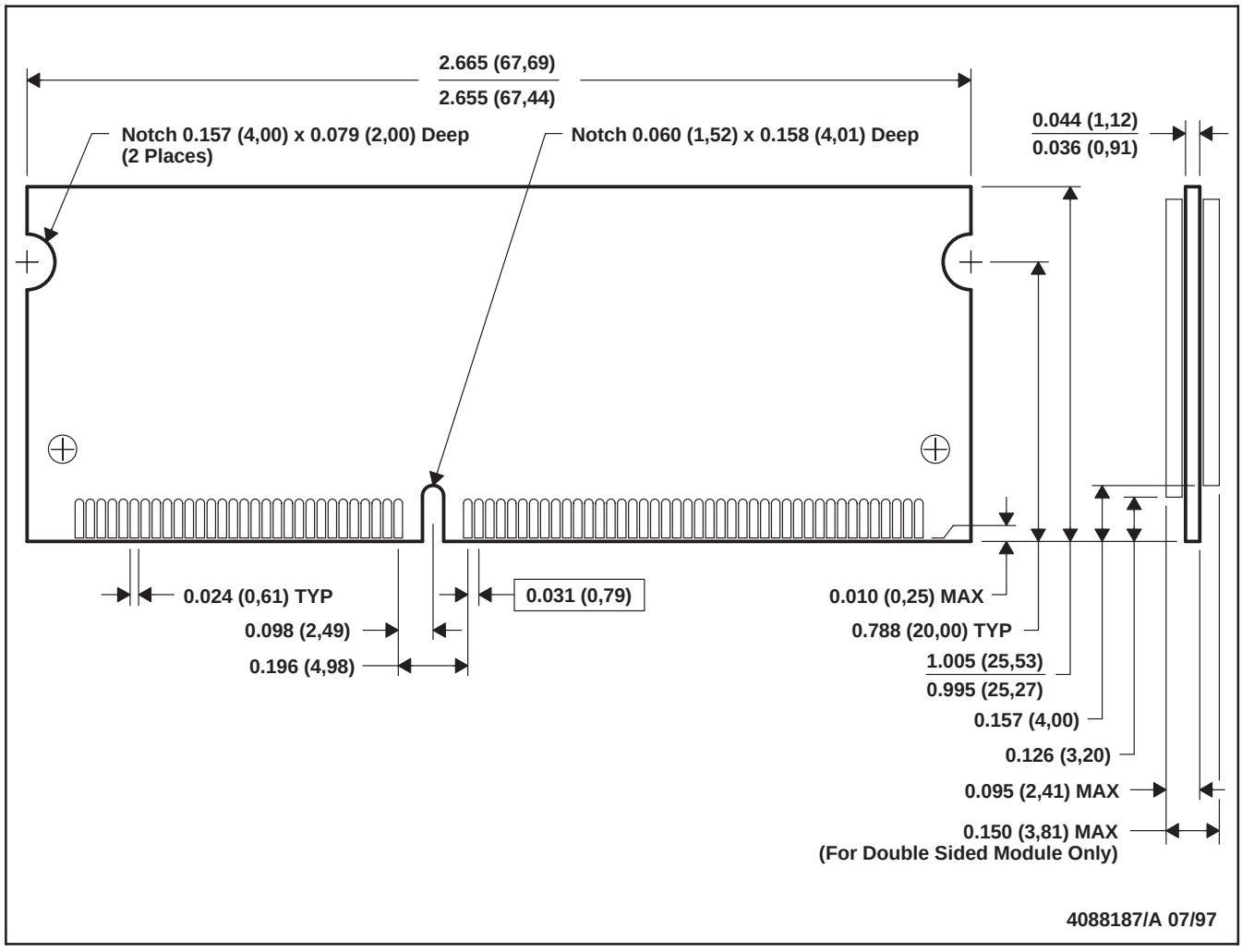
YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTES: A. Location of symbolization may vary.

PRODUCT PREVIEW

MECHANICAL DATA

BDM (R-SODIMM-N144) **SMALL OUTLINE DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-190

PRODUCT PREVIEW

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