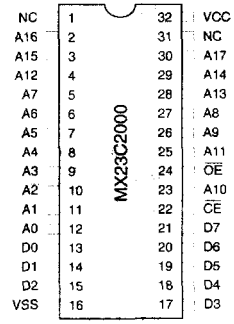
2M-BIT MASK ROM (8 BIT OUTPUT)

FEATURES

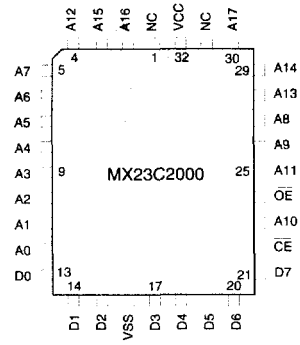
- Bit organization
  - 256K x 8 (byte mode)
- Fast access time
  - Random access: 70ns (max.)
- Current
  - Operating: 40mA
  - Standby: 100uA
  - (50μA for PLCC)
- Supply voltage
  - 5V ± 10%
- Package
  - 32 pin PDIP (600 mil)
  - 32 pin PLCC
  - 32 pin SOP (450 mil)
  - 32 pin TSOP (8mm x 20mm)

PIN CONFIGURATION

32 PDIP / 32 SOP



32 PLCC



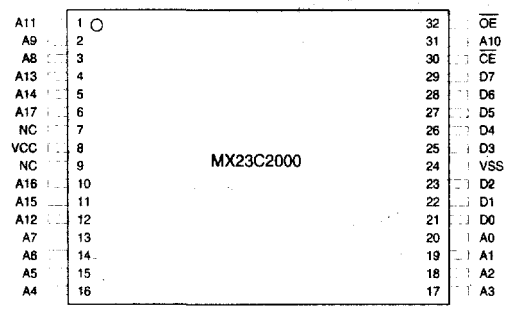
ORDER INFORMATION

Part No.	Access Time	Package
MX23C2000PC-70	70ns	32 pin PDIP
MX23C2000PC-90	90ns	32 pin PDIP
MX23C2000PC-10	100ns	32 pin PDIP
MX23C2000PC-12	120ns	32 pin PDIP
MX23C2000PC-15	150ns	32 pin PDIP
MX23C2000QC-70	70ns	32 pin PLCC
MX23C2000QC-90	90ns	32 pin PLCC
MX23C2000QC-10	100ns	32 pin PLCC
MX23C2000QC-12	120ns	32 pin PLCC
MX23C2000QC-15	150ns	32 pin PLCC
MX23C2000MC-70	70ns	32 pin SOP
MX23C2000MC-90	90ns	32 pin SOP
MX23C2000MC-10	100ns	32 pin SOP
MX23C2000MC-12	120ns	32 pin SOP
MX23C2000MC-15	150ns	32 pin SOP
MX23C2000TC-70	70ns	32 pin TSOP
MX23C2000TC-90	90ns	32 pin TSOP
MX23C2000TC-10	100ns	32 pin TSOP
MX23C2000TC-12	120ns	32 pin TSOP
MX23C2000TC-15	150ns	32 pin TSOP

PIN DESCRIPTION

Symbol	Pin Function
A0~A17	Address Inputs
D0~D7	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

32 TSOP



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Power Supply Voltage	VCC	-0.5V to 7.0V
Input Voltage	VI	-0.5V to VCC + 0.5V
Output Voltage	VO	-0.5V to VCC + 0.5V
Ambient Operating Temperature	Topr	-10°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5.0V ± 10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	0.8VCC	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.5V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5μA	0V, VCC
Output Leakage Current	ILO	-	5μA	0V, VCC
Operating Current	ICC1	-	40mA	tRC = 100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	100μA*	$\overline{CE}$ > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHz
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHz

Note : ISTB2 spec is 50μA(max.) for the PLCC package type

AC CHARACTERISTICS (Ta = 0°C ~ 70°C , VCC = 5.0V ± 10%)

Item	Symbol	23C2000-70*		23C2000-90		23C2000-10		23C2000-12		23C2000-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	70ns	-	90ns	-	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	30ns	-	45ns	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns	-	20ns	-	20ns

Note : Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.
* 70ns speed grade is under development.

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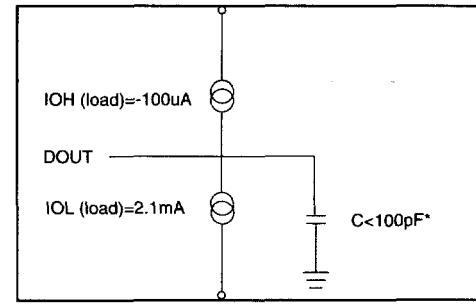
AC Test Conditions

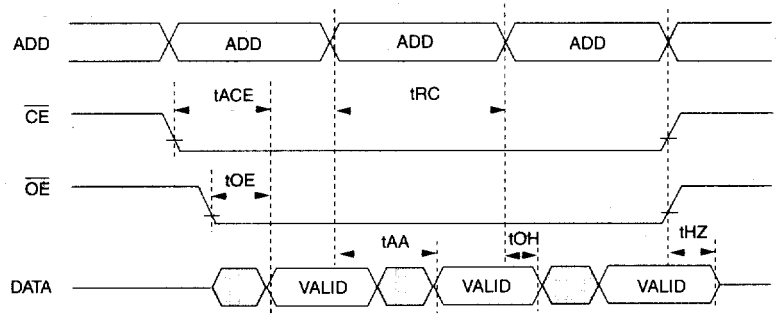
- Input Pulse Levels : 0.4V~2.4V
  0V~3V (for 70ns)
- Input Rise and Fall Times : 10ns
- Input Timing Level : 1.5V
- Output Timing Level : 0.8V and 2.0V
  1.5V (for 70ns)
- Output Load : See Figure



Note: No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.
*CL=30pF for 70ns

TIMING DIAGRAM

RANDOM READ



Note: CE,OE are enable

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
3.7	To add 70ns speed grade.	P3	NOV/16/1998
3.8	Loading=30pF for 70ns.	P3	NOV/23/1998
3.9	AC Characteristics: tOH 10ns --> 0ns	P3	JAN/29/1999