LH5821/LH5822/LH5823

LCD Dot Matrix Driver LSI

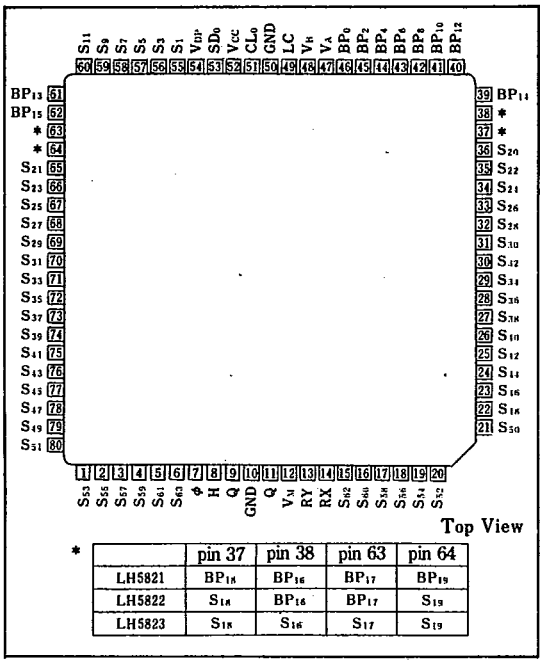
■ Description

The LH5821/LH5822/LH5823 are CMOS driver LSIs for LCD dot matrix display.
Any one of display duty ratio, 1/7 ~ 1/20 can be selected by programming.
Write and read to/from the built-in RAM of display data can be made only by 3 signals, serial data, synchronous signal, and transfer clock.
The LH5826 is available for segment output expansion.

■ Features

1. Display data RAM : 1280bits
2. 10-bit serial data transfer
3. Built-in oscillator for display
4. Duty (Selectable by programming)
   LH5821 : 1/7-1/20
   LH5822 : 1/7-1/18
   LH5823 : 1/7-1/16
5. Segment output
   LH5821 : 44bits
   LH5822 : 46 bits
   LH5823 : 48 bits
6. Common output
   LH5821 : 20 bits
   LH5822 : 18 bits
   LH5823 : 16 bits
7. Clock output for double voltage
8. Power supply voltage : 5V (TYP.)
9. Display voltage
   LH5821, LH5822 : 12V (MAX.)
   LH5823 : 10V (MAX.)
10. 80-pin quad-flat package

■ Pin Connections



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	pin 37	pin 38	pin 63	pin 64
LH5821	BP_{18}	BP_{16}	BP_{17}	BP_{19}
LH5822	S_{18}	BP_{16}	BP_{17}	S_{19}
LH5823	S_{18}	S_{16}	S_{17}	S_{19}

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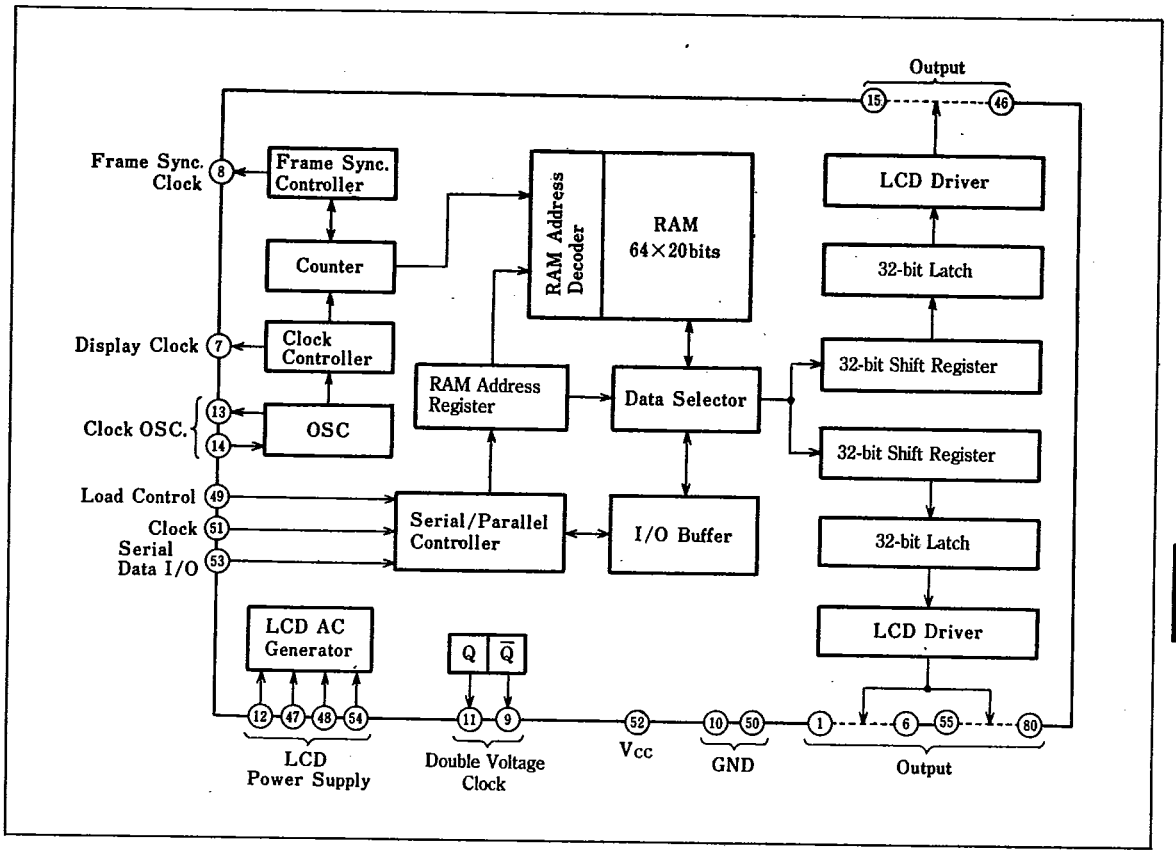
Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage*	V_{CC}	−0.3 to +7	V	1
	V_{DP}	−0.3 to +13(+11)	V	1
Operating temperature	T_{opr}	−5 to +55	℃	
Storage temperature	T_{stg}	−55 to +155	℃	

Note 1: Referenced to GND. Value in parentheses ( ) applies to LH5823.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Display voltage	V_{DP}	6		12(10)	V	2

Note 2: Value in parentheses ( ) applies to LH5823.

■ DC Characteristics

(V_{CC}=4.5 to 5.5V, Ta=−5 to 55℃)

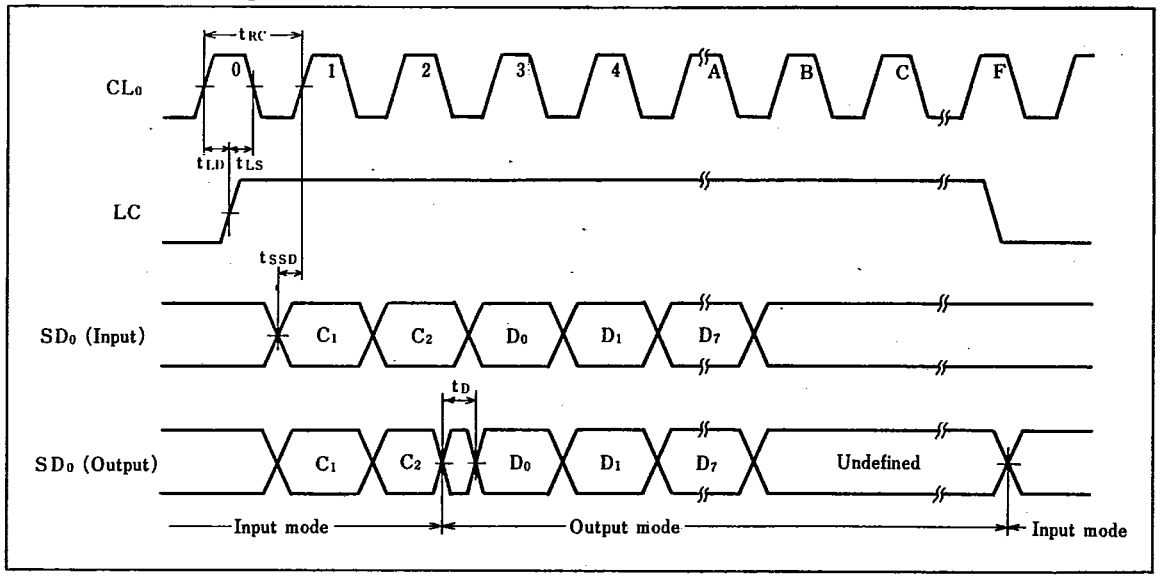
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH}		V_{CC}−0.8		V_{CC}	V	3
	V_{IL}		0		0.8		
Input current	I_{IH}	$V_{IH}=V_{CC}$		25	50	μA	4
	I_{IL}	V_{IL}=0V			1		
Output voltage	V_{OH}	I_{OH}=400μA	2.4			V	5
	V_{OL}	I_{OL}=1.6mA			0.8		
Output resistance	R_Q	V_{CC}=5V, V_{DS}=1.0V		80		Ω	6,7
	R_{SEG}	V_{DP}=6V, Ta=25℃, V_{DS}=1V		1.0	30	kΩ	7,8
	R_{COM}			1.5	4.5	kΩ	9
	R_V			40	1	Ω	10
Input leakage current	$\lvert I_L \rvert$				1.0	μA	6
Current consumption	I_{CC1}	Durling no-load blank display f_ϕ=100kHz, f_{CLO}=0Hz, Ta=25℃		200	500	μA	
	I_{CC2}	Durling data write (write cycle 1/45 MHz) f_ϕ=100kHz, f_{CLO}=1MHz, Ta=25℃			2	mA	
	I_{DP}	Durling no-load blank display V_{DP}=12V, f_ϕ=100kHz, 1/16 duty		5	10	μA	

Note 3: Applied to pins CL_0, LC and SD_0
Note 4: Applied to p LC
Note 5: Applied to pins SD_0, H and ϕ
Note 6: Applied to all pins except LC
Note 7: Applied to pins Q and $\overline{Q}$
Note 8: Applied to segment output pin.
Note 9: Applied to common output pin.
Note10: Applied to pins V_A and V_B

■ AC Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CL_0 cycle time	t_{RC}		1			μs
LC hold time	t_{LD}		0			ns
LC setup time	t_{LS}		100			ns
SD_0 setup time	t_{SSD}		100			ns
SD_0 input/output switching time	t_D	C_L=50pF		80	450	ns

■ AC Timing Diagram



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■ Functions

(1) Pin description

Pin name	No. of pins	I/O	Functions
V_{CC}, GND	3	I	Power supply for logic circuit
V_{DP}, V_A, V_M, V_B	4		Power supply for liquid crystal drive
LC	1		Serial data transfer sync. signal
CL_0	1		Serial data transfer clock input
RX	1		Input clock oscillation pin
RY	1	O	Input clock oscillation pin
ϕ	1		Clock output for display
H	1		Liquid crystal frame sync. signal
Q, $\overline{Q}$	2		Clock output for double voltage generation
S_{20}~S_{63} (LH5821)	44		Liquid crystal segment drive signal
S_{18}~S_{63} (LH5822)	46		
S_{16}~S_{63} (LH5823)	48		
BP_0~BP_{19} (LH5821)	20		Liquid crystal common drive signal
BP_0~BP_{17} (LH5822)	18		
BP_0~BP_{15} (LH5823)	16		
SD_0	1	I/O	Serial data input/output

(2) Relationship between 10-bit serial data and modes

10-bit data/mode	C_1	C_2	D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
Chip select/duty setup mode	0	0	Chip select data | Duty data
RAM address setup mode	0	1	A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
8-bit data write mode	1	0	Data
8-bit data read mode	1	1	Data

(C_1, C_2 : Control data, D_0~D_7 : Data)

• LC single

The LC signal is a sync. signal for serial transfer, and when LC is low, LSI remains in the standby condition regardless of the condition of SD_0 and CL_0, When LC becomes high and clock CL_0 is supplied, the LSI is enabled.

• CL_0 signal

The CL_0 signal is the clock signal for serial transfer and is used to write and read serial tranpfer data SD_0.

• SD_0 signal

The SD_0 signal is 10-bit serial transfer data of which the first 2 bits are control data and the remaining 8 bits are data. In the read mode the SD_0 pin becomes an output pin and outputs the 8-bit RAM data in serial. After the write or read mode has been executed, the lower 6 bits, A_0-A_5, of the RAM address are automatically incremented, but A_6 and A_7 do not change.

• Chip select

In the LSI, the chip select code is set at "0000", this chip is selected by the chip select code "0000" input from the SD_0 pin.

The RAM address setting and writing and reading of the 8-bit data is executed only for the chip selected, and once a chip is selected, it remains in the selected condition until a select code for the next chip is input.

• ϕ signal

The ϕ signal is the clock output for display and is supplied to LH5826.

• H signal

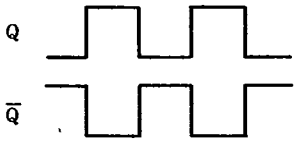
The H signal is the frame period signal for the liquid crystal and is supplied to LH5826. When the power is turned on, the timing signal in each device is in an asynchronous condition, and after the H signal is generated, they are synchronized.

• Auto clear

When the power is turned on, the display signal generates an OFF pattern. Auto clear is canceled when all of the duty data of the chip select duty data are made "1" and input, and then the contents of the RAM are displayed. The chip select duty does not change at this time.

• Double voltage clock

A double voltage clock is output from pins Q and $\overline{Q}$. The Q and $\overline{Q}$ signals are clock signals made by dividing the display clock ϕ by 2, and their respective polarities are opposite.



■ System Configuration Example