8 MHz VIDEO OUTPUT AMPLIFIER

GENERAL DESCRIPTION

The TDA6100Q is a video amplifier in a SIL 9 MP (Single In Line 9 pins Medium Power) package, using high-voltage DMOS technology and is intended to directly drive the cathode of a cathode ray tube (CRT).

Features

- High bandwidth and slew rate
- No external heatsink required
- Black-current measurement output for automatic black-current stabilization (ABS)
- A cathode output separated from the feedback output
- Internal protection against CRT flashover discharges
- Protection against electrostatic discharge (ESD)
- Simple application with a variety of colour decoders
- Differential input with designed-in maximum values of the following:
  - common mode input capacitance of 3 pF
  - differential mode input capacitance of 2 pF
  - differential input voltage temperature drift of 0.4 mV/K

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
High supply voltage	V_{P1}	180	–	210	V
Low supply voltage	V_{P2}	10.8	–	13.2	V
Total power dissipation	P_{tot}	0	–	1.9	W
Operating ambient temperature range	T_{amb}	0	–	+ 65	°C

PACKAGING OUTLINE

9-lead SIL; plastic (SOT111B).

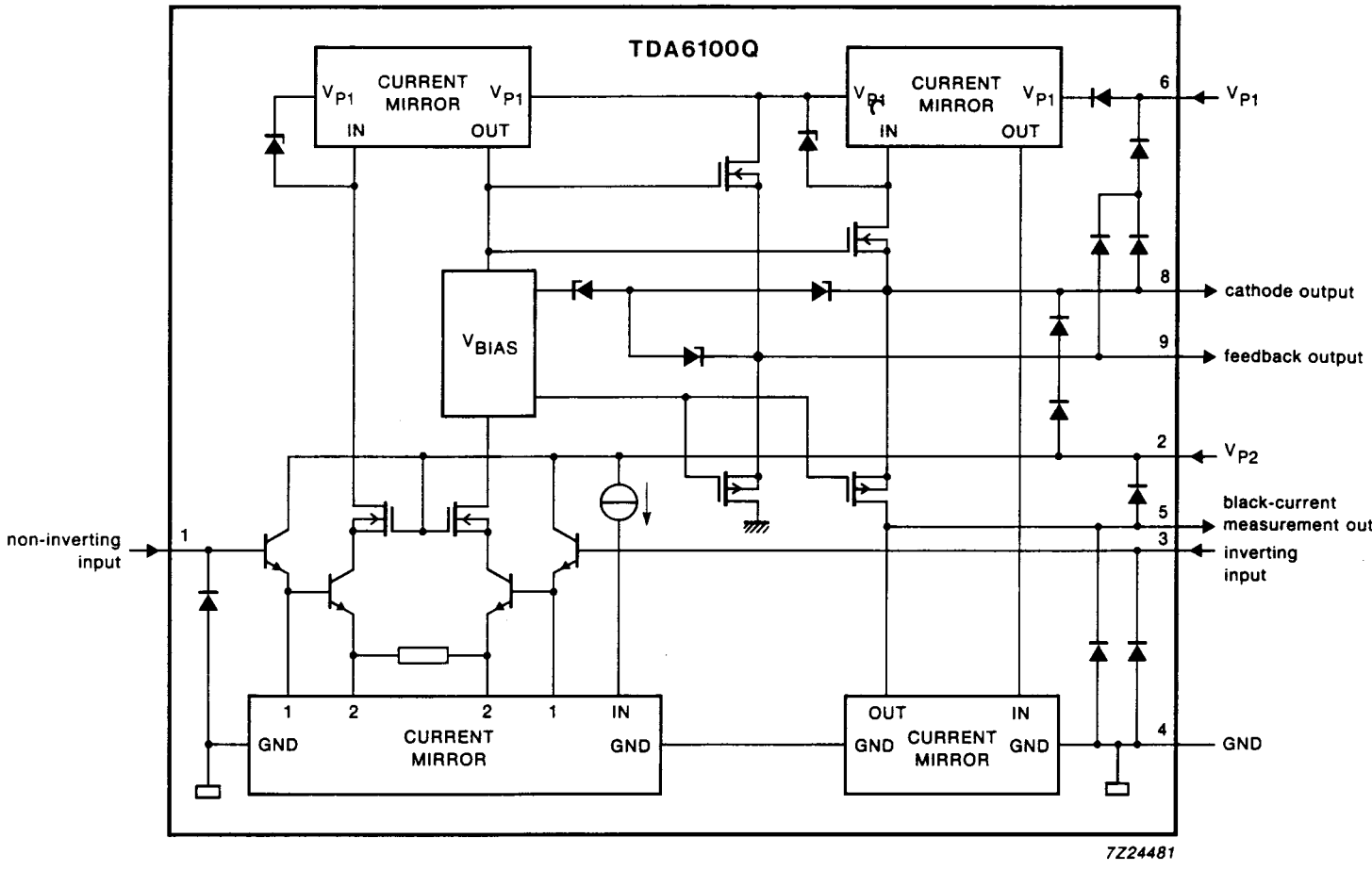


Fig.1 Block diagram.

PINNING

1 Non-inverting input
2 Low supply voltage
3 Inverting input
4 Ground, substrate, heat tab
5 Black-current measurement output
6 High supply voltage
7 Not connected
8 Cathode output
9 Feedback output

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	typ.	max.	unit
High supply voltage		V_{P1}	0	–	250	V
Low supply voltage		V_{P2}	0	–	14	V
Input voltage (pins 1 and 3)		V_1, V_3	0	–	V_{P2}	V
Differential mode input voltage (pin 1 to 3)		V_{1-3}	−6	–	6	V
Black-current measurement output voltage (pin 5)		V_5	0	–	V_{P2}	V
Cathode and feedback output voltage (pins 8 and 9)		V_8, V_9	V_{P2}	–	V_{P1}	V
Non-inverting and inverting input current (pins 1 and 3)		I_1, I_2	0	–	1	mA
Cathode and feedback repetitive peak output current (pins 8 and 9)		I_8, I_9	−25	–	+ 25	mA
Cathode non-repetitive peak output current						
LOW	Q = 50 μC	I_8	−2.5	–	+ 2.5	A
HIGH	Q = 100 nC	I_8	−10	–	+ 10	A
Total power dissipation		P_{tot}	0	–	1.9	W
Storage temperature range		T_{stg}	−65	–	+ 150	°C
Junction temperature range		T_j	0	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 45 K/W

From junction to case $R_{th\ j\text{-}c}$ = 10 K/W

CHARACTERISTICS

Operating range

V_{P1} = 180 to 210 V; V_{P2} = 10.8 to 13.2 V; V_1 = 2.6 to 5 V; V_5 = 1.4 V to the smallest of (V_8 – 8 V) or V_{P2}; T_{amb} = 0 to 65 °C.

Test conditions (unless otherwise specified)

V_{P1} = 200 V; V_{P2} = 12 V; V_5 = 6 V; T_{amb} = 25 °C; C_L = 10 pF; V_1 = 5 V (C_L consists of parasitic and cathode capacitance). For test circuit see Fig.2.

parameter	conditions	symbol	min.	typ.	max.	unit
Quiescent current						
high voltage supply	$V_8 = V_{P1}/2$	I_{P1}	4	4.9	6	mA
low voltage supply	$V_8 = V_{P1}/2$	I_{P2}	2.5	3.1	3.8	mA
Input bias current	$V_8 = V_{P1}/2$		0	–	20	μA
Input offset current	$V_8 = V_{P1}/2$		–3	–	+3	μA
Offset current of black-current measurement output	I_8 = 0 A; 50 V < V_8 < V_{P1} – 20 V; 1.4 V < V_5 < V_{P2}	$I_{5(off)}$	–10	0	+10	μA
Linearity of current transfer						
LOW I_8	I_8 = 0 to 10 μA; 50 V < V_8 < V_{P1} – 20 V; 1.4 V < V_5 < V_{P2}	$\Delta I_5/\Delta I_8$	0.9	1	1.1	
HIGH I_8	I_8 = 0 to 3 mA; 50 V < V_8 < V_{P1} – 20 V; 1.4 V < V_5 < V_{P2}	$\Delta I_5/\Delta I_8$	0.9	1	1.1	
Maximum peak output current (pins 8 and 9)	20 V < V_8 < V_{P1} – 20 V	$\lvert I_{O\,max}\rvert$	–	20	–	mA
Input offset voltage	$V_8 = V_{P1}/2$	$V_{I(off)}$	–50	–	+50	mV
Output voltage (pins 8 and 9)						
minimum	V_{1-3} = –1 V	$V_{O\,min}$	–	–	20	V
maximum	V_{1-3} = 1 V	$V_{O\,max}$	V_{P1} –20	–	–	V
Gain-bandwidth product of open loop gain V_9/V_{1-3}	f = 500 kHz; $V_{8(p-p)}$ = 60 V	BW_g	–	0.7	–	GHz
Small signal bandwidth	$V_{8(p-p)}$ = 60 V sine	BW_s	6.5	8	–	MHz
Large signal bandwidth	$V_{8(p-p)}$ = 100 V sine	BW_l	5	6.5	–	MHz
Cathode output propagation time 50% input – 50% output	V_8 = 50 to 150 V square wave; f < 1 MHz; t_f input < 20 ns	t_p	40	51	62	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Cathode output rise time 10% output – 90% output	V_8 = 50 to 150 V square wave; f < 1 MHz; t_f input < 20 ns	t_r	40	53	65	ns
Cathode output fall time 90% output – 10% output	V_8 = 150 to 50 V square wave; f < 1 MHz; t_r input < 20 ns	t_f	40	53	65	ns
Settling time; 50% input – 99% < output < 101%	$V_{8(p-p)}$ = 100 V square wave; f < 1 MHz; t_r, t_f input < 20 ns	t_s	–	–	220	ns
Slew rate between 50 and 150 V	$V_{1-3(p-p)}$ = 2 V square wave; f < 1 MHz; t_r, t_f input < 20 ns	SR	–	1700	–	V/μs
Cathode output voltage overshoot	$V_{8(p-p)}$ = 100 V square wave; f < 1 MHz; t_r, t_f input < 20 ns; note 1	OV	–	–	5	%
Differential input resistance		R_I	–	100	–	kΩ
High voltage power supply rejection ratio	f < 50 kHz; note 2	HVPSRR	–	80	–	dB
Low voltage power supply rejection ratio	f < 50 kHz; note 2	LVPSRR	–	80	–	dB

DEVELOPMENT DATA

Notes to the characteristics

1. If $V_{P2} - V_1 < 7$ V, there can be more overshoot than specified.
2. PSRR: the ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.
3. The above electrical characteristics and stable operation are specified for a feedback range of 1/75 to 1/90.
4. The cathode output is protected against peak currents (caused by high-resistance flash) of 2.5 A maximum with a charge content of 50 μC.
5. The cathode output is also protected against peak currents (caused by low-resistance flash) of 10 A maximum with a charge content of 100 nC.

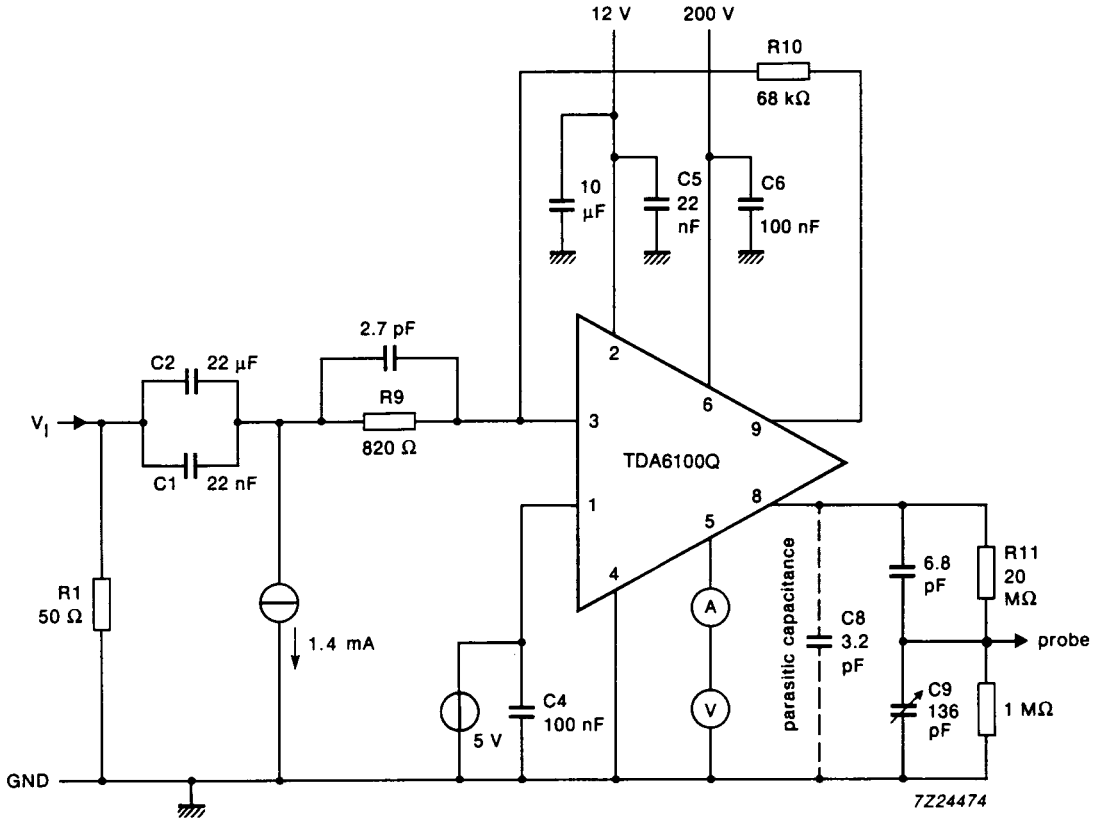


Fig.2 Test circuit with feedback factor of 1/83.

FLASHOVER PROTECTION

The device incorporates protection diodes to prevent CRT flashover discharges; these diodes clamp the cathode output voltage between $V_{P1} + V_{diode}$ and $V_{P2} - V_{diode}$. To limit the diode current the following is needed: an external 1.5 kΩ high-voltage carbon resistor in series with the cathode output and a 1 kV spark-gap (see Fig.9).

V_{P1} – GND has to be decoupled:

- With a capacitor > 20 nF with good HF characteristics (e.g. ceramic). This capacitor (between pins 6 and 4) must be placed as near as possible to the device and no more than 10 mm away from it.
- With a capacitor > 10 µF on the CRT's printed-circuit board (common for the three output stages).

V_{P2} – GND has to be decoupled with a capacitor > 20 nF on the CRT's printed-circuit board.

APPLICATION INFORMATION

Dissipation

There are two components of the dissipation — static dissipation (independent of the frequency) and dynamic dissipation (proportional to the frequency).

The static dissipation is due to both high- and low-voltage supply currents and load currents in the feedback network and CRT and is given by:

$P_{stat} = (V_{P1} \times I_{P1}) + (V_{P2} \times I_{P2}) + (V_8 \times I_8) - (V_9 \times V_9/R_{fb})$.

Where $V_9 = V_8 = 100$ V; feedback resistor $R_{fb} = 68$ kΩ; $I_8 = 0.3$ mA and other typical conditions as provided in the **CHARACTERISTICS.** The static dissipation, $P_{stat} = 0.9$ W.

The dynamic dissipation is given by:

$P_{dyn} = V_{P1} \times (C_L + C_{fb} + C_{int}) \times f \times V_{o(p-p)} \times b$.

Where load capacitance $C_L = 10$ pF; feedback capacitance $C_{fb} = 0$; internal load capacitance $C_{int} = 4$ pF; sine wave frequency $f = 4$ MHz; peak-to-peak output voltage $V_{o(p-p)} = 100$ V and the non-blanking duty factor $b = 80\%$. The dynamic dissipation, $P_{dyn} = 0.9$ W.

To minimize the load capacitance, C_L, TDA6100 must be mounted on the printed-circuit board at the base of the CRT.

The total dissipation, $P_{tot} = P_{stat} + P_{dyn} = 1.8$ W under the conditions given.
From $T_j = T_{amb} + (P_{tot} \times R_{th\ j\text{-}a}) < T_{j,\ max} = 150\ ^oC$, it follows that no additional heatsink is required for $T_{amb} < T_{amb\ max} = 65\ ^oC$.

Black-current stabilization

To use the black-current stabilization feature, a signal source including a black-current stabilization loop is needed (TDA3562A or TDA4580). The black-current needs to be converted to a voltage by, for example, an 82 kΩ resistor connected to ground and a 150 kΩ resistor connected to V_{P2}. A clamping diode connected to V_{P2} prevents capacitive load currents from causing the voltage to exceed $V_{P2} + V_{diode}$. Care must be taken to minimize the parasitic capacitance at the current-to-voltage conversion node. Both TDA4580 and TDA3562A feature sequential black-current stabilization, therefore the black-current measurement outputs of all three video output stages can be added. To obtain the correct ratio of cathode currents for colour balance at the stabilized black-level, the circuit illustrated by Fig.3 may be used.

The output voltage depends on the currents $I_{5,R}$, $I_{5,G}$ and $I_{5,B}$ as expressed in the following formula:

$$V_O = R4 \times \frac{[(R1 + R2 + R3)I_{5,B} + (R1 + R2)I_{5,G} + (R1)I_{5,R}]}{(R1 + R2 + R3 + R4)}.$$

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

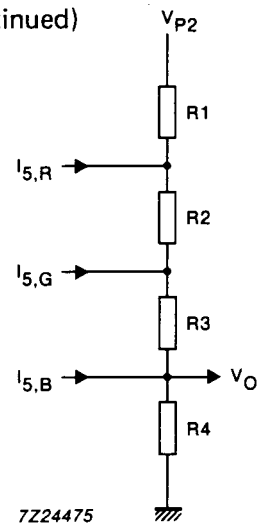


Fig.3 Colour balance diagram.

Figure 4 below illustrates a method for adjusting the ratios of the stabilized black-currents.

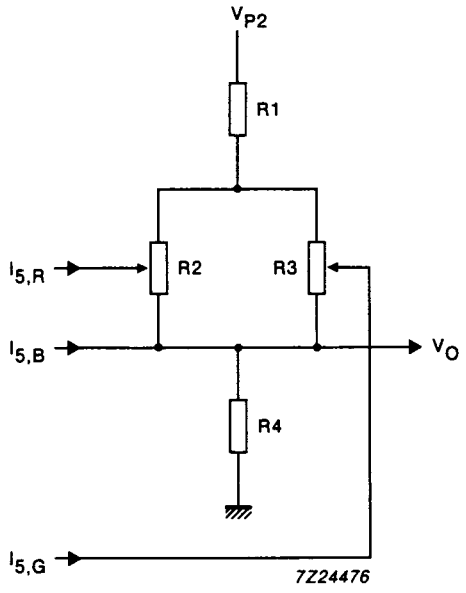


Fig.4 Stabilized black-current adjustment.

The black-current measurement output of the TDA6100Q deals with both positive and negative leakage currents at the cathode output.

Gain and DC biasing

Figure 5 illustrates a circuit in which the gain and the black-level output can be adjusted independently. If the potentiometers have a relatively low value of resistance, the feedback factor remains approximately constant. The input black-level is given by $V_{I,BL}$. Figure 6 illustrates a circuit for this adjustment when ABS is used.

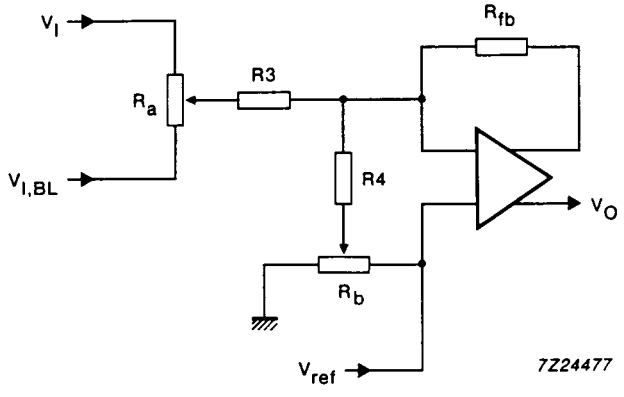


Fig.5 Gain and black-level adjustment.

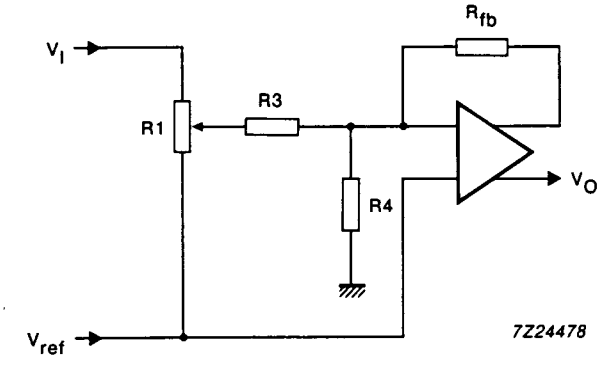


Fig.6 Gain and black-level adjustment with ABS.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Referring to the circuit illustrated by Fig.6 the total gain is given by:

$$A = \frac{a \times R_{fb}}{R_a(a\text{-}a^2) + R3} \text{ with } 0 \leqslant R_a(a\text{-}a^2) \leqslant R_a/4$$

If the value of the gain is known, then the adjustment of the potentiometer can be found from:

$$a = 0.5 \left\{ \left[\left(\frac{R_{fb}}{A \times R_a} - 1 \right)^2 + \left(4 \times \frac{R3}{R_a} \right) \right]^{1/2} - \left(\frac{R_{fb}}{A \times R_a} - 1 \right) \right\}$$

The feedback factor (stipulating the bandwidth) of the circuit follows from:

$$1/k = 1 + \frac{R_{fb}}{R4//[R3 + R_a(a\text{-}a^2)]}$$

The output black-level is given by:

$$V_{O,BL} = V_{ref} \frac{R_{fb} + R4}{R4} - A(V_{I,BL} - V_{ref})$$

If the value of the black-level is known, then R4 can be calculated as a function of V_{ref} or, V_{ref} as a function of R4, as shown below:

$$R4 = R_{fb} \times \frac{V_{ref}}{V_{O,BL} + A(V_{I,BL} - V_{ref}) - V_{ref}}$$

$$V_{ref} = \frac{V_{O,BL} + A \times V_{I,BL}}{(A + 1 + R_{fb}/R4)}$$

To obtain the required feedback, R3 and R4 or V_{ref} must be chosen. The results can be read from the above formulae.

DC biasing at high gain

When the device is used as an 8 MHz and x 90 gain amplifier with AC coupling of the signal source, DC biasing can be accomplished by using the circuits illustrated by Figs 7 and 8.

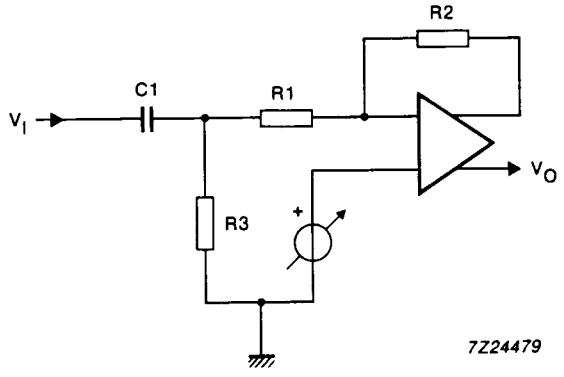


Fig.7 DC biasing using an adjustable voltage source.

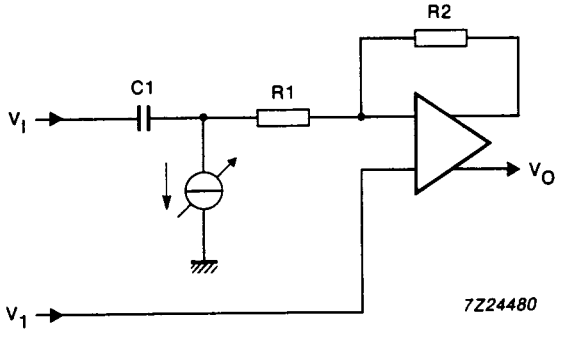
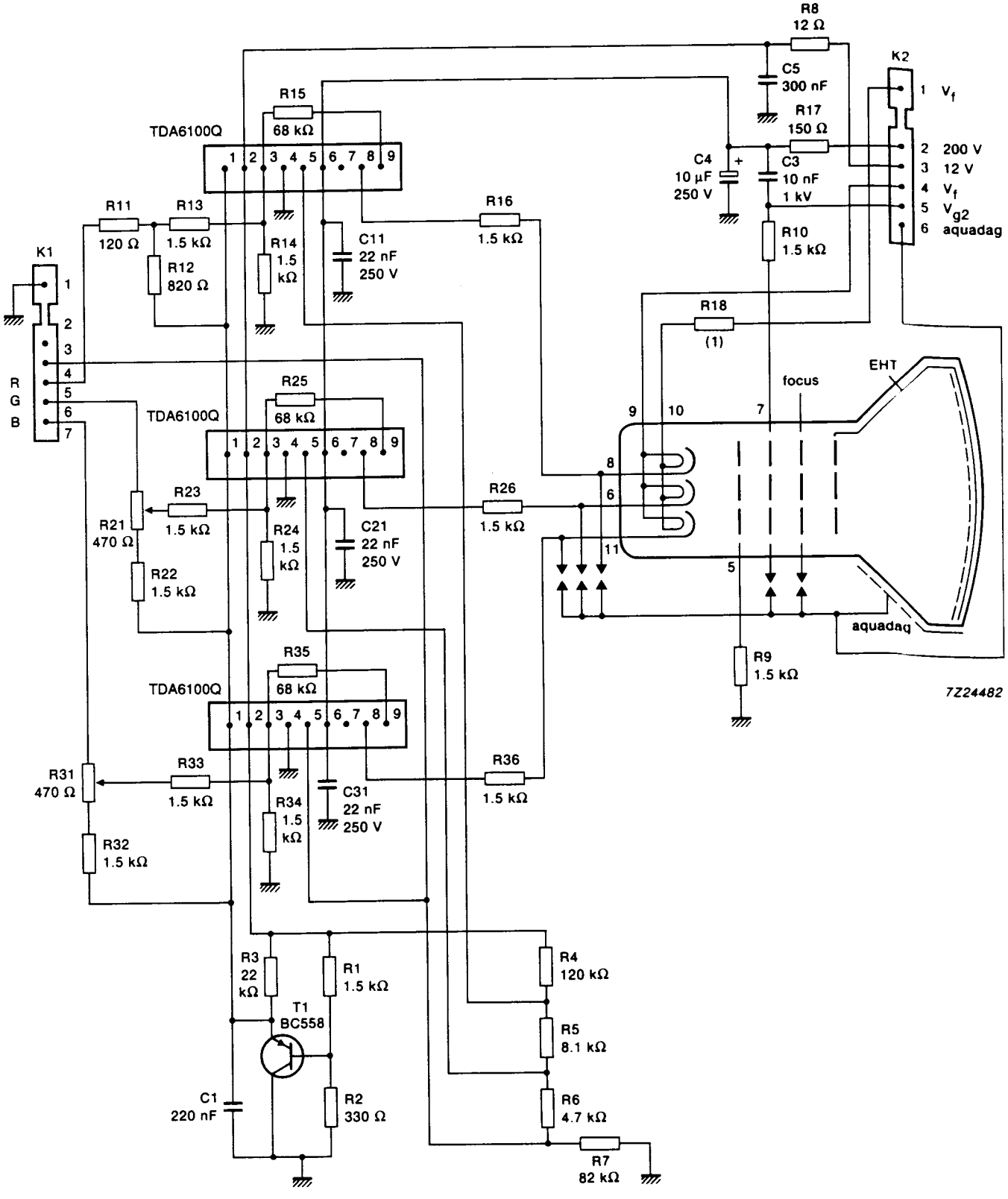


Fig.8 DC biasing using an adjustable current source.

Application circuit

Figure 9 illustrates an application circuit for use with ABS (eg TDA4580), in which a number of components are common for the three output stages.

APPLICATION INFORMATION (continued)



(1) Value to be fixed.

Fig.9 Application circuit for use with ABS (eg TDA4580) using CRT A66EAK00X (30AX).