# Dual 9-Bit Parity Generator & Checker 8-Bit Word Comparator • 850 ps Delay 10G PicoLogic™ Family



## FEATURES

- Generate or check even or odd parity for two sets of 8 data lines (1300 ps)
- Generates equivalence of two 8 bit words (850 ps)
- Check equivalence and parity of two 8 bit words simultaneously (1300 ps)
- Cascadable for N-bits parity
- Up to1.5 GHz input frequency
- ECL and Picologic family compatible I/O
- Wired-OR output capability
- On-chip threshold compensation circuit (VBB input) and reference voltage generator (VBBS)
- Available in leadless or C-leaded chip carriers or in unpackaged die form
- Packages contain internal decoupling capacitors for optimum high frequency performance
- 0° to 85° operating temperature range

## APPLICATIONS

- Cache tag comparison
- Frame synchronization & code identification
- Correlation
- Parity generation and checking

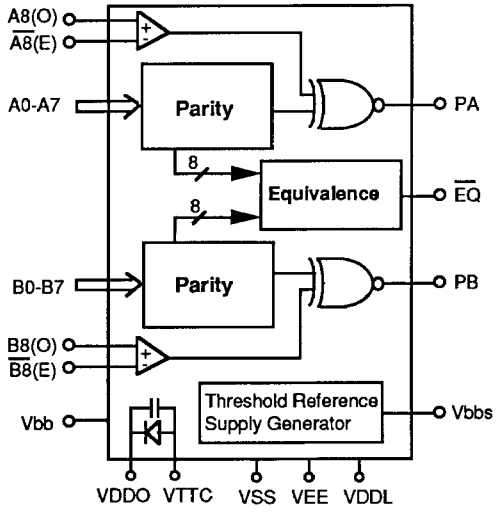
## FUNCTIONAL DESCRIPTION

The 10G045 is an ECL and PicoLogic family compatible ultra-fast dual 9-bit parity checker, 8-bit parity generator and 8 bit word comparator. The device can be configured to generate even or odd parity and can be cascaded to provide N-bit parity. The equivalence and parity of two 8-bit words can be checked simultaneously. For compatibility with any ECL or GaAs logic family, the 10G045 incorporates the PicoLogic standard input threshold compensation circuit driven by the VBB input as well as an on-chip threshold reference generator which provides a nominal -1.3V reference voltage on the VBBS output pin.

Typical data to parity output propagation delay is 1000 ps; typical data input to equivalence output delay is 700 ps; typical parity input to parity output delay is 700 ps. Operation at 1.5 GHz can be sustained while dissipating less than 1.2 W at room temperature. Output rise and fall times are typically 150 ps.

The 10G045 is a member of GigaBit Logic's 10G PicoLogic family of gallium arsenide integrated circuits and is fabricated using Gigabit's high volume, GaAs MESFET process technology.

## BLOCK DIAGRAM



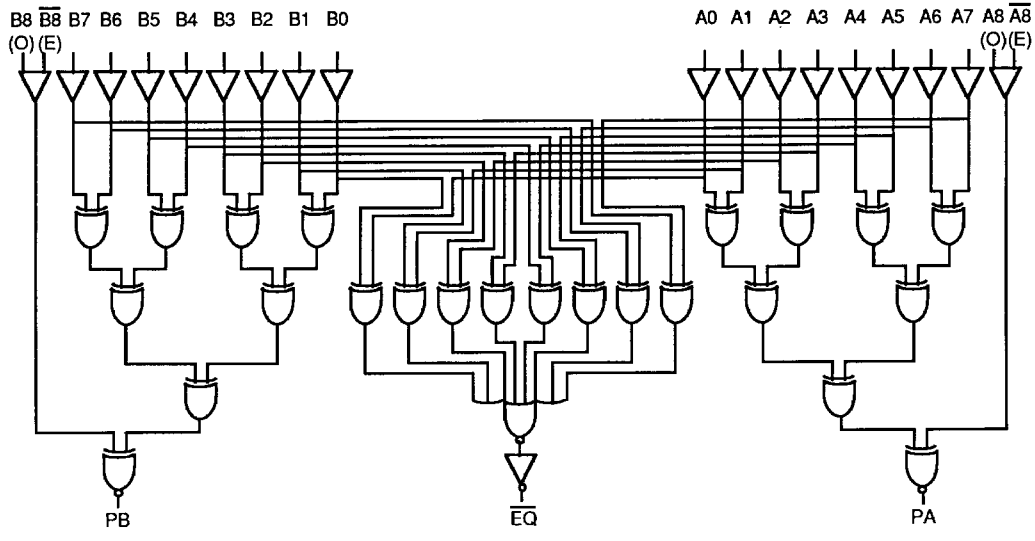

## 10G045 ORDERING INFORMATION

| PACKAGE TYPE | DELAY (Max. @ 25°C) |
|---|---|
| | 850 ps ($\overline{EQ}$ Output) |
| 40 pin Leadless CC | 10G045-2L |
| 40 pin C-leaded CC | 10G045-2C |
| Dice | 10G045-2X |

## PIN DESCRIPTIONS

| | |
|---|---|
| A0 - A7 | Data inputs, A word. |
| B0 - B7 | Data inputs, B word. |
| A8(O), B8(O) | Odd parity inputs. |
| $\overline{A8}$(E), $\overline{B8}$(E) | Even parity inputs. |
| $\overline{EQ}$ | Equivalence output of words A and B. |
| PA, PB | Parity outputs of words A and B. Programmable for even or odd parity. |
| VDDO | Output driver ground (0V). |
| VDDL | Internal logic ground (0V). |
| VSS | - 3.4V power supply. |
| VEE | - 5.2V power supply. |
| VDCH | Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. Consult App. Note 4 for details. |
| VTTC | Internal VDDO decoupling capacitor return pin. VTTC is brought into the 10G045 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G045 die. VTTC is typically tied to VTT (nom. -2.0V). |
| VBB | Reference input to the 10G045's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G045 from ECL. Connect to the VBBS pin when the 10G045 is driven from PicoLogic. This pin may not be left unconnected. |
| VBBS | PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic. |

## 10G045 LOGIC DIAGRAM



## TRUTH TABLES

The 10G045 can be programmed for even or odd parity by appropriate connection of the even and odd parity inputs as shown below.

Generate EVEN parity of 8-bit word (A side shown)

| Input A8(O) | Input $\overline{A8(E)}$ | Sum of HIGH Inputs A0 - A7 | Output PA |
|---|---|---|---|
| H | L or VBB(S) | EVEN | L |
| H | L or VBB(S) | ODD | H |

Generate ODD parity of 8-bit word (A side shown)

| Input A8(O) | Input $\overline{A8(E)}$ | Sum of HIGH Inputs A0 - A7 | Output PA |
|---|---|---|---|
| L | H or VBB(S) | EVEN | H |
| L | H or VBB(S) | ODD | L |

Check EVEN parity of 9-bit word (A side shown)

| Input A8(O) | Sum of HIGH Inputs A0 - A7, $\overline{A8(E)}$ | Output PA |
|---|---|---|
| VBB(S) | EVEN | L |
| VBB(S) | ODD (Parity Error) | H |

Check ODD parity of 9-bit word (A side shown)

| Input $\overline{A8(E)}$ | Sum of HIGH Inputs A0 - A7, A8(O) | Output PA |
|---|---|---|
| VBB(S) | ODD | L |
| VBB(S) | EVEN (Parity Error) | H |

Equivalence of two 8-bit words:

$$\overline{EQ} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \approx B3) + (A4 \oplus B4) + (A5 \oplus B5) + (A6 \oplus B6) + (A7 \oplus B7)$$

## DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| ISS | Power Supply Current | | 175 | 240 | mA |
| IEE | Power Supply Current | | 115 | 150 | mA |
| PD | Power Dissipation | | 1.2 | 1.6 | W |

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

## AC CHARACTERISTICS (Note 1)

**10G045-2**

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = Gnd, unless otherwise indicated.

| SYMBOL | PARAMETER | Tc = 0°C | | Tc = +25°C | | | Tc=+85°C | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | TYP | MAX | MIN | MAX | | |
| 1/(2T1) | Operating frequency | 1.0 | | 1.1 | 1.5 | | 1.0 | | GHz | |
| T2 | Data to parity output high delay | 800 | 1300 | 800 | 1000 | 1300 | 800 | 1300 | ps | |
| T3 | Data to parity output low delay | 800 | 1300 | 800 | 1000 | 1300 | 800 | 1300 | ps | |
| T4 | Parity input to parity output high delay | 550 | 900 | 550 | 700 | 900 | 550 | 900 | ps | |
| T5 | Parity input to parity output low delay | 550 | 900 | 550 | 700 | 900 | 550 | 900 | ps | |
| T6 | Data input to $\overline{EQ}$ output high delay | 550 | 950 | 550 | 700 | 850 | 550 | 900 | ps | |
| T7 | Data input to $\overline{EQ}$ output low delay | 550 | 950 | 550 | 700 | 850 | 550 | 900 | ps | |
| T8 | Output rise time | | 200 | | 150 | 200 | | 200 | ps | 2 |
| T9 | Output fall time | | 150 | | 150 | 200 | | 150 | ps | 2 |

Notes: 1. Test conditions ( unless otherwise indicated ) :

VBB = -1.2V — VIH = -0.7V — VDCH = VDDO

VTT = -2.0V — VIL = -1.7V

VTTC = VTT — VOH ≥ -0.7V

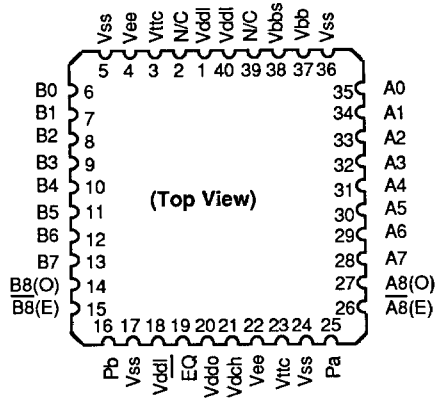
RLOAD = 50Ω to -2.0V — VOL ≤ -1.7V

Input signal rise and fall time ≤ 150 ps

2. Rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.

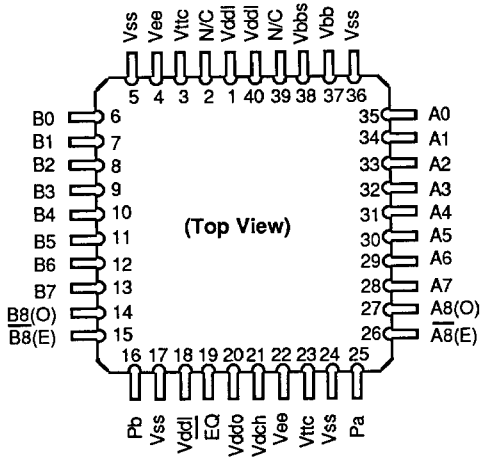
## PACKAGE PINOUT DIAGRAMS

### PACKAGE TYPE "L"




NOTES: Pin 1 is marked for orientation. N/C = No Connection.

### PACKAGE TYPE "C"




NOTES: Pin 1 is marked for orientation. N/C = No Connection.

## SWITCHING WAVEFORMS