1 MHz – 8 GHz, 60 dB Logarithmic Detector/Controller

Preliminary Technical Data **AD8318**

FEATURES

Wide Bandwidth: 1 MHz to 8 GHz

High Accuracy: ±1.0 dB over 55 dB up to 5.8 GHz

Stability Over Temperature ±0.5 dB

Low Noise Measurement/Controller Output VOUT

Pulse Response Time 8/13 nS (Fall/Rise)

Integrated Temperature Sensor

Small Footprint CSP Package

Power-Down Feature: <1.5 mW at 5V

Single Supply Operation: 5V @ 65 mA

Fabricated Using High Speed SiGe Process

FUNCTIONAL BLOCK DIAGRAM

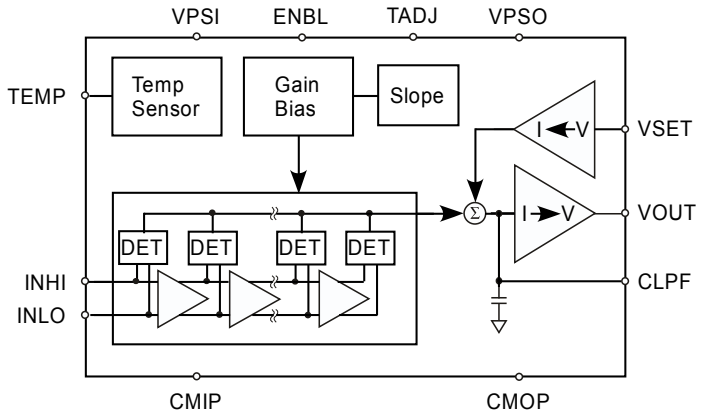

Figure 1. Functional Block Diagram

APPLICATIONS

RF Transmitter PA Setpoint Control & Level Monitoring

RSSI Measurement in Base Stations, WLAN, Radar

GENERAL DESCRIPTION

The AD8318 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device can be used in either measurement or controller modes. The AD8318 maintains accurate log conformance for signals of 1 MHz to 6 GHz and provides useful operation to 8 GHz. The input range is typically –60 dBm to 0 dBm (re 50Ω) with error less than ±1dB. The AD8318 has a 8 ns response time that enables RF burst detection to beyond 60 MHz. The device provides unprecedented logarithmic intercept stability versus ambient temperature conditions. A 2mV/K slope temperature sensor output is also provided for additional system monitoring. A single supply of +5 V is required. Current consumption is typically 65 mA. Power consumption decreases to < 1mW when the device is disabled.

The AD8318 can be configured to provide a control voltage to a power amplifier or a measurement output, from pin **VOUT**. Since the output can be used for controller applications, special attention has been paid to minimize wide-band noise. In this mode, the set-point control voltage is applied to **VSET**. The feedback loop through an RF amplifier is closed via **VOUT**; the output of which regulates the amplifier's output to a magnitude corresponding to V_{SET}. The AD8318 provides 0V to 3.9V output capability at the **VOUT** pin, suitable for controller applications. As a measurement device, **VOUT** is externally connected to **VSET** to produce an output voltage V_{OUT} that is a decreasing linear-in-dB function of the RF input signal amplitude.

The logarithmic slope is –25 mV/dB, determined by the **VSET** interface. The intercept is 20 dBm (re 50Ω, CW input) using the **INHI** input. These parameters are very stable against supply and temperature variations.

The AD8318 is fabricated on a SiGe bipolar IC process and is available in a 4x4 mm, 16-pin MLFCSP package, for the operating temperature range of –40°C to +85°C..

Rev. PrF 4/2/04

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SPECIFICATIONS

Table 1. V_P = 5 V, C_{LPF}=200pF, T_A = 25°C, 52.3 Ohm termination resistor at INHI unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	**INHI** (pin 14) and **INLO** (pin 15)				
Specified Frequency Range		0.001		8	GHz
DC Common-Mode Voltage			VPOS – 1.3	1	V
Input Impedance	f = 2.2 GHz		225Ω||0.7pF		Ω||pF
MEASUREMENT MODE	**VOUT** (pin 6) shorted to **VSET** (pin 7), Sinusoidal Input Signal				
f = 900 MHz	500 ohms at **TADJ**				
± 1 dB Dynamic Range	–40°C < T_A < +85°C		48		dB
Maximum Input Level	± 1 dB Error		-1		dBm
Minimum Input Level	± 1 dB Error		-58		dBm
Slope			-24.5		mV/dB
Intercept			22		dBm
Output Voltage - High Power In	PIN = -10dBm		0.772		V
Output Voltage- Low Power In	PIN = -50dBm		1.75		V
Temperature Sensitivity	PIN = -10dBm				
	25°C ≤ T_A ≤ +85°C		0.00270		dB/ °C
	-25°C ≤ T_A ≤ +25°C		0.00016		dB/ °C
	-40°C ≤ T_A ≤ +25°C		0.00040		dB/ °C
f = 1.900 GHz					
± 1 dB Dynamic Range	–40°C < T_A < +85°C		44		dB
Maximum Input Level	± 1 dB Error		-3		dBm
Minimum Input Level	± 1 dB Error		-58		dBm
Slope			-24.4		mV/dB
Intercept			20.5		dBm
Output Voltage - High Power In	PIN = -10dBm		0.732		V
Output Voltage- Low Power In	PIN = -50dBm		1.71		V
Temperature Sensitivity	PIN = -10dBm				
	25°C ≤ T_A ≤ +85°C		0.00068		dB/ °C
	-25°C ≤ T_A ≤ +25°C		0.00440		dB/ °C
	-40°C ≤ T_A ≤ +25°C		0.00520		dB/ °C
f = 2.200 GHz					
± 1 dB Dynamic Range	–40°C < T_A < +85°C		49		dB
Maximum Input Level	± 1 dB Error		-3		dBm
Minimum Input Level	± 1 dB Error		-60		dBm
Slope			-24.3		mV/dB
Intercept			19.7		dBm
Output Voltage - High Power In	PIN = -10dBm		0.710		V
Output Voltage- Low Power In	PIN = -50dBm		1.69		V
Temperature Sensitivity	PIN = -10dBm				
	25°C ≤ T_A ≤ +85°C		0.00106		dB/ °C
	-25°C ≤ T_A ≤ +25°C		0.00377		dB/ °C
	-40°C ≤ T_A ≤ +25°C		0.00447		dB/ °C

Parameter	Conditions	Min	Typ	Max	Unit
f = 3.60 GHz					
± 1 dB Dynamic Range	–40°C < T_A < +85°C		39		dB
Maximum Input Level	± 1 dB Error		-5		dBm
Minimum Input Level	± 1 dB Error		-58		dBm
Slope			-24.4		mV/dB
Intercept			19		dBm
Output Voltage - High Power In	PIN = -10dBm		0.704		V
Output Voltage- Low Power In	PIN = -50dBm		1.68		V
Temperature Sensitivity	PIN = -10dBm				
	25°C ≤ T_A ≤ +85°C		-0.0001		dB/ °C
	-25°C ≤ T_A ≤ +25°C		0.0049		dB/ °C
	-40°C ≤ T_A ≤ +25°C		0.0071		dB/ °C
f = 5.8 GHz					
± 1 dB Dynamic Range	–40°C < T_A < +85°C		50		dB
Maximum Input Level	± 1 dB Error		0		dBm
Minimum Input Level	± 1 dB Error		-58		dBm
Slope			-24.2		mV/dB
Intercept			25.4		dBm
Output Voltage - High Power In	PIN = -10dBm		0.810		V
Output Voltage- Low Power In	PIN = -50dBm		1.81		V
Temperature Sensitivity	PIN = -10dBm				
	25°C ≤ T_A ≤ +85°C		0.0038		dB/ °C
	-25°C ≤ T_A ≤ +25°C		0.0113		dB/ °C
	-40°C ≤ T_A ≤ +25°C		0.0096		dB/ °C
f = 8.0 GHz					
± 3 dB Dynamic Range	–40°C < T_A < +85°C		58		dB
Maximum Input Level	± 3 dB Error		3		dBm
Minimum Input Level	± 3 dB Error		-55		dBm
Slope			-22.7		mV/dB
Intercept			37		dBm
Output Voltage - High Power In	PIN = -10dBm		1.02		V
Output Voltage- Low Power In	PIN = -50dBm		1.93		V
Temperature Sensitivity	PIN = -10dBm				
	25°C ≤ T_A ≤ +85°C		0.03		dB/ °C
	-25°C ≤ T_A ≤ +25°C		-0.011		dB/ °C
	-40°C ≤ T_A ≤ +25°C		-0.009		dB/ °C
OUTPUT INTERFACE	**VOUT** (pin 6)				
Voltage Swing		0		3.9	V
Output Current Drive	Vset = 1.5 volts, RFIN = -50 dBm		60		mA
Output Noise	RF Input = 2.2 GHz, -10 dBm, f_{NOISE} = 100 kHz, CLPF = 220 pF		100		nV/√Hz
Fall Time	Input Level = off to -10 dBm, 90 to 10 %		8		ns
Rise Time	Input Level = -10 dBm to off, 10 to 90 %		13		ns

Parameter	Conditions	Min	Typ	Max	Unit
VSET INTERFACE	**VSET** (pin 7)				
Nominal Input Range		0.5		2.1	V
Logarithmic Scale Factor			-0.04		dB/mV
Input Resistance			500		kΩ
TEMPERATURE REFERENCE	**TEMP** (pin 13)				
Output Voltage	T_A = 25°C, R_L = 10kΩ		0.6		V
Temperature Slope	-40°C ≤ T_A ≤ +85°C, R_L = 10kΩ		2		mV/ °C
Current Source/Sink	T_A = 25°C		10/0.1		mA
POWERDOWN INTERFACE	**ENBL** (pin 16)				
Logic Level to Enable Device			1.7		V
ENBL Current When Enabled	*ENBL* = 5V		1		µA
ENBL Current When Disabled	*ENBL* = 0V		20		µA
POWER INTERFACE	**VPSI** (pins 3, 4), **VPSO** (pin 9)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	*ENBL* = 5V		65		mA
vs. Temperature	-40°C ≤ T_A ≤ +85°C		69		mA
Supply Current when Disabled	*ENBL* = 0V, Total Currents for **VPSI** & **VPSO**		300		µA
vs. Temperature	-40°C ≤ T_A ≤ +85°C		350		µA

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8318 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage: **VPS0, VPSI**	5.7 V
ENBL, VSET Voltage	0 to 5.7 V
Input Power (Single-ended, re: 50Ω)	12 dBm
Internal Power Dissipation	TBD
θ_{JA}	TBD °C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

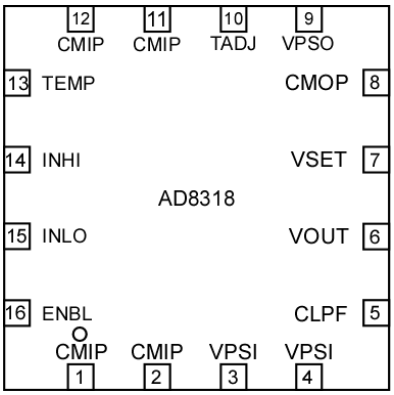


Figure 2. 16-Lead Leadframe Chip Scale Package (LFCSP)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 11, 12	**CMIP**	Device common (input system ground)
3,4	**VPSI**	Positive supply voltage for the device input system: +4.5V to 5.5V
5	**CLPF**	Loop Filter Capacitor
6	**VOUT**	Measurement and Controller output
7	**VSET**	Set-point control input for controller mode, or feedback input for measurement mode
8	**CMOP**	Device common (output system ground)
9	**VPSO**	Positive supply voltage for the device output system: +4.5V to 5.5V
10	**TADJ**	Temperature compensation adjustment
13	**TEMP**	Temperature sensor output
14	**INHI**	RF input. Nominal input range -60 dBm to 0 dBm re: 50 Ω
15	**INLO**	RF Common for **INHI**
16	**ENBL**	Device Enable. Connect to **VPSI** for normal operation. Connect pin to ground for disable mode.
	Paddle	Internally connected to **CMIP,** solder to ground

Typical Performance Characteristics AD8318

V_P = 5V, T = 25°C, -40°C, 85°C; CLPF = 220pF; RADJ = 500 Ohms; unless otherwise noted. Colors: 25°C → Black; -40°C → Blue; 85°C → Red

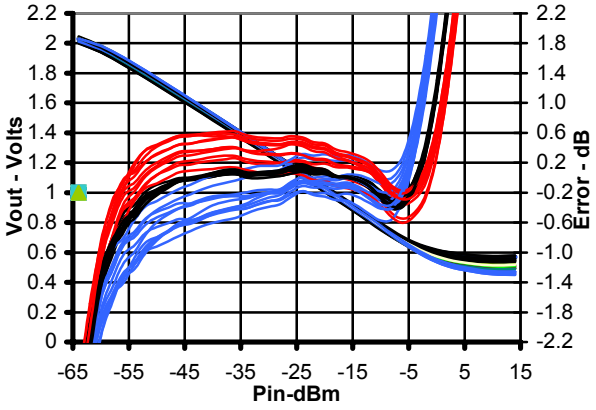


Figure 3. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, multiple devices.

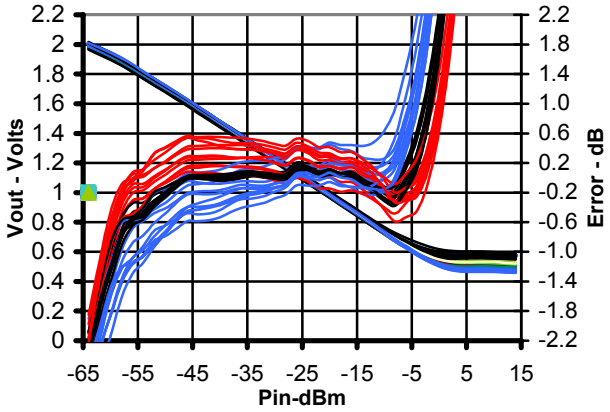


Figure 4. V_{OUT} and Log Conformance vs. Input Amplitude at 1.9GHz, multiple devices.

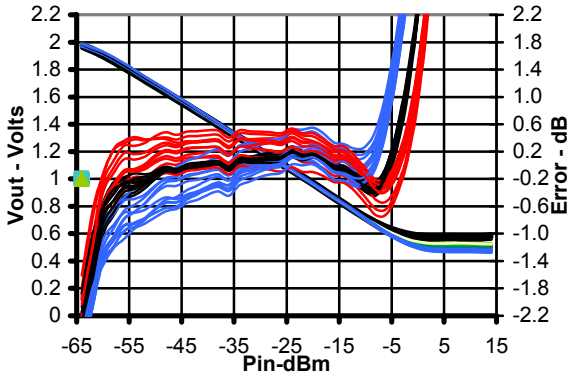


Figure 5. V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz, multiple devices.

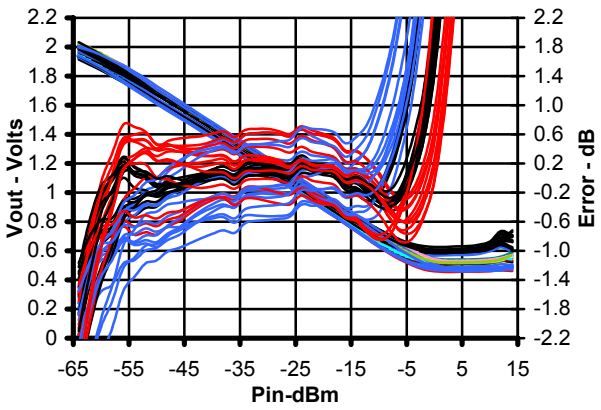


Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 3.6GHz, multiple devices. RADJ = 51 Ohms

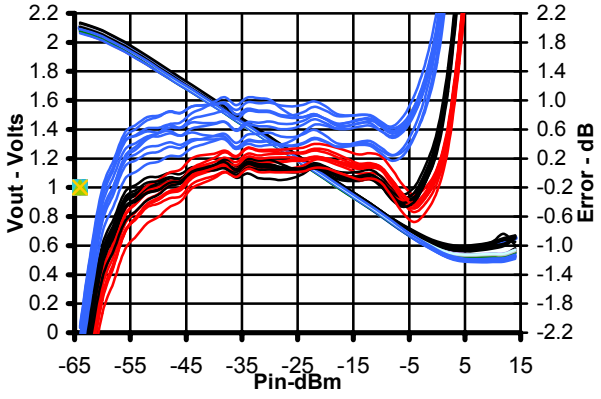


Figure 7 V_{OUT} and Log Conformance vs. Input Amplitude at 5.8 GHz, multiple devices. RADJ=1000 Ohms

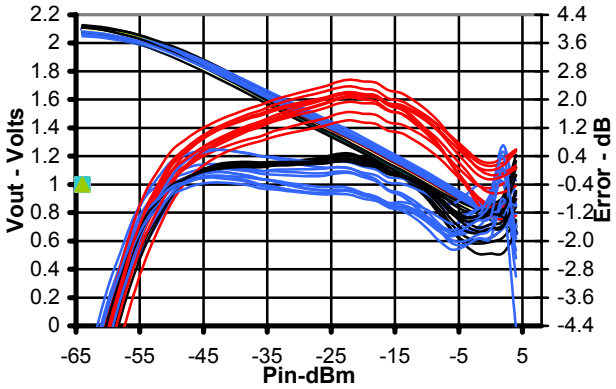


Figure 8. V_{OUT} and Log Conformance vs. Input Amplitude at 8 GHz, multiple devices.

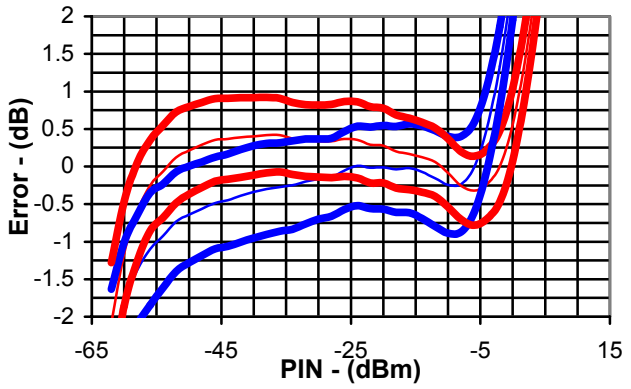


Figure 9. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude, 3 Sigma to either side of mean, 900 MHz

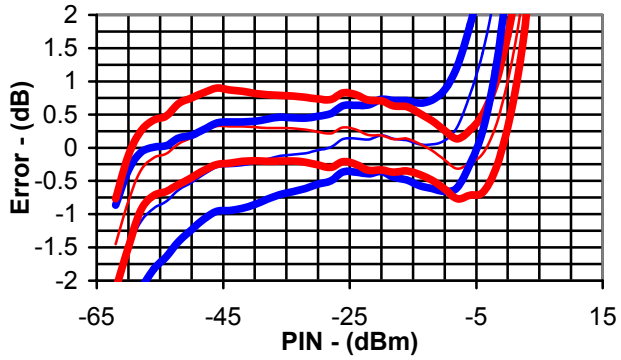


Figure 10. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude, 3 Sigma to either side of mean, 1900 MHz

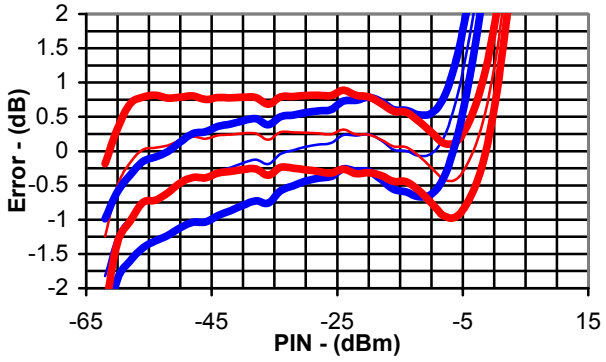


Figure 11. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude, 3 Sigma to either side of mean, 2.2 GHz

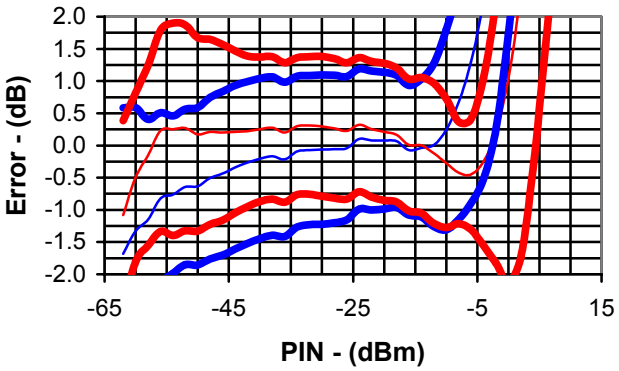


Figure 12. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude, 3 Sigma to either side of mean, 3.6 GHz

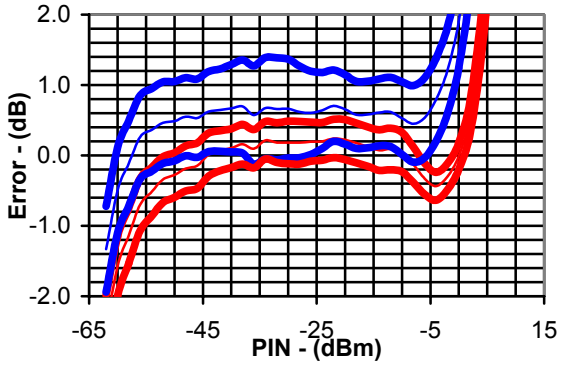


Figure 13. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude, 3 Sigma to either side of mean, 5.8GHz. RADJ=1000 Ohms

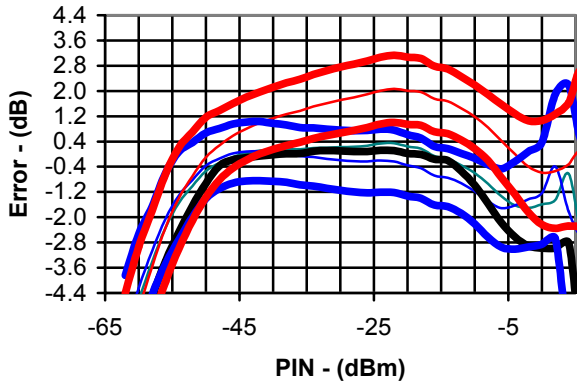


Figure 14. Distribution of Error at Temperature after Ambient Normalization vs. Input Amplitude, 3 Sigma to either side of mean, 8 GHz

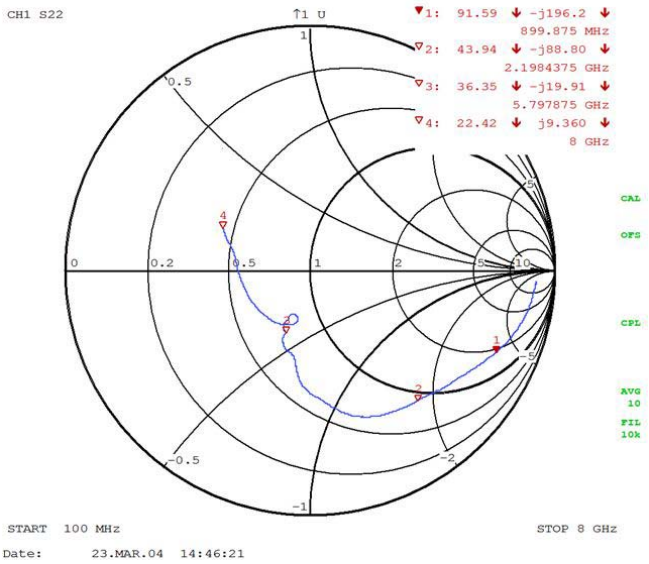


Figure 15. Input Impedance vs. Frequency

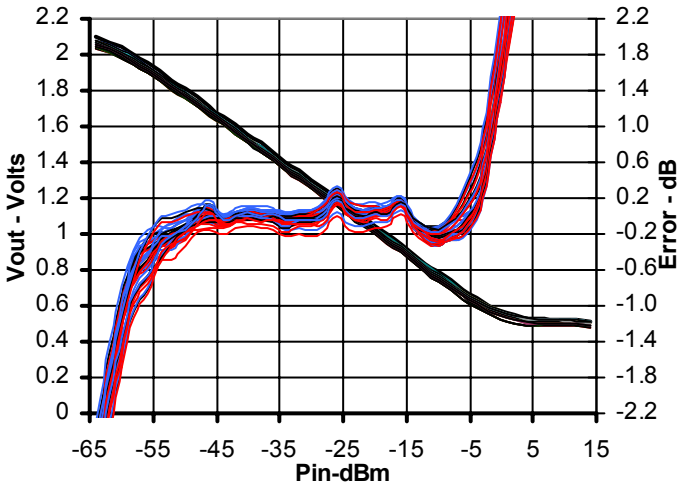


Figure 20.. Output Voltage stability vs. supply voltage at 1.9 GHz when V_P varies by 10%, multiple devices

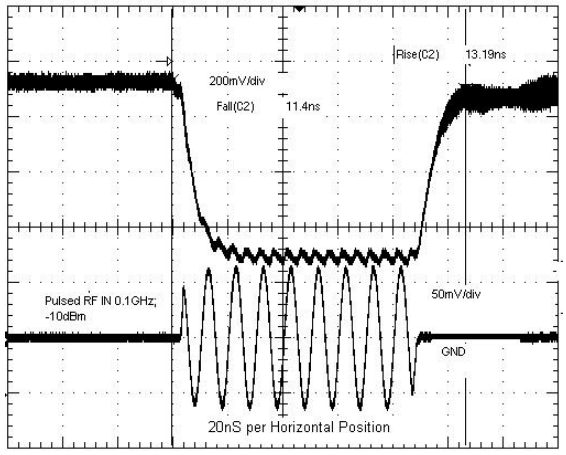


Figure 17. V_{OUT} Pulse Response Time. Pulsed RF Input 0.1GHz, –10dBm; Clpf = Open

GENERAL DESCRIPTION

The AD8318 is a 9-stage demodulating logarithmic amplifier, which provides RF measurement and power amplifier control functions. The design is very similar to the AD8313 Logarithmic Detector/Controller. However, the AD8318 device input frequency range is extended to 8 GHz with 60 dB dynamic range. Other improvements include: reduced intercept variability versus temperature, increased dynamic range at higher frequencies, low noise measurement and controller output (**VOUT**), adjustable low pass corner frequency (**CLPF**), temperature sensor output (**TEMP**), negative transfer function slope and 8 ns response time for RF burst detection capability. A block diagram is shown below in Figure 21.

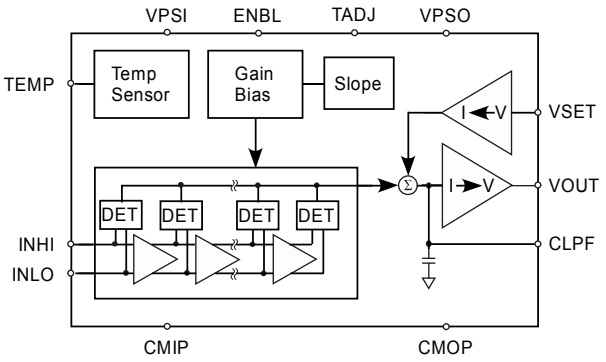


Figure 21. Block Diagram

A fully differential design, on a proprietary high speed SiGe process, is used in extending high frequency performance. Input **INHI** receives the signal with a low frequency impedance of nominally 500 Ω in parallel with 0.7 pF. The maximum input with +1 dB log-conformance error is typically 0 dBm (Re: 50Ω). The noise spectral density referred to the input is 1.15nV/√Hz, which is equivalent to a voltage of 118μV rms in a 10.5 GHz bandwidth, or a noise power of –66 dBm (Re: 50Ω). This noise spectral density sets the lower limit of the dynamic range. However, the low-end accuracy of the AD8318 is enhanced by specially shaping the demodulating transfer characteristic to partially compensate for errors due to internal noise. The input system common pin, **CMIP**, provides a quality low–impedance connection to the printed circuit board (PCB) ground through the use of four package pins. The package paddle, which is internally connected to the **CMIP** pin, should also be grounded to the PCB to reduce thermal impedance from the die to the PCB.

The logarithm function is piece-wise approximated by 9 cascaded gain stages. (For a more comprehensive explanation of the logarithm approximation, please refer to the AD8307 data sheet, available at www.analog.com.) The cells have a nominal voltage gain of 8.7dB each, and a 3dB bandwidth of 10.5GHz.

Using precision biasing, the gain is stabilized over temperature and supply variations. Since the cascaded gain stages are DC coupled, the overall DC gain is high. An offset compensation loop is included to correct for offsets within the cascaded cells. At the output of each of the gain stages, a square-law detector cell is used to rectify the signal. The RF signal voltages are converted to a fluctuating differential current having an average value that increases with signal level. Along with the nine gain stages and detector cells, an additional detector is included at the input of the AD8318, altogether providing a 60 dB dynamic range. After the detector currents are summed and filtered, the function $I_D*\log_{10}(V_{IN}/V_{INTERCEPT})$ is formed at the summing node, where I_D is the internally set detector current, V_{IN} is the input signal voltage, and $V_{INTERCEPT}$ is the intercept voltage (i.e. when $V_{IN}=V_{INTERCEPT}$, the output voltage would be 0V, if it were capable of going to 0V).

Measurement Mode

When the V_{OUT} voltage or a portion of the V_{OUT} voltage is fed back to the **VSET** pin, the device operates in measurement mode. As seen in figure 22, the AD8318 has an offset voltage, a negative slope, and a V_{OUT} measurement intercept at the high end of its input signal range.

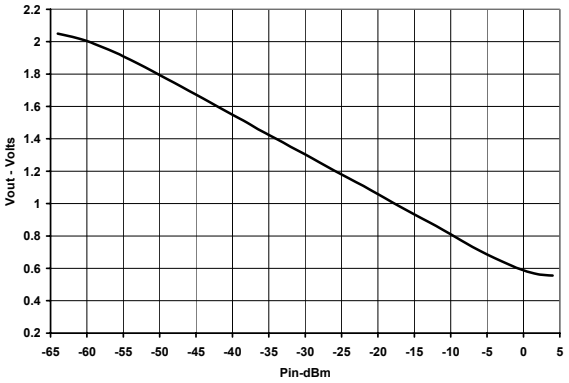


Figure 22. Typical Output Voltage vs. Input Signal

The output voltage versus input signal voltage of the AD8318 is linear-in-dB over a multi-decade range. The equation for this function is of the form

$$V_{OUT} = X * V_{SLOPE/DEC} * \log10(V_{IN}/V_{INTERCEPT})$$

$$= X * V_{SLOPE/dB} * 20 * \log10(V_{IN}/V_{INTERCEPT})$$

where

X is the feedback factor in $V_{SET} = V_{OUT}/X$

$V_{SLOPE/DEC}$ is -500 mV/decade

$V_{SLOPE/dB}$ is approximately -25 mV/dB

$V_{INTERCEPT}$ is the x-intercept of the linear-in-dB portion of the V_{OUT} *vs.* V_{IN} curve. $V_{INTERCEPT}$ is +7dBV for a sinusoidal input signal

An offset voltage, V_{OFFSET}, of 0.5V is internally added to the detector signal, so that the minimum value for V_{OUT} is X* V_{OFFSET}, so for X = 1, minimum V_{OUT} is 0.5 V.

The slope is very stable versus process and temperature variation. When base-10 logarithms are used, $V_{SLOPE/DECADE}$ represents the "volts/decade", and since a decade corresponds to 20 dB, $V_{SLOPE/DECADE}/20 = V_{SLOPE/dB}$ represents the slope in "volts/dB".

As noted in the equations above, the V_{OUT} voltage has a ***negative*** slope. This is also the correct slope polarity to control the gain of many power amplifiers in a negative feedback configuration. Since both the slope and intercept vary slightly with frequency, it is recommended to refer to the specification pages for application specific values for slope and intercept.

Although demodulating log amps respond to input signal voltage, not input signal power, it is customary to discuss the amplitude of high frequency signals in terms of power. In this case, the characteristic impedance of the system, Z_o, must be known to convert voltages to their corresponding power levels. The following equations are used to perform this conversion.

$P(dBm) = 10 * \log_{10}(V_{rms}^2/(Z_O * 1mW))$
$P(dBV) = 20 * \log_{10}(V_{rms}/1V_{rms})$
$P(dBm) = P(dBV) - 10*\log_{10}(Z_O * 1mW/1V_{rms}^2)$

For example, $P_{INTERCEPT}$ for a sinusoidal input signal is expressed in terms of dBm (decibels referred to 1 mW), in a 50Ω system is:

$P_{INTERCEPT}(dBm) = P_{INTERCEPT}(dBV) - 10*\log10(Zo * 1mW/1V_{rms}^2)$
$= +7 \text{ dBV} - 10*\log_{10}(50*10^{-3}) = +20 \text{ dBm}$

For a square wave input signal in a 200Ω system,

$P_{INTERCEPT} = 4 \text{ dBV} - 10*\log_{10}(200\Omega*1mW/1V_{rms}^2)] = +11 \text{ dBm}$

Further information on the intercept variation dependence upon waveform can be found in the AD8313 and AD8307 data sheets.

Controller Mode

The AD8318 provides a controller mode feature at the **VOUT** pin. Using V_{SET} for the set-point voltage, it is possible for the AD8318 to control subsystems, such as power amplifiers (PAs), variable gain amplifiers (VGAs) or variable attenuators (VVAs) that have output power that is monotonic with respect to their gain control signal.

To operate in controller mode, the link between **VSET** and **VOUT** is broken. A setpoint voltage is applied to the **VSET** input; **VOUT** is connected to the gain control terminal of the variable gain amplifier (VGA) and the detector's RF input is connected to the output of the VGA (usually using a directional coupler and some additional attenuation). Based on the defined relationship between V_{OUT} and the RF input signal when the device is in measurement mode, the AD8318 will adjust the voltage on **VOUT** (in controller mode) until a the level at the RF input corresponds to the applied V_{SET}. So when the AD8318 operates in controller mode, there is no defined relationship between V_{SET} and the V_{OUT} voltage; V_{OUT} will settle to a value that results in the correct input signal level appearing at INHI/INLO.

In order for this output power control loop to be stable, a ground-referenced capacitor must be connected to the C_{FLT} pin. This capacitor integrates the error signal (which is actually a current) that is present when the loop is not balanced.

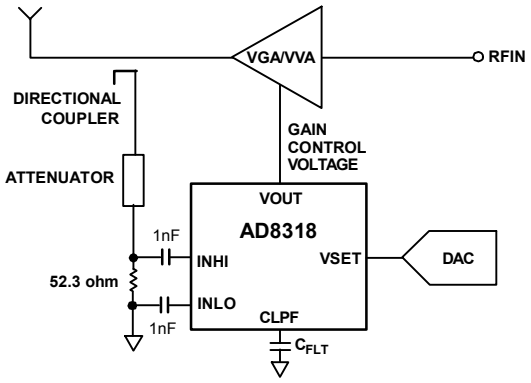


Figure 23 Controller Mode

Decreasing V_{SET}, which corresponds to demanding a higher signal from the VGA, will tend to increase V_{OUT}. The gain of the variable gain element must be proportional to the gain-control of the element..

V_{SET} Interface

The V_{SET} input drives the high impedance (250 kΩ) input of an internal op-amp. The V_{SET} voltage appears across the internal 3.13kΩ resistor to generate I_{SET}. When a portion of V_{OUT} is applied to **VSET**, the feedback loop forces $-I_D*\log_{10}-(V_{IN}/V_{INTERCEPT}) = I_{SET}$. If $V_{SET} = V_{OUT}/X$, then $I_{SET} = V_{OUT}/(X*3.13k\Omega)$. The result is:

$V_{OUT} = (-I_D*3.13k*X)*\log_{10}(V_{IN}/V_{INTERCEPT})$

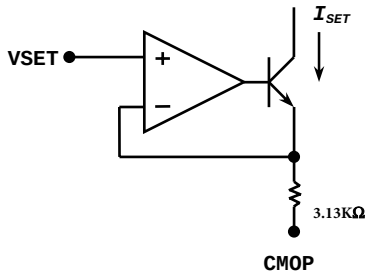


Figure 24. VSET Interface

The slope is given by $-I_D*X*3.13k\Omega = -500mV*X$. For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, then X=2. The slope will be set to -1V/decade or -50mV/dB.

Output Interface

The **VOUT** pin is driven by an PNP output stage. An internal 10Ω resistor is placed in series with the emitter follower output and the **VOUT** pin. The rise time of the output is limited mainly by the slew on **CLPF**. The fall time is an RC limited slew given by the load capacitance and the pull down resistance at **VOUT**. There is an internal pull down resistor of 350Ω. Any resistive load at **VOUT** is placed in parallel with the internal pull-down resistor and provides additional discharge current. For maximal slew rate at **VOUT**, minimize stray capacitance at **VOUT**, leave the **CLPF** pin unconnected, and drive a 50Ω load via a 40Ω back-match resistor.

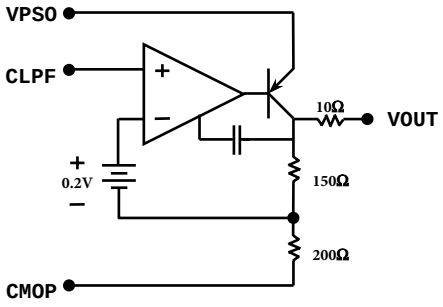


Figure 25 AD8318 Output Interface

Response Time Capability

The AD8318 has a 8 ns rise/fall time capability (10-90%) for input power switching between the noise floor and 0dBm. This capability enables RF burst measurements at repetition rates to beyond 60MHz. In most measurement applications, the AD8318 will have an external capacitor connected to **CLPF** to provide additional filtering for **VOUT**. However, the use of the **CLPF** capacitor slows the response time. For an application requiring maximum RF burst detection capability, the **CLPF** capacitor pin should be left unconnected. In this case, the integration function is provided by the 700fF on-chip capacitor. Since there is a 10Ω internal resistor in series with the output driver, a 40Ω back-match resistor is required when driving a 50Ω coaxial cable. The AD8318 has the drive capability to drive a 50Ω load at the end of the coaxial cable or transmission line. See figure 25.

When other transmission medium impedances are used, the appropriate back-match resistor must be provided. It is recommended that the back-match resistor be placed close to the **VOUT** pin.

Input Interface

The Smith chart depicted in Figure 15. gives the AD8318's typical input impedance. At DC, the resistance is typically 2 kΩ. At frequencies up to 1GHz, the impedance is approximated as 500Ω||0.7pF. The RF input pins are coupled to a network given by the simplified schematic below.

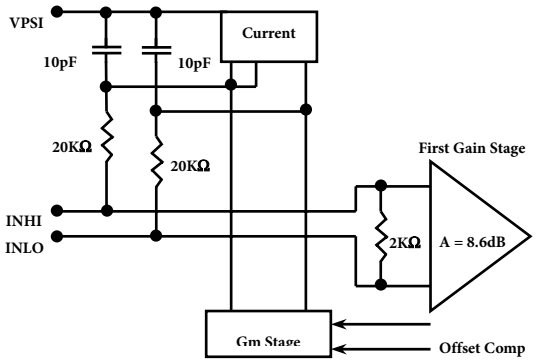


Figure 26. AD8318 Input Interface

The device must be AC coupled through external coupling capacitors. Suggested coupling capacitors are 1nF ceramic 0402 style capacitors, for input frequencies of 1MHz to 8GHz. The coupling capacitors should be mounted close to the **INHI** and **INLO** pins. The coupling capacitor values can be increased to lower the input stage's high-pass cutoff frequency. The high-pass corner is set by the input coupling capacitors and the internal 10pF high-pass capacitor. The DC voltage on **INHI** and **INLO** will be about one diode voltage drop below V_{PSI}.

Temperature Compensation Interface

The primary component of the variation in V_{OUT} versus temperature, as the input signal amplitude is held constant, is drift of the intercept. This drift is also a weak function of

the input signal frequency, so provision is made for optimization of internal temperature compensation at a given frequency by providing pin **TADJ**.

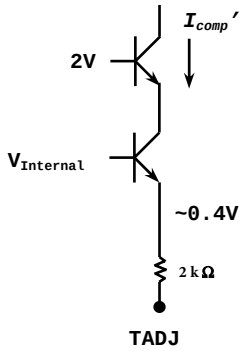


Figure 27. TADJ Interface

A resistor, nominally 500 Ω for optimal temperature compensation at 2.2 GHz input frequency, is connected between this pin and ground. The value of this resistor partially determines the magnitude of an analog correction coefficient which is employed to reduce intercept drift.

Temperature Sensor Interface

The AD8318 internally generates a voltage that is proportional-to-absolute-temperature (VPTAT). The VPTAT voltage is multiplied bya factor of 5 which scales V_{TEMP} for a +2mV/°C change in output voltage versus temperature variation. The output voltage at 27°C is typically 600mV. An emitter follower drives the **TEMP** pin, as shown in figure 28.

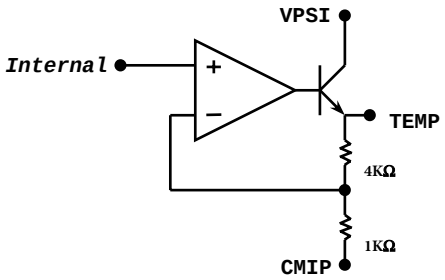


Figure 28. AD8318 Temp Sensor Interface

The internal pull down resistance is 5kΩ. The slope of the temperature sensor (2mV/°C) changes slightly when driving loads less than 1kΩ. Refer to Figure X. for V_{TEMP} slope versus load resistance performance.

Enable Interface

The enable interface has high input impedance. The voltage on **ENBL** must be greater than 2 V_{BE} to enable the device. A 200Ω resistor is placed in series with the **ENBL** input for added protection.

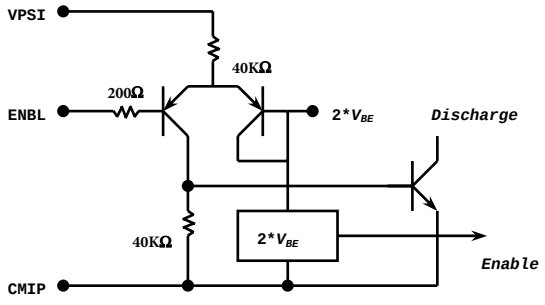


Figure 29. ENBL Interface

Power Supply Interface

Since the AD8318 can handle input frequencies ≥ 6 GHz, it is desired to have low impedance supply pins with adequate isolation between functions that are noisy and output cells. In the AD8318, two positive supply pins must be connected to the same potential. The **VPSI** pin biases the input circuitry, while the **VPSO** biases the low noise output driver for **VOUT**. Separate commons are also included in the device. **CMOP** is used as the common for the output drivers.

USING THE AD8318

Basic Connections

A power supply voltage of between 4.5 V and 5.5 V should be applied to pins VPS0 and VPS1. The supply to these pins should be the same. 100 pF and 0.1 uF power supply decoupling capacitors should be connected close to each power supply pin (the two adjacent VPS1 pins can share a pair of decoupling capacitors because of their proximity).

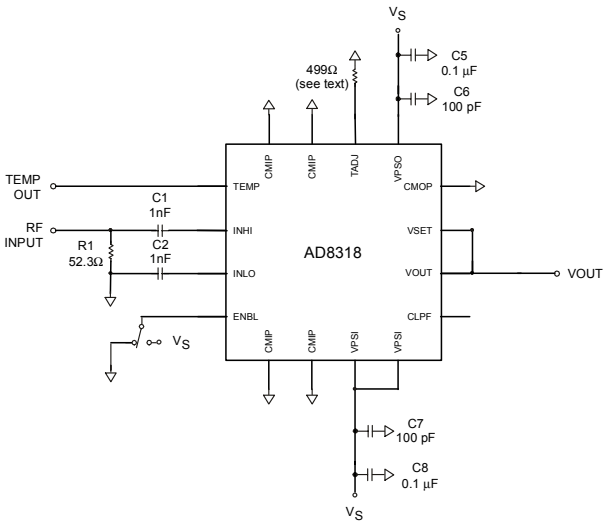


Figure 30. Basic Connections

The paddle of the AD8318's LFCSP package is internally connected to **CMIP**. For optimum thermal and electrical performance, the paddle should be soldered to a low impedance ground plane.

To enable the AD8318, the ENBL pin must be pulled high. Taking **ENBL** low will put the AD8318 in sleep mode, reducing current consumption to 300 uA.

Logarithmic Slope

To operate in measurement mode, **VOUT** must be connected to **VSET**. Connecting **VOUT** directly to **VSET** yields the nominal logarithmic slope of approximately -25 mV/dB. The output swing corresponding the specified input range will then be approximately 0.5 to 2.1 V. The slope and output swing can be increased by placing a resistor divider between **VOUT** and **VSET** (i.e. one resistor from **VOUT** to **VSET** and one resistor from **VSET** to common). For example, if two equal resistors are used (e.g. 10 kΩ/10 kΩ), the slope will double to approximately -50 mV/dB. The input impedance of **VSET** is approximately 500 KΩ. Slope setting resistors should be kept below ~50 kΩ to prevent this input impedance from affecting the resulting slope.

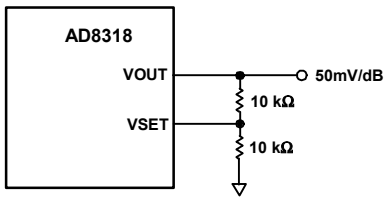


Figure 31. Increasing the Slope

Input Signal Coupling

The RF input to the AD8318 (INHI) is single-ended and must be ac-coupled. INLO (input common) should be ac-coupled to ground

While the input can be reactively matched, in general this is not necessary. An external 52.3 Ω ohm shunt resistor (connected on the signal side of the input coupling capacitors) combines with the relatively high input impedance to give an adequate broadband 50 Ω match.

Temperature Compensation

The temperature drift of the output voltage of the AD8318 can be improved by connecting a ground referenced resistor to the TADJ pin. Table 4 lists recommended resistors for various frequencies. These resistors have been chosen to provide the best overall temperature drift based on measurements of a large population of devices. The value of the TADJ resistor can also be adjusted on a device-by-device basis. This however individual uncompensated temperature drift of each device be measured.

The relationship between output temperature drift and frequency is not linear and cannot be easily modeled. As a result, experimentation is required to choose the correct R_{ADJ} resistor at frequencies not listed in the table below.

Table 4 – Recommended TADJ Resistors

Frequency	Recommended R_{ADJ}
900 MHz	500Ω
1.9 MHz	500Ω
2.2 GHz	500Ω
3.6 GHz	51 Ω
5.8 GHz	1 kΩ
8 GHz	500Ω

EVALUATION BOARD

Table 4. Evaluation Board (Rev A) Configuration Options

Component	Function	Default Conditions
TP1, TP2	**Supply and Ground Connections**	Not Applicable
SW1	**Device Enable**: When in position A, the **ENBL** pin is connected to +VS and the AD8318 is in operating mode. In position B, the **ENBL** pin is grounded through R3, putting the device in power down mode. The **ENBL** pin may be exercised by a pulse generator connected to J3 with SW1 in position B.	SW1 = A R3 = 10k (size 0603)
R1, C1, C2	**Input Interface**: The 53Ω resistor in position R1 combines with the AD8318's internal input impedance to give a broadband input impedance of around 50Ω.•Capacitors C1 and C2 are DC blocking capacitors. A reactive impedance match can be implemented by replacing R1 with an inductor and C1 and C2 with appropriately-valued capacitors .	R2= 52.3Ω (Size 0402) C1 = 1 nF (Size 0402) C2 = 1 nF (Size 0402)
R2	**Temperature Sensor Interface**: The temperature sensor output voltage is available at J1, via the current limiting resistor, R2.	
C4	**Temperature Compensation Interface**: The internal temperature compensation resistor is optimized for an input signal of 2.2 GHz when C4 is 1kΩ. This circuit can be adjusted to optimize performance for other input frequencies by changing the value of the resistor in position C4. Note that the designation C4 on the evaluation board is a typographical error as this pad will always be populated with a resistor. This error will be corrected on the Rev B revision of the board.	C4 = 500 kΩ (Size 0603)
R7, R8, R10	**Output Interface - Measurement Mode**: In measurement mode, a portion of the output voltage is fed back to pin **VSET** via R7. Optionally, a resistor may be installed in position R8 to reduce part-to-part variations in the amount of feedback caused by slight variations in input impedance at pin VSET. The magnitude of the slope of the **VOUT** output voltage response may be increased by reducing the portion of *VOUT* that is fed back to **VSET**. R10 can be used as a back-terminating resistor or as part of a single pole low pass filter.	R7 = 0Ω = (size 0402) R8 = open (size 0402) R9 = open (size 0402 R10= 0Ω (size 0402)
R7, R8, R10	**Output Interface - Controller Mode**: In this mode, R7 must be open. In controller mode, the AD8318 can control the gain of an external component. A set-point voltage is applied to pin **VSET**, the value of which corresponds to the desired RF input signal level applied to the AD8318 RF input.. A sample of the RF output signal from this variable-gain component is selected, typically via a directional coupler, and applied to AD8318 RF input. The voltage at pin **VOUT** is applied to the gain control of the variable gain element. A control voltage is applied to pin VSET via R9 and R8. The magnitude of the control voltage may optionally be attenuated via the voltage divider comprised of R8 and R9, or a capacitor may be installed in position R8 to form a low pass filter along with R9.	R7 = open (size 0402) R8 = open (size 0402) R9 = 0 Ω (size 0402) R10= 0Ω (size 0402)
C5, C6, C7, C8, R5, R6	**Power Supply Decoupling**: The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8318, a 0Ω series resistor and a 0.1uF capacitor placed nearer to the power supply input pin.	C6 = 100 pF (Size 0402) C7 = 100 pF (Size 0402) C5 = 0.1 µF •Size (Size 0603) C8 = 0.1 µF •Size (Size 0603) R5 = 0 Ω (size 0603) R6 = 0 Ω (size 0603)
C9	**Filter Capacitor**: The low pass corner frequency of the circuit that drives pin **VOUT** can be lowered by placing a capacitor between **CLPF** and ground.	C4 = open Size (Size 0603)

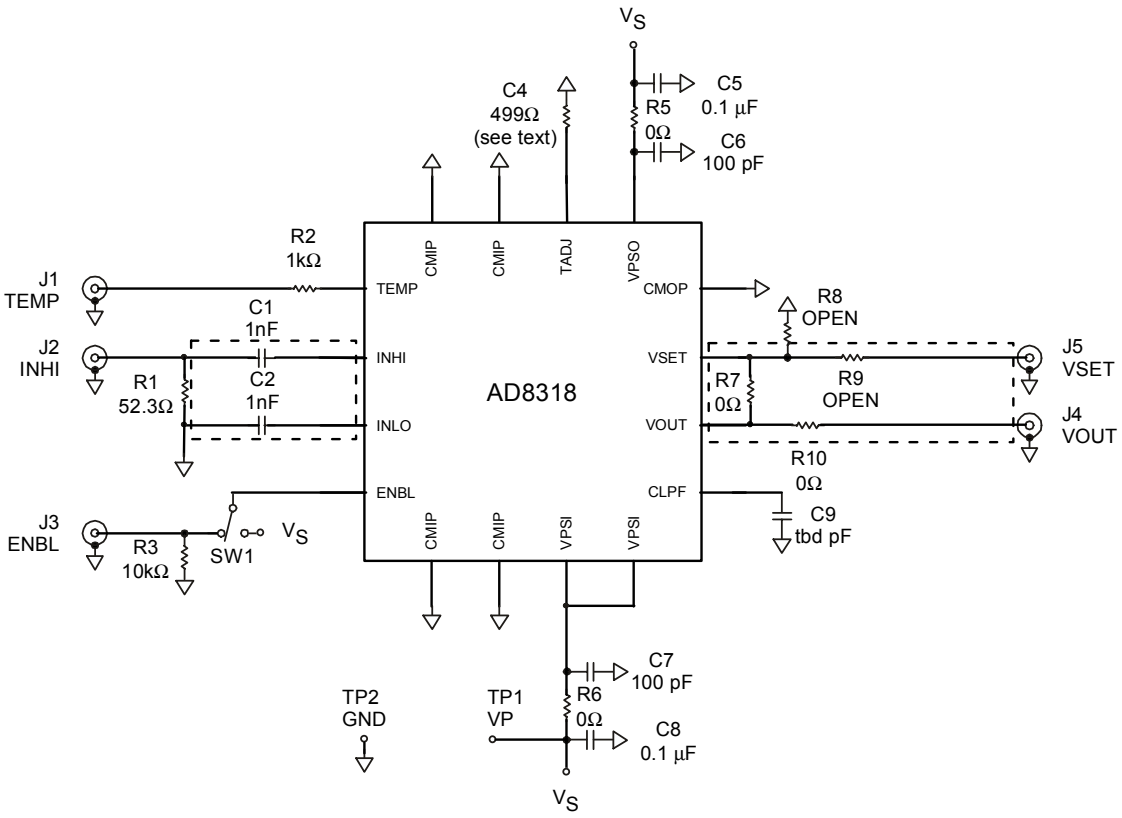


Figure 32. Evaluation Board Schematic (Rev A)

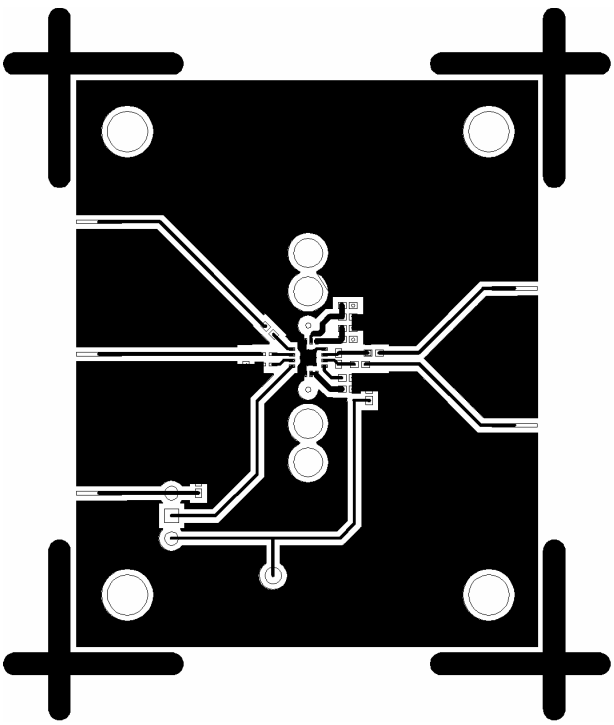


Figure 33. Component Side Layout

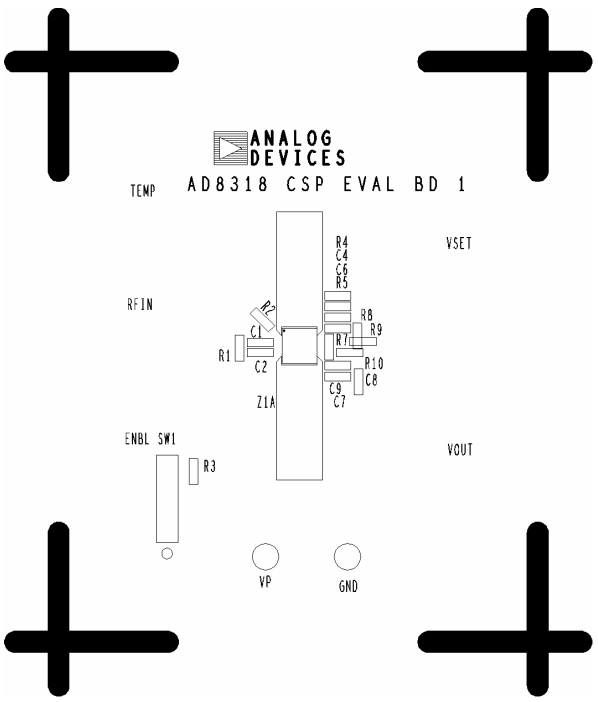
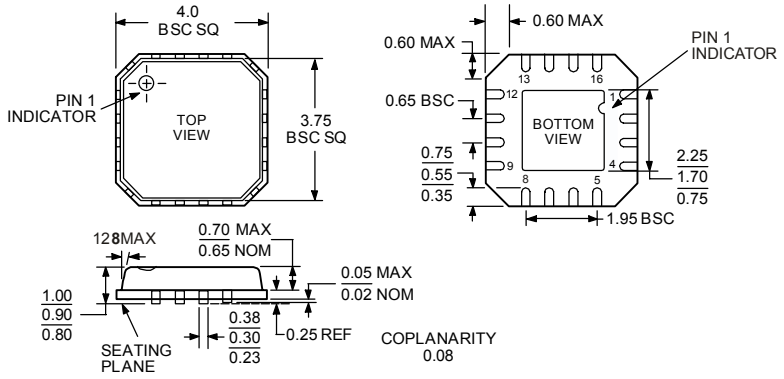


Figure 34. Component Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

16-Lead Chip Scale Package [LFCSP]
4 x 4 mm Body
(CP-16)

Figure 35. 16-Lead Lead Frame Chip Scale Package

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8318 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 5. Ordering Guide

AD8318 Products	Temperature Package	Package Description	Package Outline	Branding
AD8318ACPZ	–40°C to +85°C	16-Lead LFCSP	CP-16	
AD8318-EVAL		Evaluation Board		

PR04853-0-4/04(PrF)

ANALOG DEVICES

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