
Document Title

8M DDR SYNCHRONOUS SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>DraftData</u>	<u>Remark</u>
Rev. 0.0	Initial document.	May 2003	Advance
Rev. 0.1	Change AC CHARACTERISTICS -Remove Bin-40 -Data Setup time -33 : 0.25 -> 0.3 -Data Hold time -33 : 0.25 -> 0.3 -Remove : tqTRK, tcXCV -Add : tcXCH,tcXCL,tchQV,tclQV,tchQX,tclQX,tclQZ,tchlZ Change RECOMMENDED DC OPERATING CONDITIONS -Input Reference Voltage (Max) : 1.0 -> 0.95 Change DC CHARACTERISTICS - Fill up the blank(TBD) - Change Isb1 : 150 -> 100	Sep. 2003	Advance
Rev. 0.2	Change PACKAGE PIN CONFIGURATIONS - Remove the number at DQ pins	Oct. 2003	Advance

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

FEATURES

- 256Kx36 or 512Kx18 Organizations.
- 2.5V V_{DD}/1.5V V_{DDQ}.(1.9V max V_{DDQ})
- HSTL Input and Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write.
- Free Running Active High and Active Low Echo Clock Output Pin.
- Asynchronous Output Enable.
- Registered Addresses, Burst Control and Data Inputs.
- Registered Outputs.
- Double and Single Data Rate Burst Read and Write.
- Burst Count Controllable With Max Burst Length of 4
- Interleaved and Linear Burst mode support
- Bypass Operation Support
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1)
- 153(9x17) Pin Ball Grid Array Package(14mmx22mm)

GENERAL DESCRIPTION

The K7D803671C and K7D801871C are 9,437,184 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 262,144 words by 36 bits for K7D803671C and 524,288 words by 18 bits for K7D801871C, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level clock, K and \bar{K} are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. Data inputs are registered one cycle after write addresses are asserted(Late Write), at the rising edge of K clock for single data rate (SDR) write operations and at rising and falling edge of K clock for a double data rate (DDR) write operations.

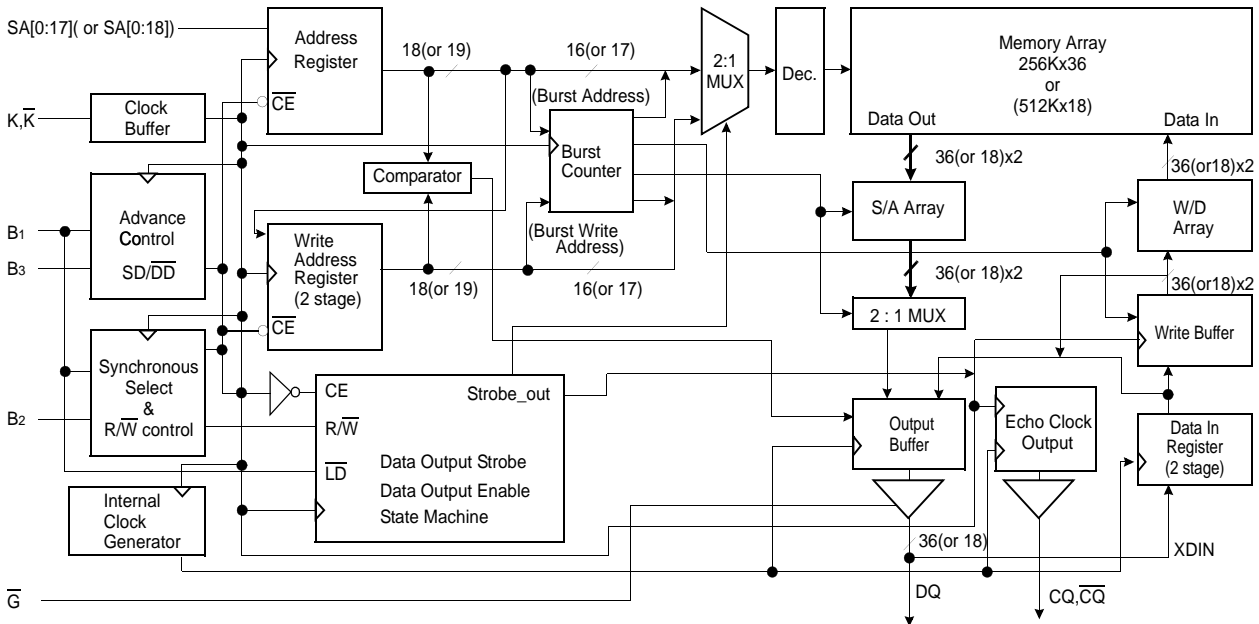
Data outputs are updated from output registers off the rising edges of K clock for SDR read operations and off the rising and falling edges of K clock for DDR read operations. Free running echo clocks are supported which are representative of data output access time for all SDR and DDR operations.

The chip is operated with a single +2.5V power supply and is compatible with Extended HSTL input and output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

ORDERING INFORMATION

Part Number	Organization	Maximum Frequency
K7D803671C-HC37	256Kx36	375MHz
K7D803671C-HC33		333MHz
K7D803671C-HC30		300MHz
K7D801871C-HC37	512Kx18	375MHz
K7D801871C-HC33		333MHz
K7D801871B-HC30		300MHz

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, K̄	Differential Clocks	ZQ	Output Driver Impedance Control Input
SA	Synchronous Address Input	TCK	JTAG Test Clock
SA0, SA1	Synchronous Burst Address Input (SA0 = LSB)	TMS	JTAG Test Mode Select
DQ	Synchronous Data I/O	TDI	JTAG Test Data Input
CQ, CQ̄	Differential Output Echo Clocks	TDO	JTAG Test Data Output
B1	Load External Address	VREF	HSTL Input Reference Voltage
B2	Burst R/W Enable	VDD	Power Supply
B3	Single/Double Data Selection	VDDQ	Output Power Supply
Ḡ	Asynchronous Output Enable	VSS	GND
LBO	Linear Burst Order	NC	No Connection

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7D803671C(256Kx36)

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	DQ	DQ	SA	VSS	B ₁	VSS	SA	DQ	DQ
C	VSS	VDDQ	SA	SA	\overline{G}	SA	SA	VDDQ	VSS
D	DQ	DQ	NC	VSS	VDD	VSS	SA	DQ	DQ
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	DQ	CQ ₁	DQ	VDD	VDD	VDD	DQ	CQ ₂	DQ
G	VSS	VDDQ	VSS	VSS	K	VSS	VSS	VDDQ	VSS
H	DQ	DQ	DQ	VDD	\overline{K}	VDD	DQ	DQ	DQ
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	DQ	DQ	DQ	VSS	B ₂	VSS	DQ	DQ	DQ
L	VSS	VDDQ	VSS	\overline{LBO}	B ₃	MODE	VSS	VDDQ	VSS
M	DQ	$\overline{CQ_1}$	DQ	VDD	VDD	VDD	DQ	$\overline{CQ_2}$	DQ
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	DQ	DQ	NC	VSS	VDD	VSS	SA	DQ	DQ
R	VSS	VDDQ	VDD	SA	SA ₁	SA	VDD	VDDQ	VSS
T	DQ	DQ	SA	VSS	SA ₀	VSS	SA	DQ	DQ
U	VSS	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	VSS

* Mode Pin(6L) is a internally NC.

K7D801871C(512Kx18)

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	NC	DQ	SA	VSS	B ₁	VSS	SA	NC	DQ
C	VSS	VDDQ	SA	SA	\overline{G}	SA	SA	VDDQ	VSS
D	DQ	NC	NC	VSS	VDD	VSS	SA	DQ	NC
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	NC	CQ ₁	NC	VDD	VDD	VDD	DQ	NC	DQ
G	VSS	VDDQ	VSS	VSS	K	VSS	VSS	VDDQ	VSS
H	DQ	NC	DQ	VDD	\overline{K}	VDD	NC	DQ	NC
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	NC	DQ	NC	VSS	B ₂	VSS	DQ	NC	DQ
L	VSS	VDDQ	VSS	\overline{LBO}	B ₃	MODE	VSS	VDDQ	VSS
M	DQ	NC	DQ	VDD	VDD	VDD	NC	$\overline{CQ_1}$	NC
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	NC	DQ	SA	VSS	VDD	VSS	SA	NC	DQ
R	VSS	VDDQ	VDD	SA	SA ₁	SA	VDD	VDDQ	VSS
T	DQ	NC	SA	VSS	SA ₀	VSS	SA	DQ	NC
U	VSS	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	VSS

* Mode Pin(6L) is a internally NC.

Read Operation(Single and Double)

During SDR read operations, addresses and controls are registered at the first rising edge of K clock and then the internal array is read between first and second rising edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During DDR read operations, addresses and controls are registered at the first rising edge of K clock, and then the internal array is read twice between first and second rising edges of K clock. Data outputs are updated from output registers sequentially by burst order off the second rising and falling edge of K clock.

Interleave and linear burst operation is controlled by \overline{LBO} pin and the burst count is controllable with the maximum burst length of 4. To avoid data contention, at least one NOP operations are required between the last read and the first write operation.

Write Operation(Late Write)

During SDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. During DDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered twice at the following rising and falling edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write operation are data inputs fully written into SRAM array.

Echo clock operation

Free running type of Echo clocks are generated from K clock regardless of read, write and NOP operations. They will stop operation only when K clock is in the stop mode.

Echo clocks are designed to represent data output access time and this allows the echo clocks to be used as reference to capture data outputs outputs.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array.

Programmable Impedance Output Driver

The data output and echo clock driver impedance are adjusted by an external resistor, RQ, connected between ZQ pin and Vss, and are equal to $RQ/5$. For example, 250 Ω resistor will give an output impedance of 50 Ω . Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with \overline{G} high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time \overline{G} are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: Vss, VDD, VDDQ, VREF, then VIN. VDD and VDDQ can be applied simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: VIN, VREF, VDDQ, VDD, Vss. VDD and VDDQ can be removed simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-down.

TRUTH TABLE

K	\overline{G}	B1	B2	B3	DQ	Operation
L	X	X	X	X	Hi-Z	Clock Stop
↑	X	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	L	H	H	DOUT	Load Address, Single Read
↑	L	L	H	L	DOUT	Load Address, Double Read
↑	X	L	L	H	DIN	Load Address, Single Write
↑	X	L	L	L	DIN	Load Address, Double Write
↑	X	H	H	X	B	Increment Address, Continue

NOTE : - B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".
- K & \overline{K} are complementary.

BURST SEQUENCE TABLE

4 Burst Operation for Interleaved Burst ($\overline{LBO} = V_{DDQ}$)

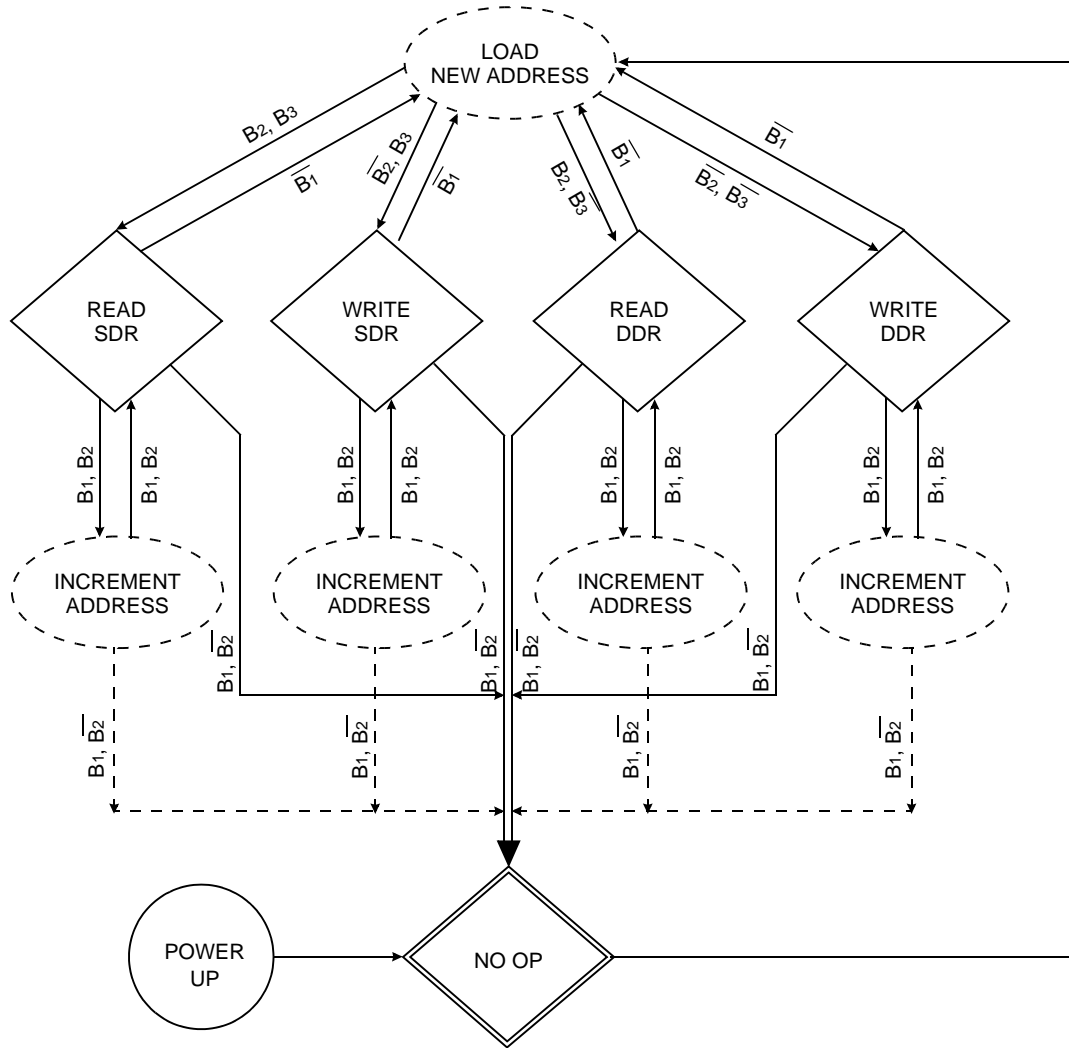
Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

NOTE : - For Interleave Burst $\overline{LBO} = V_{DDQ}$ is recommended. If $\overline{LBO} = V_{DD}$, it must not exceed 2.63V.

4 Burst Operation for Linear Burst ($\overline{LBO} = V_{SS}$)

Linear Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE :

- State transitions ; $\overline{B_1}$ =(Load Address), B_1 =(Increment Address, Continue)
 B_2 =(Read), $\overline{B_2}$ =(Write)
 B_3 =(Single Data Rate), $\overline{B_3}$ =(Double Data Rate)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 3.13	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 2.3	V
Voltage on any pin Relative to Vss	VIN	-0.5 to VDDQ+0.5 (2.3V MAX)	V
Output Short-Circuit Current(per I/O)	IOUT	25	mA
Storage Temperature	TSTR	-55 to 125	°C

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	2.37	2.5	2.63	V	
Output Power Supply Voltage	VDDQ	1.4	1.5	1.9	V	
Input High Level Voltage	VIH	VREF+0.1	-	VDDQ+0.3	V	1, 2
Input Low Level Voltage	VIL	-0.3	-	VREF-0.1	V	1, 3
Input Reference Voltage	VREF	0.68	0.75	0.95	V	

NOTE : 1. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.

2. VIH (Max)DC=VDDQ+0.3, VIH (Max)AC=2.6V (2.1V for DQs) (pulse width ≤ 20% of cycle time).
3. VIL (Min)DC=-0.3V, VIL (Min)AC=-1.0V (-0.5V for DQs) (pulse width ≤ 20% of cycle time).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current(x36) (Cycle time = tKHKH min)	I _{DD37} I _{DD33} I _{DD30}	-	500 450 400	mA	1,2
Average Power Supply Operating Current(x18) (Cycle time = tKHKH min)	I _{DD37} I _{DD33} I _{DD30}	-	450 400 350	mA	1,2
Stop Clock Standby Current (VIN=VDD-0.2V or 0.2V fixed, K=Low, \bar{K} =High)	ISB1	-	100	mA	1
Input Leakage Current (VIN=Vss or VDDQ)	I _{LI}	-1	1	μA	
Output Leakage Current (VOUT=Vss or VDDQ)	I _{LO}	-1	1	μA	
Output High Voltage(Programmable Impedance Mode)	VOH1	VDDQ/2	VDDQ	V	3
Output Low Voltage(Programmable Impedance Mode)	VOL1	Vss	VDDQ/2	V	4
Output High Voltage(I _{OH} =-0.1mA)	VOH2	VDDQ-0.2	VDDQ	V	5
Output Low Voltage(I _{OL} =0.1mA)	VOL2	Vss	0.2	V	5

- NOTE :**
1. Minimum cycle. I_{OUT}=0mA.
 2. 50% read cycles.
 3. |I_{OH}|=(VDDQ/2)/(RQ/5)±15% @VOH=VDDQ/2 for 175Ω ≤ RQ ≤ 350Ω.
 4. |I_{OL}|=(VDDQ/2)/(RQ/5)±15% @VOL=VDDQ/2 for 175Ω ≤ RQ ≤ 350Ω.
 5. Minimum Impedance Mode when ZQ pin is connected to Vss.

PIN CAPACITANCE

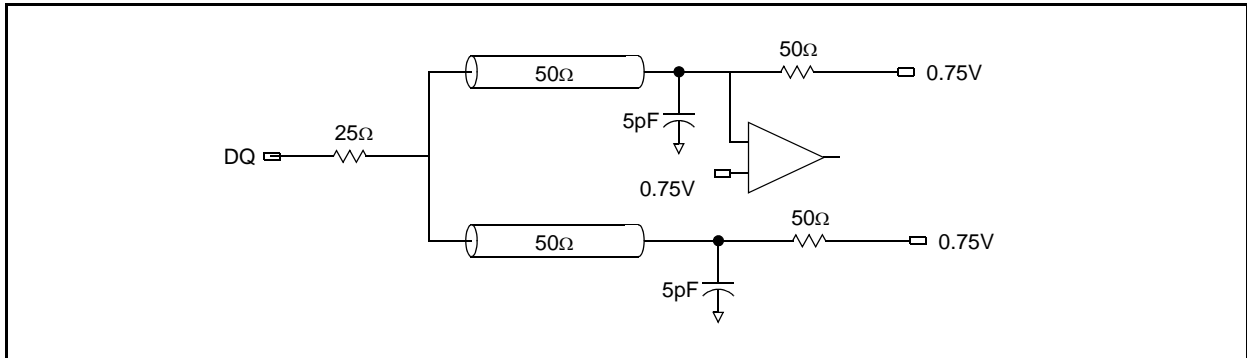
Parameter	Symbol	Test Condition	TYP	Max	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	4	pF
Data Output Capacitance	C _{OUT}	V _{OUT} =0V	-	5	pF

NOTE : Periodically sampled and not 100% tested.(T_A=25°C, f=1MHz)

AC TEST CONDITIONS(T_A=0 to 70°C, V_{DD}=2.37 -2.63V, V_{DDQ}=1.5V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	1.25/0.25	V	-
Input Reference Level	V _{REF}	0.75	V	-
Input Rise/Fall Time	T _R /T _F	0.5/0.5	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load		See Below		-

AC TEST OUTPUT LOAD

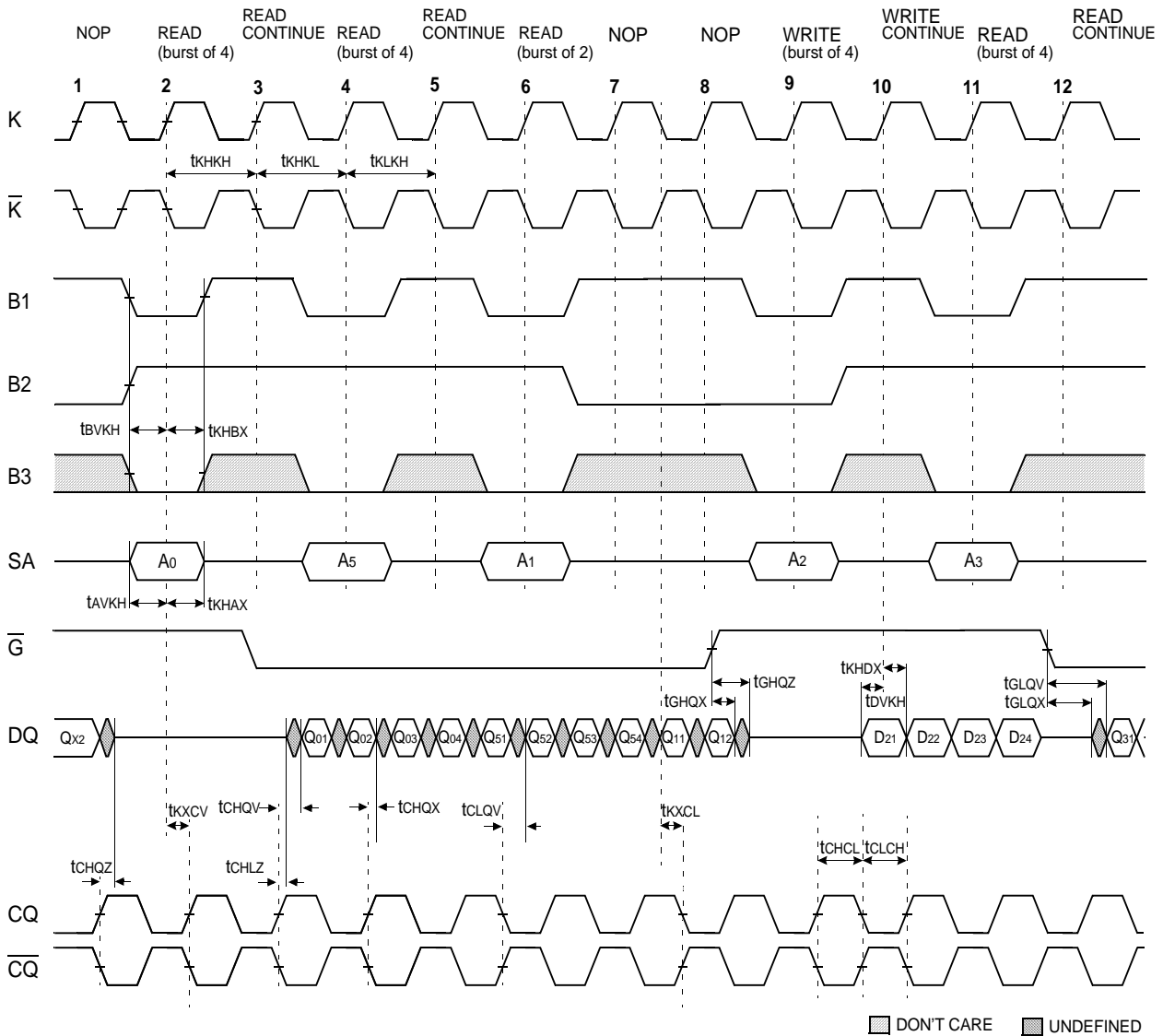


AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-37		-33		-30		UNITS	NOTES
		Min	Max	Min	Max	Min	Max		
Clock									
Clock Cycle Time	tkHKH	2.66	-	3.0	-	3.3	-	ns	1
Clock High Pulse Width	tkHKL	1.3	-	1.3	-	1.5	-	ns	
Clock Low Pulse Width	tkLKH	1.3	-	1.3	-	1.5	-	ns	
Setup Times									
Address Setup Time	tAVKH	0.4	-	0.4	-	0.4	-	ns	
Control(B1,B2,B3) Setup Time	tBVKH	0.4	-	0.4	-	0.4	-	ns	
Data Setup Time	tDVKX	0.25	-	0.3	-	0.3	-	ns	2
Hold Times									
Address Hold Time	tkHAX	0.4	-	0.4	-	0.4	-	ns	
Control(B1,B2,B3) Hold Time	tkHBX	0.4	-	0.4	-	0.4	-	ns	
Data Hold Time	tkXDX	0.25	-	0.3	-	0.3	-	ns	2
Output Times									
Echo Clock High Pulse Width	tCHCL	tkHKL-0.1	tkHKL+0.1	tkHKL-0.1	tkHKL+0.1	tkHKL-0.2	tkHKL+0.2	ns	2
Echo Clock Low Pulse Width	tCLCH	tkLKH-0.1	tkLKH+0.1	tkLKH-0.1	tkLKH+0.1	tkLKH-0.2	tkLKH+0.2	ns	2
Clock Crossing to Echo Clock High	tCXCH	0.5	2.3	0.5	2.3	0.5	2.3	ns	3
Clock Crossing to Echo Clock Low	tCXCL	0.5	2.3	0.5	2.3	0.5	2.3	ns	3
Echo Clock High to Output Vaild	tCHQV	-0.20	0.20	-0.20	0.20	-0.20	0.20	ns	
Echo Clock Low to Output Valid	tCLQV	-0.20	0.20	-0.20	0.20	-0.20	0.20	ns	
Echo Clock High to Output Hold	tCHQX	-0.20		-0.20		-0.20		ns	
Echo Clock Low to Output Hold	tCLQX	-0.20		-0.20		-0.20		ns	
Echo Clock High to Output High-Z	tCHQZ		0.20		0.20		0.20	ns	
Echo Clock High to Output Low-Z	tCHLZ	-0.20		-0.20		-0.20		ns	
\overline{G} Low to Output Valid	tGLQV	-	1.7	-	1.7	-	1.9	ns	4
\overline{G} High to Output Low-Z	tGHQX	0.5		0.5		0.5		ns	4
\overline{G} High to Output High-Z	tGHQZ	-	1.7	-	1.7	-	1.9	ns	4

- Notes:**
1. The maximum cycle time must be limited to guarantee AC timing specification.
 2. This parameter is guaranteed by design, and may not be tested at values shown in the table.
 3. This parameter refers to CQ and \overline{CQ} rising and falling edges.
 4. K and \overline{K} Clocks must be used differentially to meet AC timing specifications.

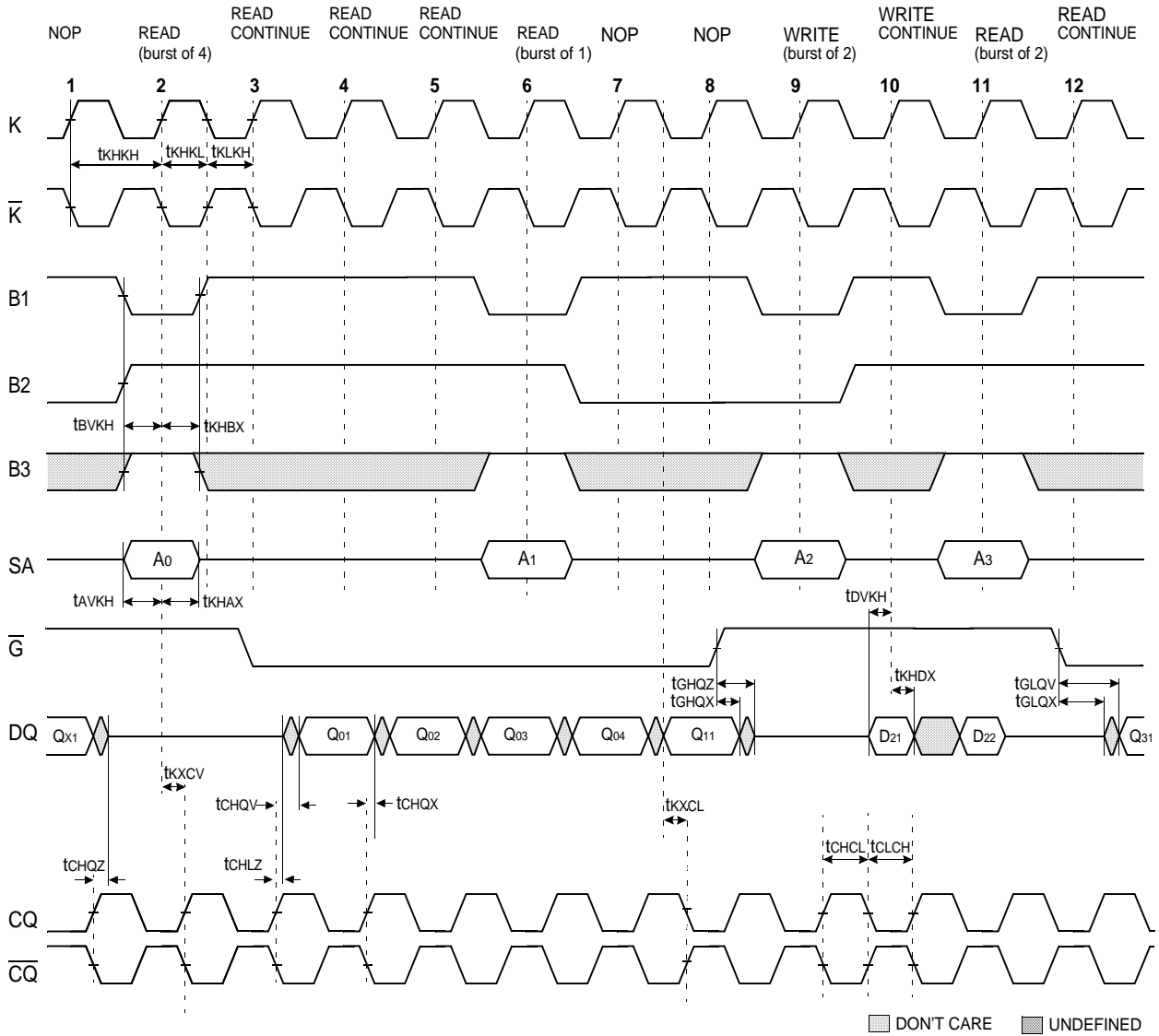
**TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES
(Burst Length=4, 2)**



NOTE

1. Q₀₁ refers to output from address A. Q₀₂ refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.

**TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES
(Burst Length=4, 2, 1)**



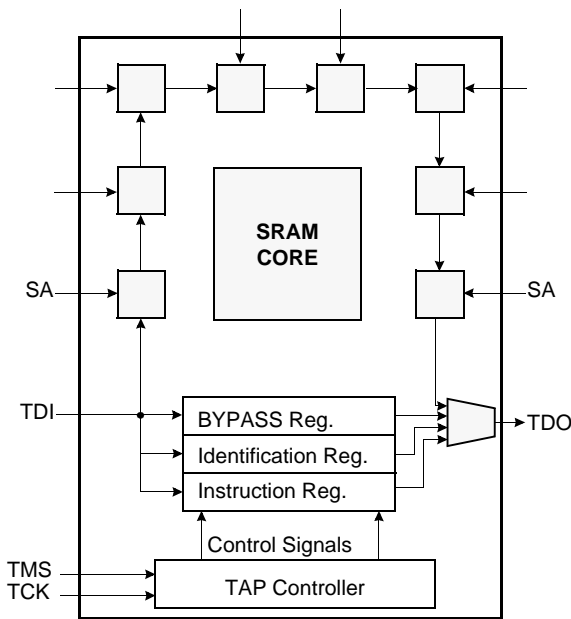
NOTE :

1. Q₀₁ refers to output from address A₀. Q₀₂ refers to output from the next internal burst address following A₀, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. This device supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation. Any further Continue assertions constitute invalid operations.
4. This device will have an address wraparound if further Continues are applied.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and therefore can be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



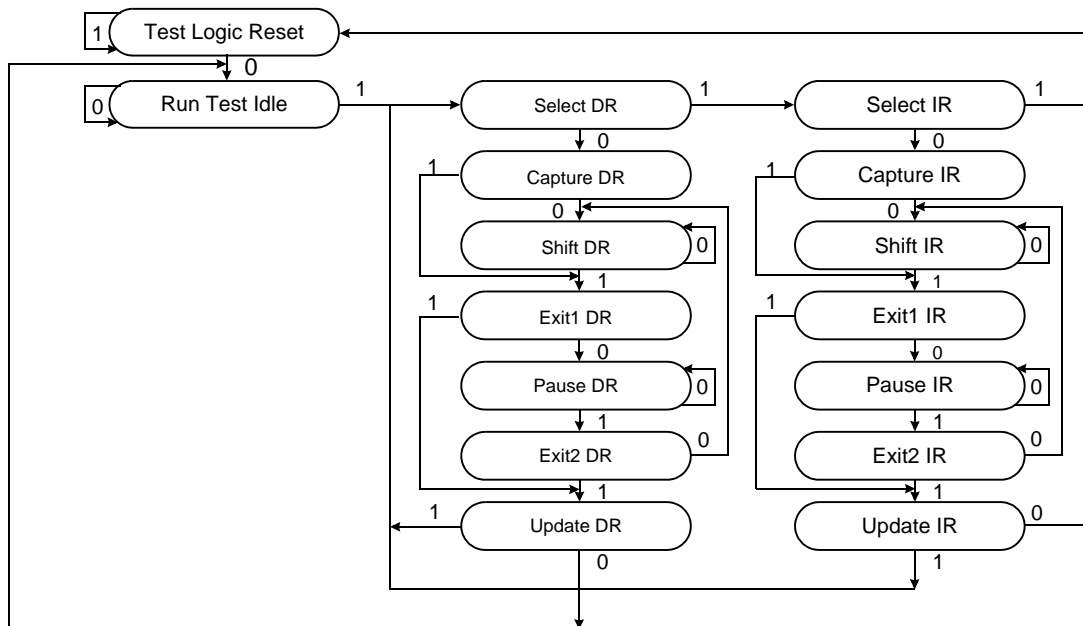
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked.
The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256K x 36	3 bits	1 bits	32 bits	68 bits
512K x 18	3 bits	1 bits	32 bits	49 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
256K x 36	0000	00110 00100	XXXXXX	00001001110	1
512K x 18	0000	00111 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	4A	SA		SA	6A	35
37	4C	SA		SA	6C	34
38	3A	SA		SA	7A	33
39	3B	SA		SA	7B	32
40	3C	SA		SA	7C	31
41	3D	NC		SA	7D	30
42	2B	DQ		DQ	8B	29
43	1B	DQ		DQ	9B	28
44	2D	DQ		DQ	8D	27
45	3F	DQ		DQ	7F	26
46	1D	DQ		DQ	9D	25
47	2F	CQ		CQ	8F	24
48	1F	DQ		DQ	9F	23
49	3H	DQ		DQ	7H	22
50	2H	DQ		DQ	8H	21
51	1H	DQ		DQ	9H	20
52	5A	ZQ		\bar{G}	5C	19
53	5B	B ₁		K	5G	18
54	5K	B ₂		\bar{K}	5H	17
55	5L	B ₃	MODE		6L	16
56	4L	\bar{LBO}		DQ	9K	15
57	1K	DQ		DQ	8K	14
58	2K	DQ		DQ	7K	13
59	3K	DQ		DQ	9M	12
60	1M	DQ		\bar{CQ}	8M	11
61	2M	\bar{CQ}		DQ	9P	10
62	1P	DQ		DQ	7M	9
63	3M	DQ		DQ	8P	8
64	2P	DQ		DQ	9T	7
65	1T	DQ		DQ	8T	6
66	2T	DQ		SA	7P	5
67	3T	SA		SA	7T	4
68	4R	SA		SA	6R	3
				SA	5T	2
				SA	5R	1

* Reserved for Mode Pin

BOUNDARY SCAN EXIT ORDER(x18)

26	4A	SA		SA	6A	25
27	4C	SA		SA	6C	24
28	3A	SA		SA	7A	23
29	3B	SA		SA	7B	22
30	3C	SA		SA	7C	21
31	3D	NC		SA	7D	20
32	2B	DQ				
				DQ	9B	19
				DQ	8D	18
				DQ	7F	17
33	1D	DQ				
34	2F	CQ				
				DQ	9F	16
35	3H	DQ				
				DQ	8H	15
36	1H	DQ				
37	5A	ZQ		\bar{G}	5C	14
38	5B	B ₁		K	5G	13
39	5K	B ₂		\bar{K}	5H	12
40	5L	B ₃	MODE		6L	11
41	4L	\bar{LBO}		DQ	9K	10
42	2K	DQ		DQ	7K	9
43	1M	DQ		\bar{CQ}	8M	8
				DQ	9P	7
44	3M	DQ				
45	2P	DQ				
46	1T	DQ		DQ	8T	6
				SA	7P	5
47	3P	SA		SA	7T	4
48	3T	SA		SA	6R	3
49	4R	SA		SA	5T	2
				SA	5R	1

* Reserved for Mode Pin

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	2.37	2.5	2.63	V	
Input High Level	V _{IH}	1.7	-	V _{DD} +0.3	V	
Input Low Level	V _{IL}	-0.3	-	0.7	V	
Output High Voltage(I _{OH} =-2mA)	V _{OH}	2.1	-	V _{DD}	V	
Output Low Voltage(I _{OL} =2mA)	V _{OL}	V _{SS}	-	0.2	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

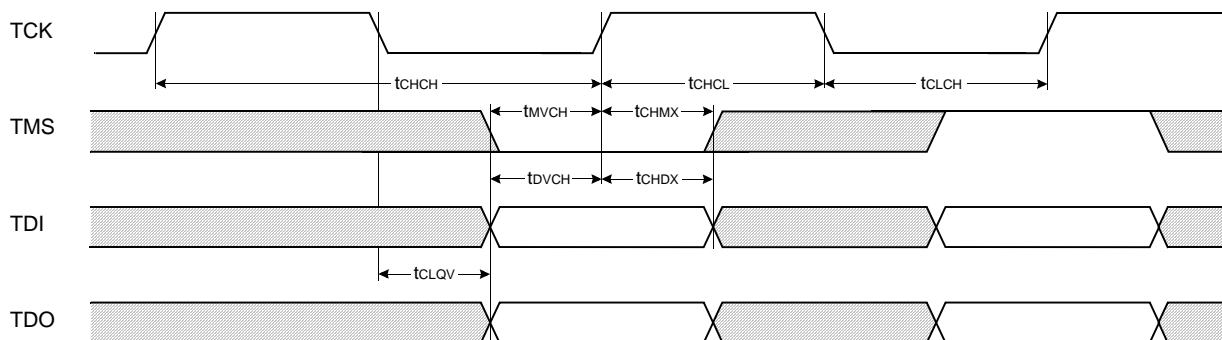
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.25	V	1

NOTE : 1. See SRAM AC test output load on page 5.

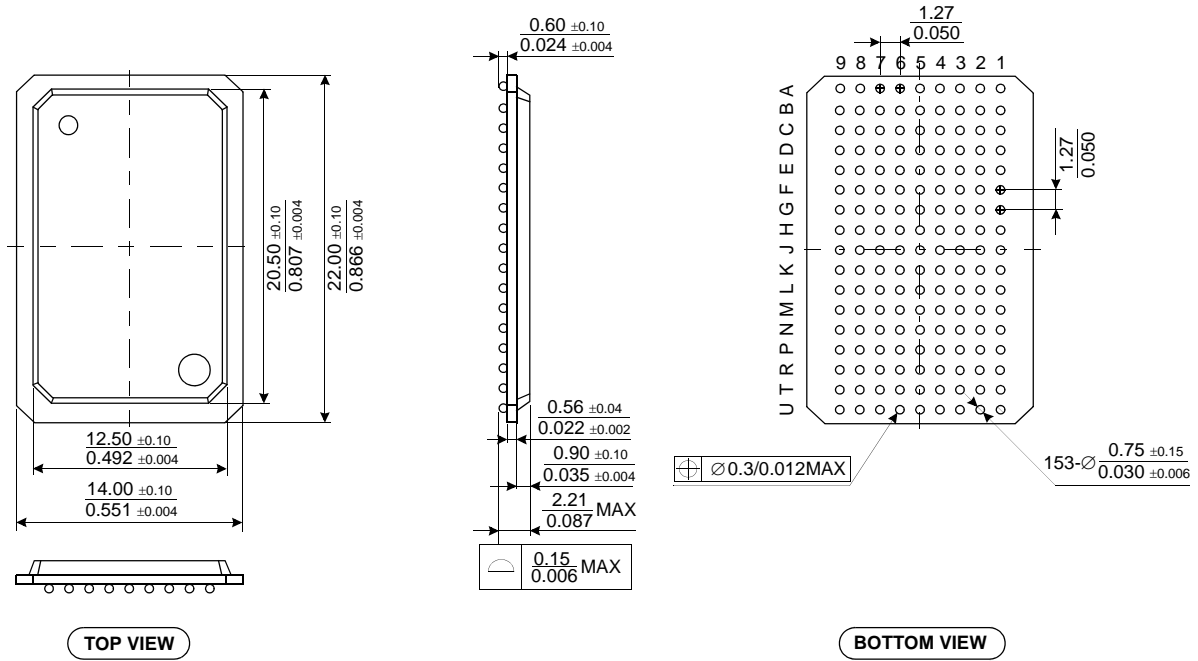
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



153 BGA PACKAGE DIMENSIONS



- NOTE :**
1. All Dimensions are in Millimeters.
 2. Solder Ball to PCS Offset : 0.10 MAX.
 3. PCB to Cavity Offset : 0.10 MAX.

153 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient(at still air)	Theta_JA	TBD	°C/W	
Junction to Case	Theta_JC	TBD	°C/W	
Junction to Board	Theta_JB	TBD	°C/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times \text{Theta_JA}$.