SED1765

CMOS HIGH DUTY LCD SEGMENT DRIVER

■ DESCRIPTION

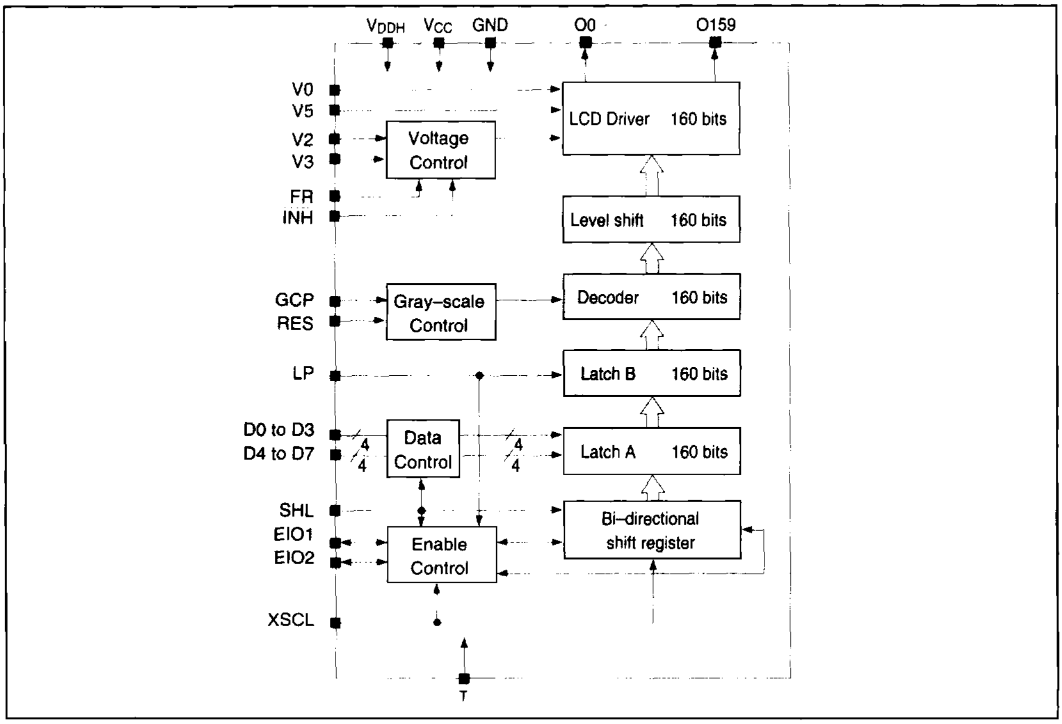
The SED1765 is a segment (column) driver for high-capacity dot matrix liquid crystal panels. It incorporates 160 high-voltage segment (column) drivers, and is designed for use in conjunction with the SED1703F common (row) driver device.

The SED1765 uses a PWM (Pulse Width Modulation) technique to provide 16, 8, or 4-level gray-scale displays without ghosting. The LCD drivers have been designed for low on output resistance making the SED1765 suitable for MIM LCD panels, and yielding gray-scale displays with few contrast disparities.

■ FEATURES

- 16, 8 or 4-level PWM gray-scale LCD driver
- Supports gray-scale gamma correction
- Two parallel 4-bit inputs
- 160 LCD drive outputs
- Maximum clock speed of 12 MHz allows a 640x480 pixel display with daisy-chain enable.
  Speeds up to 16 MHz are possible using external enable generation
- Wide 14 to 40 V range of LCD drive voltages
- Display blanking function
- Output shift direction is pin-selectable
- Automatic enable signal propagation allows cascade connection and decreases power consumption
- Adjustable LCD drive voltage offset relative to ground and supply
- Logic circuitry uses single 5.0V ±10% power supply
- CMOS Si-gate process
- Packages:
  Al pad chip: SED1765D0A
  Au bump pad chip: SED1765D0B
- Also available in tab

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

● 1.1 Gray-Scale Control Circuit

This circuit divides the gray-scale generation clock input on pin GCP, passes it to the decoder block. The divider circuit is reset on the falling edge of the RE3 or LP inputs or when the $\overline{\text{INH}}$ input is LOW.

● 1.2 Data Control Circuit

This circuit reorders the gray-scale data input on the D0 to D3 and D4 to D7 pins, into the order specified by the SHL input, and puts them on the internal data bus. It holds all data bus lines LOW if the device is disabled by the control signal from the enable controller.

● 1.3 Enable Controller

This circuit causes the data bus and the internal clock to be held LOW, and puts the device into power save mode, if the enable signal is inactive.

In systems with more than one segment driver, the enable inputs and outputs are cascaded, and the enable input at the head of the chain connected to ground. The enable controller counts the number of input data bits, and sets the enable output LOW to allow the next device in the chain to start loading data. This configuration eliminates the need for the controlling device to generate enable control signals.

The EIO output is reset HIGH by the LP input.

1.4 Shift Register

Segment data shift register. The latch A control signal is shifted by the shift clock. The direction of data shift is selected by the SHL pin as shown in the figure below.

SHL	O (SEG Output)							EIO	
	159	158	157	......	2	1	0	1	2
L	A0	B0	A1	......	B78	A79	B79	Output	Input
H	B79	A79	B78	......	A1	B0	A0	Input	Output

1.5 Latch A

The gray-scale data present on the internal data bus is latched successively by the latch control signal from the shift register.

1.6 Latch B

The data in latch A is latched in on the falling edge of LP.

1.7 Decoder

This circuit is locked to the signal from the gray-scale controller, and generates a pulse width corresponding to the gray-scale data value.

1.8 Level Shifter

The level shifter converts the logic-level signal from latch B to the voltage levels required by the LCD drivers.

1.9 LCD Drivers and Voltage Control Circuit

The LCD drivers drive individual columns of the display matrix with the voltage determined by the inhibit signal $\overline{\text{INH}}$, the frame signal FR, and the latched display data. This is shown in the table below.

$\overline{\text{INH}}$	Data	FR	SEG Output Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	H	V2
		L	V3

PIN DESCRIPTION

Pin Name	Function
O0 to O159	Segment drive outputs
D0 to D3, D4 to D7	4-bit gray-scale data inputs. D0 and D4 are the LSBs of each 4-bit nibble.
XSCL	Segment data shift clock input. Data is shifted into the driver on the falling edge of XSCL.
LP	Segment data latch strobe. Data is latched on the falling edge of LP.
EIO1, EIO2	Daisy chain enable input/outputs configured by SHL
GCP	Gray-scale reference clock input.
RES	PWM waveform reset input. The PWM waveform is reset to the OFF level by the falling edge of this input.
SHL	Shift direction select input. This signal configures EIO1, EIO2 and selects the shift register shift direction. An is input on D0 to D3 and Bn on D4 to D7.
FR	LCD AC-drive waveform input.
$\overline{\text{INH}}$	Display blanking input. When LOW, all outputs go to "off" levels.
V_{CC}, GND	Logic power supply inputs.
T	Test input. Tie low

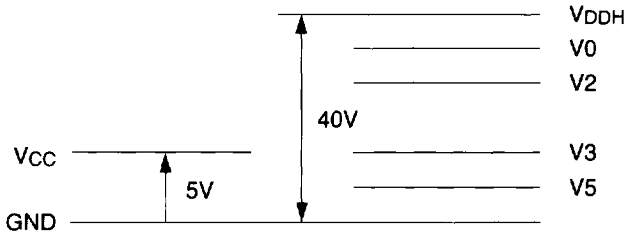
ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	-0.3 to +45.0	V
Supply voltage (3)	V0, V2, V3, V5	-0.3 to V_{DDH}+0.3	V
Input voltage	V_I	-0.3 to V_{CC}+0.3	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature 1	T_{stg}	-65 to +150	°C

Notes: 1. All voltages are with respect to ground.

2. Drive voltages should always be such that $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq$ ground.



3. The device may be permanently damaged if the LCD power supplies are applied while the 5V logic supply is floating. Pay particular attention to the power-on and power-off sequence.

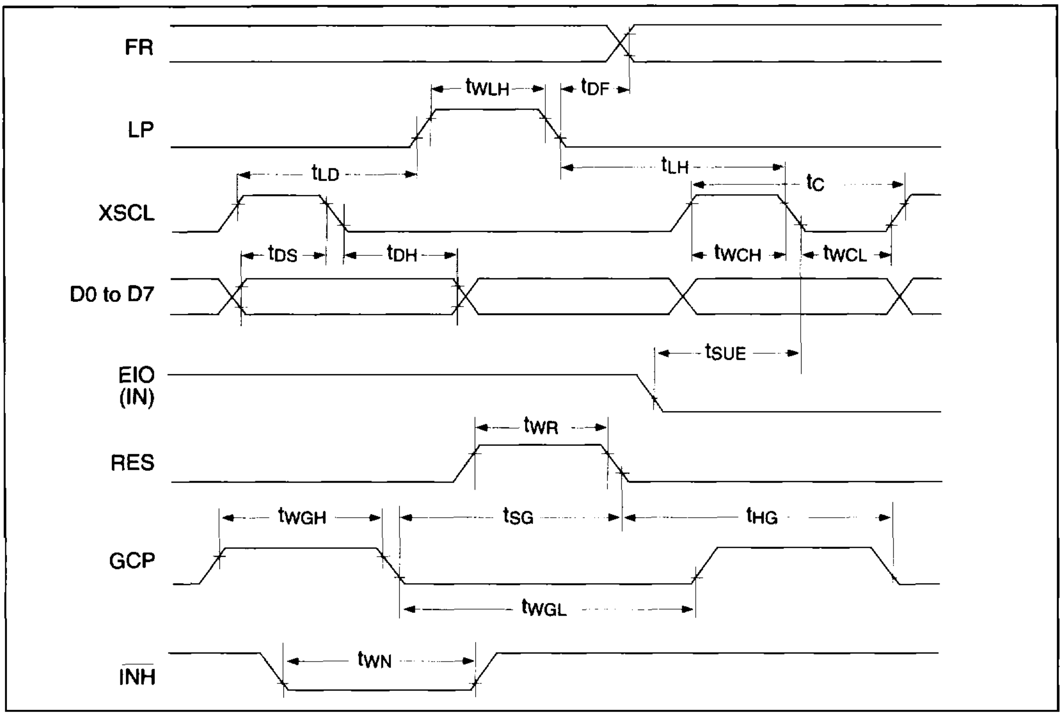
- **DC Characteristics**

T_a=-20 to 75°C, V5=0V, V_{CC}=5.0V±10% unless otherwise noted

Parameter	Symbol	Condition	Applicable Signal	Rating			Unit
				Min	Typ	Max	
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Supply voltage (2)	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Input voltage	V0	V0≥V2≥V3≥V5 Recommended	V0	V_{DDH}-2.5	—	V_{DDH}	V
Input voltage (1)	V2		V2	7/9xV_{DDH}	—	V_{DDH}	V
Input voltage (2)	V3, V5		V3, V5	GND	—	2.9xV_{DDH}	V
HIGH-level input voltage	V_{IH}		All input pins.	0.8xV_{CC}	—	0.2xV_{CC}	V
LOW-level input voltage	V_{IL}			GND	—	0.2xV_{CC}	V
HIGH-level output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO1, EIO2	V_{CC}-0.4	—	V_{CC}	V
LOW-level output voltage	V_{OL}	I_{OH}=0.4 mA		GND	—	0.4	V
Input leakage current	I_{LI}	GND≤V_I≤V_{CC}	All pins except EIO	—	—	2.0	µA
I/O leakage current	$I_{LI/O}$	GND≤V_I≤V_{CC}	EIO1, EIO2	—	—	5.0	µA
Quiescent current	I_{GND}	V_{DOH}=14.0 to 40.0 V V_{IH}=V_{CC}, V_{IL}=GND	GND	—	—	25	µA
Segment output ON resistance See note 1.	R_O	V_{OH}=0.5V, V_{DDH}=10.0V	O0 to O159	—	2.0	6.5	kΩ
		V_{DDH}=20.0V		—	1.5	3.5	
		V_{DDH}=30.0V		—	1.3	3.0	
Operating current (1)	f_{CC}	V_{CC}=5.0V, V_{IH}=V_{CC}, V_{IL}=GND, f_{xaCL}=10.6MHz, f_{LP}=33.8kHz, I_{f16}=0.54 MHz, FR=70 Hz, D0 to D7=F0F0..., alternating	V_{CC}	—	2.5	5.0	mA
Operating current (2)	I_{DDH}	V_{CC}=5.0V, V5=0V, V3=4V, V2=26V, V0=V_{DDH}=30V, other conditions same as I_{CC}	V_{DDH}	—	0.5	1.2	mA
Input capacitance See note 2.	C_I	T_a=25°C, Freq.=1 MHz	All pins except E1O	—	—	8.0	pF
I/O capacitance See note 2.	C_{LO}	T_a=25°C, Freq.=1 MHz	EIO1, EIO2	—	—	15.0	pF

1. Within the specified ranges of V0, V2, V3 and V4
2. Applies to chip part only.

- **AC Characteristics**
- **Input Timing**



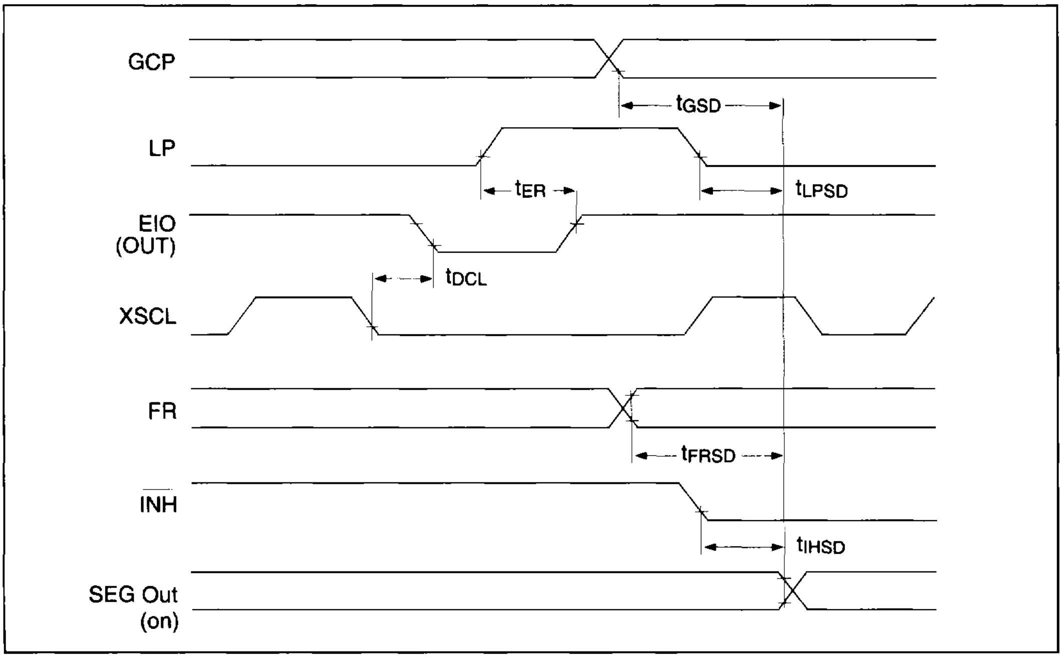
Note: For timing for LP pulse input, omit one XSCL clock cycle.

Ta=-20 to 75°C, VCC=5.0V±10%

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
XSCL-period	tC		71	—	—	ns
XSCL High pulse width	tWCH		30	—	—	ns
XSCL Low pulse width	tWCL		30	—	—	ns
EIO setup time	tSUE		30	—	—	ns
Data setup time	tDS		30	—	—	ns
Data hold time	tDH		20	—	—	ns
XSCL→LP rising edge	tLD		10	—	—	ns
LP→XSCL rising edge	tLH		100	—	—	ns
LP pulse width	tWLH	See note.	80	—	—	ns
RES pulse width	tWR		100	—	—	ns
INH low pulse width	tWN		100	—	—	ns
GCP high pulse width	tWGH		80	—	—	ns
GCP low pulse width	tWGL		80	—	—	ns
FR delay time	tDF		-300	—	+300	ns
GCP setup time	tSG		100	—	—	ns
GCP hold time	tHG		100	—	—	ns

Note: tWLP indicates the time XSLC is LOW as well as the time that LP is HIGH.

Output Timing

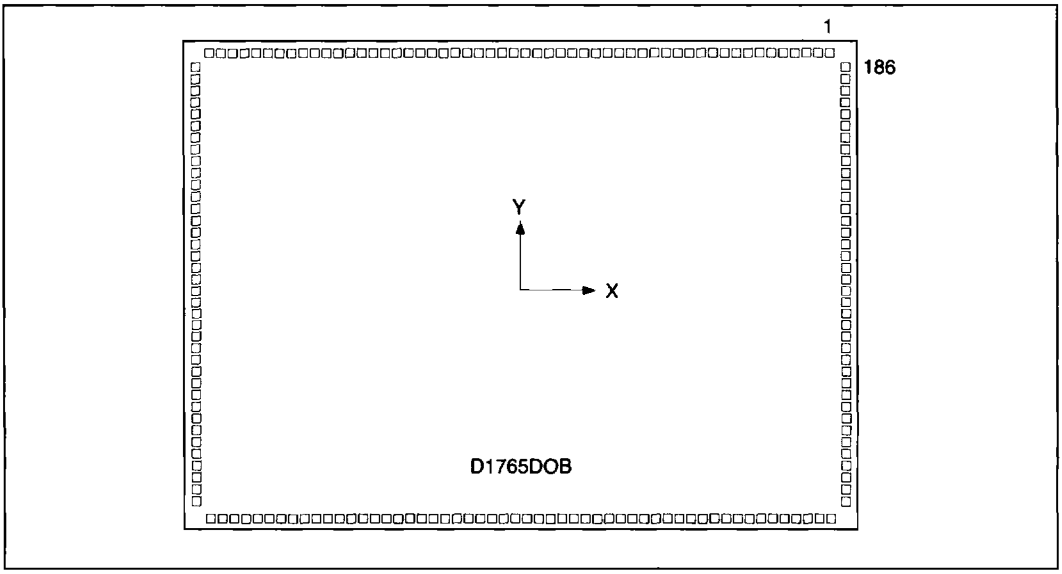


T_a=-20 to 75°C, V_{DDH}=14.0V to 40.0V

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
EIO output reset time	t_{ER}	C_L=15 pF	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	40	ns
LP→SEG (On) output delay time	t_{LPSD}	C_L=100 pF	—	—	2.0	µs
SEG→LP (On) output delay time	t_{FRSD}		—	—	2.0	µs
$\overline{INH}$→SEG (On) output delay time	t_{IHSD}		—	—	2.0	µs
GCP→SEG (On) output delay time	t_{GSD}		—	—	2.0	µs

■ MECHANICAL SPECIFICATIONS

● Pad Layout



Chip size: 8.80 x 5.62

Pad pitch: 0.134 mm min.

* Al pad (SED1765DOA)

Chip thickness: 0.400 ± 0.025 mm

Pad size, type A: 100 x 100 µm (All pads except 36, 37, 38, 39, 40)

Pad size, type B: 160 x 100 µm (Pads 36, 37, 38, 39, 40)

* Au bump pad (SED1765DOB)

Chip thickness: 0.525 ± 0.025 mm

Pad size, type A: 102 x 100 ± 20 µm (All pads except 36, 37, 38, 39, 40)

Pad size, type B: 186 x 100 ± 20 µm (Pads 36, 37, 38, 39, 40)

Note: Sizes are specified as x-dimension x y-dimension. X is parallel to the scribe-line.

- **Pad Coordinates**

Pad		X	Y
Number	Name		
1	O146	3950	2643
2	O147	3814	2643
3	O148	3678	2643
4	O149	3542	2643
5	O150	3406	2643
6	O151	3270	2643
7	O152	3134	2643
8	O153	2998	2643
9	O154	2862	2643
10	O155	2726	2643
11	O156	2590	2643
12	O157	2454	2643
13	O158	2318	2643
14	O159	2182	2643
15	EIO2	1998	2643
16	EIO1	1858	2643
17	GND	1718	2643
18	D0	1578	2643
19	D1	1438	2643
20	D2	1298	2643
21	D3	1158	2643
22	D4	1018	2643
23	D5	878	2643
24	D6	738	2643
25	D7	598	2643
26	NC	458	2643
27	SHL	318	2643
28	XSCL	178	2643
29	TEST	38	2643
30	$\overline{\text{INH}}$	-102	2643
31	LP	-242	2643
32	RES	-382	2643
33	GCP	-522	2643
34	VCC	-662	2643
35	FR	-802	2643
36	V0	-1032	2643
37	V5	-1262	2643
38	V3	-1492	2643
39	V2	-1722	2643
40	VDDH	-1952	2643
41	O0	-2182	2643
42	O1	-2318	2643
43	O2	-2454	2643
44	O3	-2590	2643
45	O4	-2726	2643
46	O5	-2862	2643
47	O6	-2998	2643
48	O7	-3134	2643
49	O8	-3270	2643
50	O9	-3406	2643
51	O10	-3542	2643
52	O11	-3678	2643
53	O12	-3814	2643
54	O13	-3950	2643
55	O14	-4230	2379
56	O15	-4230	2243
57	O16	-4230	2107
58	O17	-4230	1971
59	O18	-4230	1835
60	O19	-4230	1699
61	O20	-4230	1563
62	O21	-4230	1427
63	O22	-4230	1291
64	O23	-4230	1155
65	O24	-4230	1019
66	O25	-4230	883
67	O26	-4230	747
68	O27	-4230	611
69	O28	-4230	475
70	O29	-4230	339
71	O30	-4230	203
72	O31	-4230	67
73	O32	-4230	-69
74	O33	-4230	-205
75	O34	-4230	-341
76	O35	-4230	-477
77	O36	-4230	-613
78	O37	-4230	-749
79	O38	-4230	-885
80	O39	-4230	-1021
81	O40	-4230	-1157
82	O41	-4230	-1293
83	O42	-4230	-1429
84	O43	-4230	-1565
85	O44	-4230	-1701
86	O45	-4230	-1837
87	O46	-4230	-1973
88	O47	-4230	-2109
89	O48	-4230	-2245
90	O49	-4230	-2381
91	O50	-3954	-2643
92	O51	-3820	-2643
93	O52	-3686	-2643
94	O53	-3552	-2643
95	O54	-3418	-2643
96	O55	-3284	-2643
97	O56	-3150	-2643
98	O57	-3016	-2643
99	O58	-2882	-2643
100	O59	-2748	-2643

- **Pad Coordinates (cont.)**

Pad		X	Y
Number	Name		
101	O60	-2614	-2643
102	O61	-2480	-2643
103	O62	-2346	-2643
104	O63	-2212	-2643
105	O64	-2078	-2643
106	O65	-1944	-2643
107	O66	-1810	-2643
108	O67	-1676	-2643
109	O68	-1542	-2643
110	O69	-1408	-2643
111	O70	-1274	-2643
112	O71	-1140	-2643
113	O72	-1006	-2643
114	O73	-872	-2643
115	O74	-738	-2643
116	O75	-604	-2643
117	O76	-470	-2643
118	O77	-336	-2643
119	O78	-202	-2643
120	O79	-68	-2643
121	O80	68	-2643
122	O81	202	-2643
123	O82	336	-2643
124	O83	470	-2643
125	O84	604	-2643
126	O85	738	-2643
127	O86	872	-2643
128	O87	1006	-2643
129	O88	1140	-2643
130	O89	1274	-2643
131	O90	1408	-2643
132	O91	1542	-2643
133	O92	1676	-2643
134	O93	1810	-2643
135	O94	1944	-2643
136	O95	2078	-2643
137	O96	2212	-2643
138	O97	2346	-2643
139	O98	2480	-2643
140	O99	2614	-2643
141	O100	2748	-2643
142	O101	2882	-2643
143	O102	3016	-2643
144	O103	3150	-2643
145	O104	3284	-2643
146	O105	3418	-2643
147	O108	3552	-2643
148	O107	3686	-2643
149	O108	3820	-2643
150	O109	3954	-2643

Pad		X	Y
Number	Name		
151	O110	4230	-2381
152	O111	4230	-2245
153	O112	4230	-2109
154	O113	4230	-1973
155	O114	4230	-1837
156	O115	4230	-1701
157	O116	4230	-1565
158	O117	4230	-1429
159	O118	4230	-1293
160	O119	4230	-1157
161	O120	4230	-1021
162	O121	4230	-885
163	O122	4230	-749
164	O123	4230	-613
165	O124	4230	-477
166	O125	4230	-341
167	O126	4230	-205
168	O127	4230	-69
169	O128	4230	67
170	O129	4230	203
171	O130	4230	339
172	O131	4230	475
173	O132	4230	611
174	O133	4230	747
175	O134	4230	883
176	O135	4230	1019
177	O136	4230	1155
178	O137	4230	1291
179	O138	4230	1427
180	O139	4230	1563
181	O140	4230	1699
182	O141	4230	1835
183	O142	4230	1971
184	O143	4230	2107
185	O144	4230	2243
186	O145	4230	2379

■ TYPICAL APPLICATION CIRCUIT