

T6A00/01

TFT-LCD DATA DRIVER

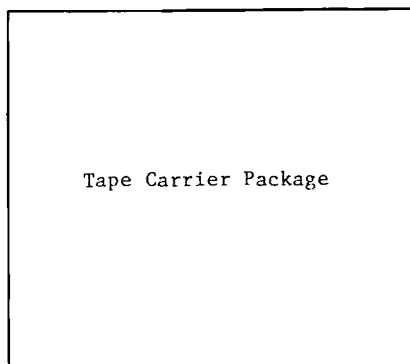
T6A00/T6A01 is a Data Driver LSI for driving TFT-LCD Panel, which achieves low power consumption by using C-MOS technology.

T6A00/T6A01 has 240 pins as TFT-LCD panel driving pins.

T6A00/T6A01 enables to correspond to a large TFT-LCD Panel that two or more T6A00/T6A01 can be cascaded.

T6A01 is the mirror type reversed T6A00.

- . TFT-LCD Data Driver LSI.
- . TFT-LCD Driving pins: 240 outputs (R,G,B each of 80 outputs)
- . Two or more T6A00/T6A01 can be cascaded.
- . It enables to correspond to various driving types by high voltage output.
- . T6A00 has T6A01 of the mirror type in order to facilitate LCD wiring.
- . It enable to correspond to various color filter arrangement by switching video signals.
- . It achieves low power consumption by auto standby function.
- . The package is a tape carrier package.
- . TFT-LCD gate driver (T6A02/T6A03) can be used with T6A00/T6A01.



Unit : mm

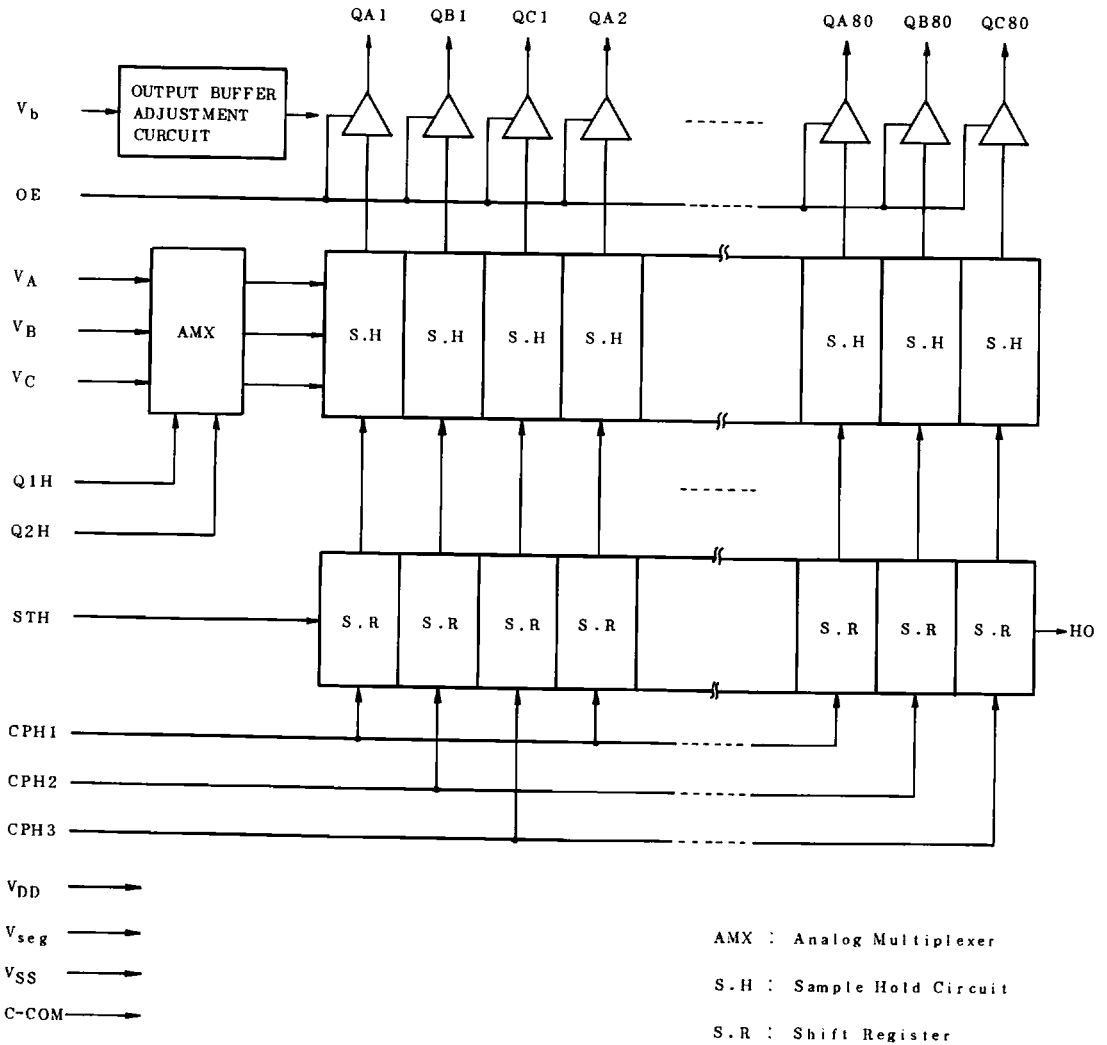
T6A00 T6A01	LEAD PITCH	
	IN, I/O	OUT
(TA)	1.50	0.17

* Refer to Packaging Outline Dimension.

- . Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

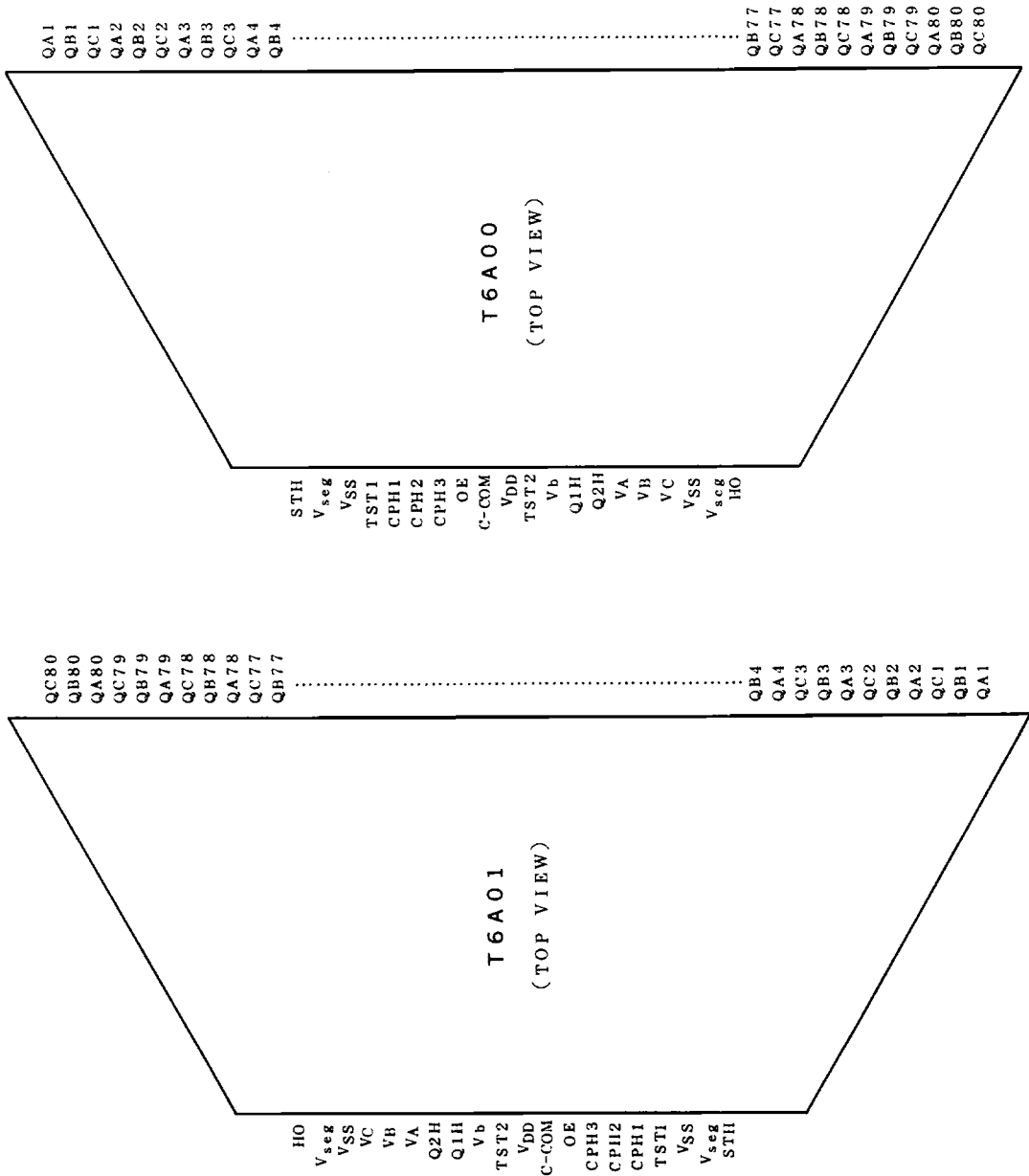
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BLOCK DIAGRAM



PIN FUNCTION

PIN CONFIGURATION



PIN DESCRIPTION

PIN NAME	I/O	FUNCTION																												
CPH1	I	Shift Clock 1 This pin is a shift clock that shifts a signal of sampling data. Sampling data is output to QA1~80.																												
CPH2	I	Shift Clock 2 This pin is a shift clock that shifts a signal of sampling data. Sampling data is output to QB1~80.																												
CPH3	I	Shift Clock 3 This pin is a shift clock that shifts a signal of sampling data. Sampling data is output to QC1~80.																												
STH	I	Sampling start pin It inputs data into LSI synchronously to the rise of CPH1. The data begin sampling in order by next CPH.																												
OE	I	Output Enable pin This pin controls an output data of output pins. OE="H" level : turns to output mode. OE="L" level : turns to High-Impedance.																												
Q1H/Q2H	I	<p>Video Signal Select pins These pins operate as shown. The result of the operation defines whether a TFT-LCD driving pin outputs a video signal data.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Q1H</th> <th>Q2H</th> <th>Input</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td rowspan="3">0</td> <td rowspan="3">0</td> <td>VA</td> <td>QC1~80</td> </tr> <tr> <td>VB</td> <td>QB1~80</td> </tr> <tr> <td>VC</td> <td>QA1~80</td> </tr> <tr> <td rowspan="3">0</td> <td rowspan="3">1</td> <td>VA</td> <td>QA1~80</td> </tr> <tr> <td>VB</td> <td>QC1~80</td> </tr> <tr> <td>VC</td> <td>QB1~80</td> </tr> <tr> <td rowspan="3">1</td> <td rowspan="3">Don't care</td> <td>VA</td> <td>QB1~80</td> </tr> <tr> <td>VB</td> <td>QA1~80</td> </tr> <tr> <td>VC</td> <td>QC1~80</td> </tr> </tbody> </table>	Q1H	Q2H	Input	Output	0	0	VA	QC1~80	VB	QB1~80	VC	QA1~80	0	1	VA	QA1~80	VB	QC1~80	VC	QB1~80	1	Don't care	VA	QB1~80	VB	QA1~80	VC	QC1~80
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		VB	QA1~80																											
		VC	QC1~80																											

PIN NAME	I/O	FUNCTION
Vb	I	TFT-LCD driving voltage adjustable pin The ability of output buffer can be changed by a voltage added to this pin.
VA VB VC	I	Video Signal Input pins These pins input video signal that output to TFT-LCD driving pins.
HO	O	TFT-LCD Expanding pin It sends a signal of start sampling to next LSI. TFT-LCD driving output can be expanded by this pin.
QA1~80 QB1~80 QC1~80	O	TFT-LCD driving pins These pins hold one of video signals (VA, VB, VC) and output the level.
C-COM	I	Standard Voltage of sample Hold It is a standard voltage of sample hold circuit.
Vseg		Power Supply Voltage It is a high voltage system power supply pin of LSI.
VDD		Power Supply Voltage It is a logical system power supply pin of LSI.
VSS		Power Supply Voltage It is a common GND of LSI.
TST1 TST2		Test pins These pins must be open.

FUNCTIONAL DESCRIPTION

. SAMPLING OF VIDEO SIGNALS

It inputs STH="H" level into LSI synchronously to the rise of CPH1 and starts sampling video signals which output to QA1 synchronously to the rise of the next. And after it is sampling in the same way.

Synchronously to the rise of CPH2 → Output to QB1, CPH3 → QC1, CPH1 → QA2,
CPH2 → QB2, CPH3 → QC2 ...

Video signal select pins (Q1H,Q2H) decide the relationship between Video signal input pins and TFT-LCD driving pins as follows: When data of QC80 finishes sampling, it turns standby state.

Q1H	Q2H	Video signal input pins	TFT-LCD driving pins
0	0	VA	QC1~80
		VB	QB1~80
		VC	QA1~80
0	1	VA	QA1~80
		VB	QC1~80
		VC	QB1~80
1	Don't care	VA	QB1~80
		VB	QA1~80
		VC	QC1~80

. TFT-LCD DRIVING OUTPUT

When OE is "H" level, TFT-LCD driving pins (QA1~QC80) output Sample hold data. During sampling, OE must keep "L" level. After it finishes sampling, OE is able to keep "H" level.

OE="H" level : turns to output mode.

OE="L" level : turns to high impedance.

. SAMPLE HOLD STANDARD VOLTAGE INPUT (C-COM)

It is fabricated sample hold into LSI by condenser. As a result, this must supply standard voltage.

Force the center of video signals and in DC level.

. TFT-LCD DRIVING OUTPUT EXPANDING METHOD

TFT-LCD expanding pin (HO) outputs "H" level of one clock synchronously to the fall of CPH1. (cf. Fig.1)

It enable to expand TFT-LCD driving output pins so as to drive a large display.

It must connect HO pin of first LSI and STH pin of second LSI.

TIMING CHART

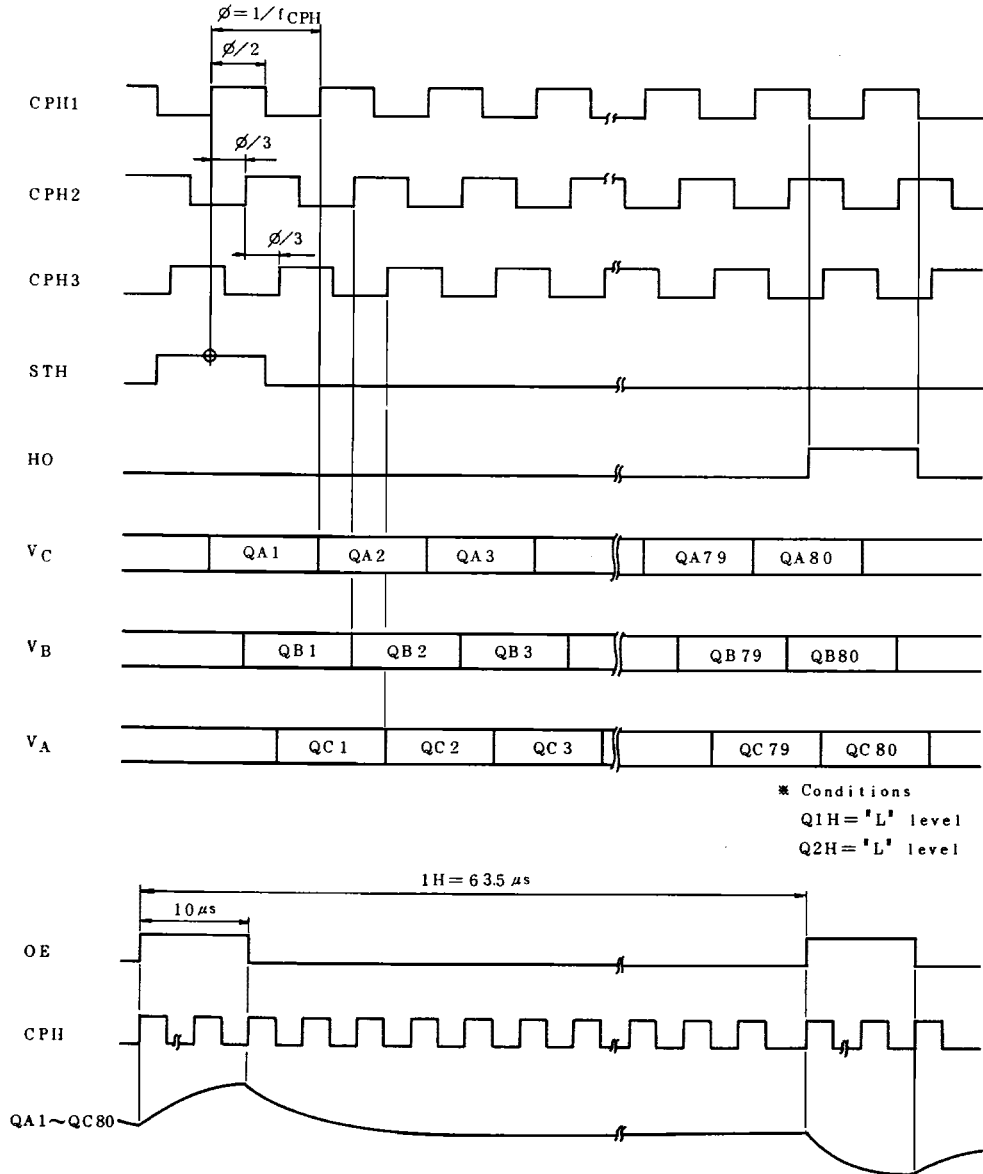


Fig. 1

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MAXIMUM RATINGS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT	NOTE
Supply Voltage 1	V _{DD}		-0.3~7.0	V	
Supply Voltage 2	V _{seg}		-0.3~18	V	
Input Voltage	V _{IN}		-0.3~V _{DD} +0.3	V	*1
Storage Temperature	T _{stg}		-55~125	°C	
Analog Input Voltage	V _{video}		V _{SS} -0.3~V _{seg} +0.3	V	

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT	NOTE
Operating Voltage 1	V _{DD}		4.5~5.5	V	
Operating Voltage 2	V _{seg}		V _{DD} -15	V	
Operating Temperature	T _{OP}		-20~75	°C	
Operating Frequency	f _{CPH}		0.5~6.0	MHz	
Output Load Capacitance	C _L		0~200	pF	
Operating Voltage Swing	V _{video}		V _{SS} +1.0~V _{seg} -2.0	V	TFT-LCD driving pin
Video Input Capacitance	C _{video}		80(max)	pF	

*1 Applicable pins are all analog input signals except for VA, VB, VC, Vb and C-COM.

DC CHARACTERISTICS

(Unless otherwise specified, $V_{DD}=4.5\sim 5.5V$, $V_{seg}=13V$, $V_{SS}=0V$, $T_a=-20\sim 75^\circ C$)

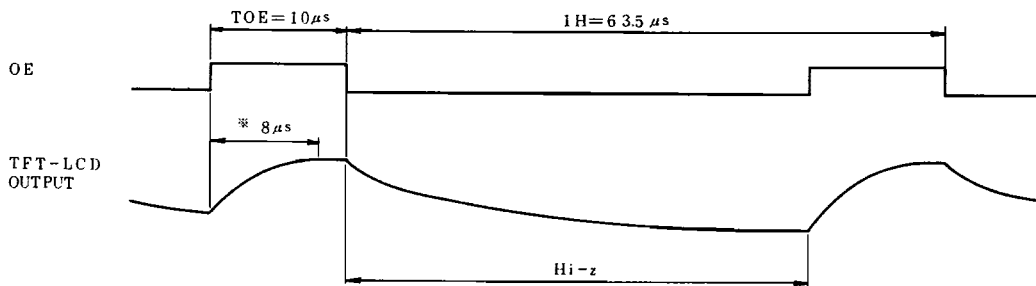
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Input "L" Level	V_{IL}		0	-	$0.2 \times V_{DD}$	V	*1
Input "H" Level	V_{IH}		$0.8 \times V_{DD}$	-	V_{DD}	V	*1
Output "L" Level	V_{OL}	$I_{OL}=40\mu A$	V_{SS}	-	$V_{SS}+0.3$	V	HO
Output "H" Level	V_{OH}	$I_{OH}=-40\mu A$	$V_{DD}-0.3$	-	V_{DD}	V	HO
Output Offset Voltage	V_{off}		-50.0	-	50.0	mV	QA1~QC80
Output Current	I_{OL}	*2	-	0.2	-	mA	QA1~QC80
Output Leak Current	I_{Dleak}		-1.0	-	1.0	μA	OE="L"
Input Current	I_{in}		-1.0	-	1.0	μA	*1
Current Consumption 1	I_{DD}	*3	-	-	4.0	mA	
Current Consumption 2	I_{seg}	*3	-	-	7.0	mA	

*1 Applicable pins are CPH1~3, STH, OE, Q1H and Q2H.

*2 $V_b=10V$, $V_{video}=11V$

*3 $f_{CPH}=3MHz$, $t_H=63.5\mu s$, $t_{OE}=10\mu s$, $V_{video}=1\sim 11V$ (width)
Load Capacitance=100pF (All output pins)

TIMING DIAGRAMS (Output)



* $8\mu s$ is adjusted by V_b (Input Level).

Fig. 2

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AC CHARACTERISTICS

(Unless otherwise specified, $V_{DD}=4.5\sim 5.5V$, $V_{seg}=13V$, $V_{SS}=0V$, $T_a=-20\sim 75^\circ C$,
Rising and falling time=6ns (all input signals))

TIMING CHART

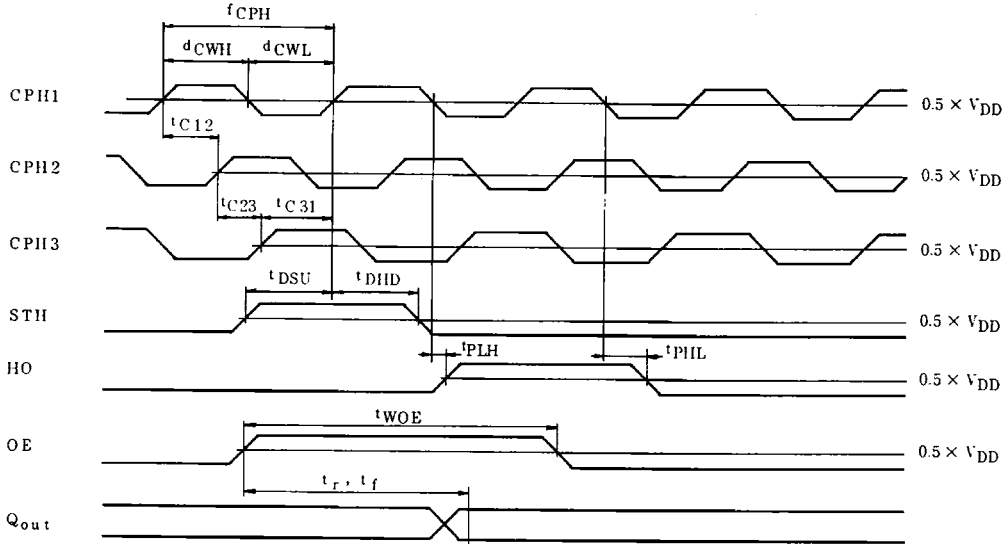


Fig. 3

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Operating Frequency	$f_{CPH}(1/t_{CPH})$		0.5	6	MHz
CPH Pulse Duty	d_{CWH}, d_{CWL}		40	60	%
Clock Delay	$t_{C12}, t_{C23}, t_{C31}$		40	$t_{CPH}/2$	ns
Data Set Up Time	t_{DSU}		20	-	ns
Data Hold Time	t_{DHD}		60	-	ns
HO "H" Transfer Delay Time	t_{PLH}		-	60	ns
HO "L" Transfer Delay Time	t_{PHL}		-	60	ns
OE Pulse Width	t_{WOE}		5	20	μs
LCD Driving Outputs Rising and Falling Time	t_r, t_f	QA1~QC80	Adjustment by V _b level		