MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX469

1200 and 2400 bps MSK Modem

Document #2048-0081.005 November 1995

Preliminary Information

Features

- Selectable Data Rates: *1200 and 2400 bps*
- Full-Duplex MSK
- RX and TX Bandpass Filters
- Clock Recovery and Carrier Detect Cabability
- Pin Selected Xtal/Clock Inputs:
  1.008MHz or 4.032MHz
- Radio and General Applications
  - Data-Over-Radio
  - PMR/Cellular Signaling
  - Portable Data Terminals
  - Personal/Cordless Telephone

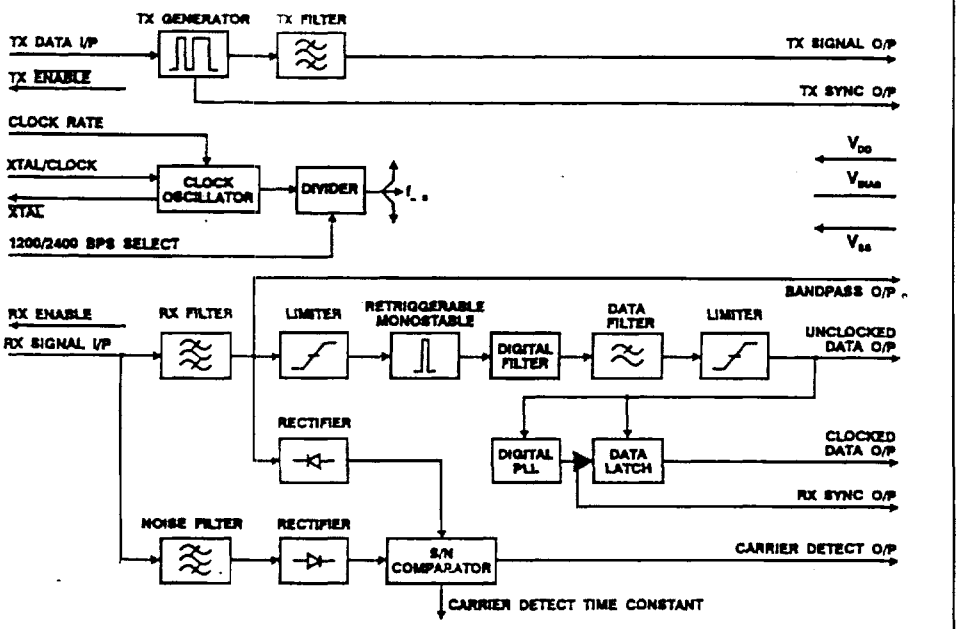
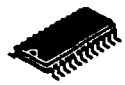


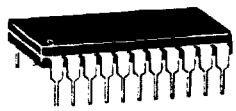
Figure 1 - Functional Block Diagram

AVAILABLE PACKAGES



MX469DW
24-pin SOIC

MX469LH
24-pin PLCC



MX469P/J
22-pin PDIP/CDIP

Brief Description

The MX469 is a full-duplex pin-selectable 1200 or 2400 bps Minimum Shift Key (MSK) Modem for FM radio links. The mark and space frequencies are 1200/1800 and 1200/2400Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point.

Use of a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides data-rate, transmit frequencies and RX/TX synchronization. The transmitter and receiver operate entirely independently including individual section powersave functions.

The MX469 includes on-chip circuitry for Carrier Detect and RX Clock Recovery, both of which are made available at output pins.

RX, TX and Carrier Detect paths each contain a bandpass filter to make sure you get the best quality signal in the Modem and TX modulation circuitry.

The MX469 demonstrates a high sensitivity and good bit-error-rate even under adverse signal conditions.

The carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high-noise environments.

This low-power device requires few external components and is available in SOIC (small outline), CDIP, PDIP and PLCC packages.

Pin Function Table

Pin Number MX469 DW	J/P	LH	Function
1	1	1	**Xtal/Clock:** The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. The selection of this frequency will affect the operational Data Rate of this device. Refer to 1200/2400 BPS Selection information on the next page. Operation of any MX•COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, it is recommended that a current limiting device (resistor or fast-reaction fuse) be installed on the power supply (V_{DD}).
2	2	2	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter.
3	3	3	**TX Sync O/P:** A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the MSK signal (See Figure 4).
5	5	5	**TX Signal O/P:** When the transmitter is enabled, this pin outputs the (140-step pseudo sinewave) MSK signal (See Figure 4). With the transmitter disabled, this output is set to a high-impedance state.
7	6	7	**TX Data I/P:** Serial logic data to be transmitted is input to this pin.
8	7	8	**$\overline{\text{TX Enable}}$:** A logic '0' will enable the transmitter (See Figure 4). A logic '1' at this input will put the transmitter into powersave while forcing "TX Sync Out" to a logic '1' and "TX Signal Out" to a high-impedance state. This pin is internally pulled to V_{DD}.
9	8	9	**Bandpass O/P:** The output of the RX Bandpass Filter. This output impedance is typically 10kΩ and may require buffering prior to use.
10	9	10	**RX Enable :** The control of the RX function. The control of other outputs is given below.

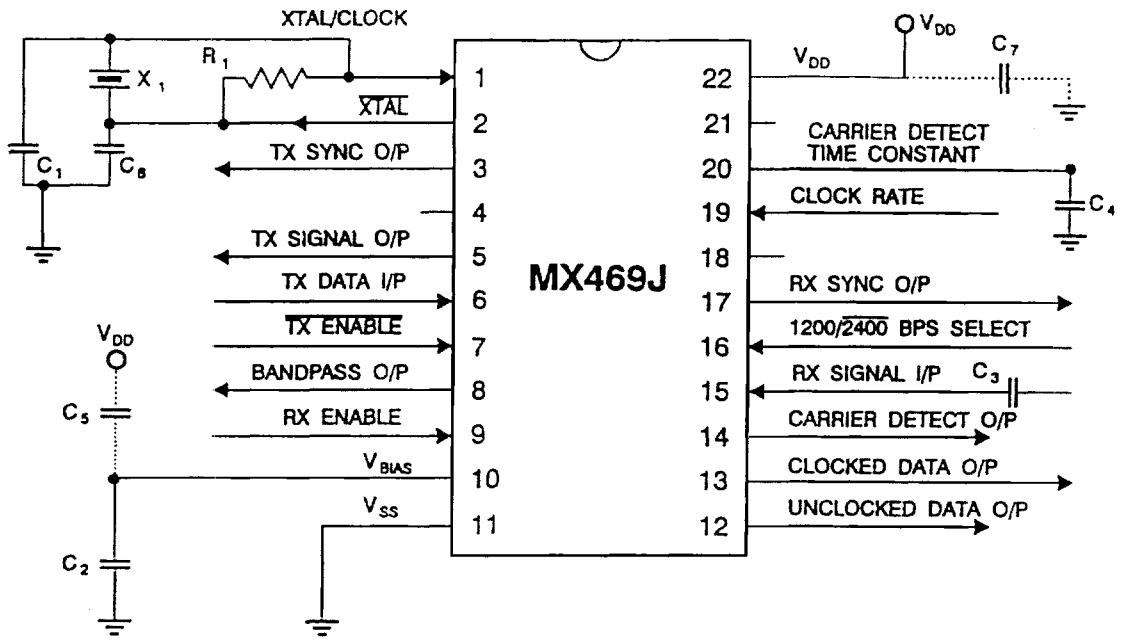
RX Enable	=	RX Function	Clock Data O/P	Carrier Detect	Rx Sync Out
"1"	=	Enabled	Enabled	Enabled	Enabled
"0"	=	Powersave	"0"	"0"	"1" or "0"

11	10	11	**V_{BIAS}:** The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} by a capacitor (C_2). See Figure 2 and RX Enable notes. This bias voltage is maintained under all powersave conditions.
12	11	12	**V_{SS}:** Negative supply rail (GND).

Pin Number			Function
MX469			
DW	J/P	LH	
13	12	13	**Unclocked Data O/P:** The recovered asynchronous serial data output from the receiver.
14	13	14	**Clocked Data O/P:** The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "RX Sync O/P", (See Figures 5 and 7).
15	14	15	**Carrier Detect O/P:** When an MSK signal is being received this output is a logic '1'.
16	15	16	**RX Signal I/P:** The MSK signal input for the receiver. This input should be coupled via a capacitor, C_3.
18	17	18	**RX Sync O/P:** A flywheel squarewave output. This clock will synchronize to incoming RX MSK data (See Figures 5 and 7).
19	16	19	**1200/$\overline{2400}$ BPS Select:** A logic '1' on this pin selects the 1200 bps option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one-and-a-half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 bps option. Tone frequencies are: one-half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pullup resistor. **Operational Data Rate Configurations** are illustrated in the table below.
20	18	20	Internally connected, leave open circuit.
21	19	21	**Clock Rate:** A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
23	20	22	**Carrier Detect Time Constant :** Part of the carrier detect integration function. The value of C_4 connected to this pin will affect the carrier detect response time and hence noise performance (See Figure 2, Note 3).
24	22	24	V_{DD}: Positive supply. A single 5-volt supply is required.
4,6, 17, 22	4, 21	4, 6, 17, 23	No internal connection, do not use.

Xtal/Clock Frequency	1.008MHz		4.032MHz	
Clock Rate pin	0	0	1	1
1200/2400 Select pin	1	0	1	0
Data Rate (bps)	**1200**	**2400**	**1200**	**2400**

Application Information



Component	Value	Tolerance
R_1	1.0MΩ	±10%
C_1	33pF	±5%
C_2	1.0µF	±20%
C_3	0.1µF	±20%
C_4	0.1µF	±10%
C_5	1.0µF	±25%
C_6	33pF	±5%
C_7	1.0µF	±20%
X_1	1.008MHz or 4.032MHz	See 'Clock-Rate' Pin

Notes

1. Decoupling circuits depend upon whether the input signal is referenced to V_{BIAS} or V_{SS}. Use C_5 when the input signal is referenced to V_{BIAS}. Use C_7 when the input signal is referenced to V_{SS}. It is not necessary to use both C_5 and C_7.
2. The value of C_4 determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. C_4 may be varied to trade-off response time for noise immunity.
3. C_6 reduces Xtal voltage overshoot. Refer to MX•COM Xtal Application Note (see Application section).

Figure 2 - External Components

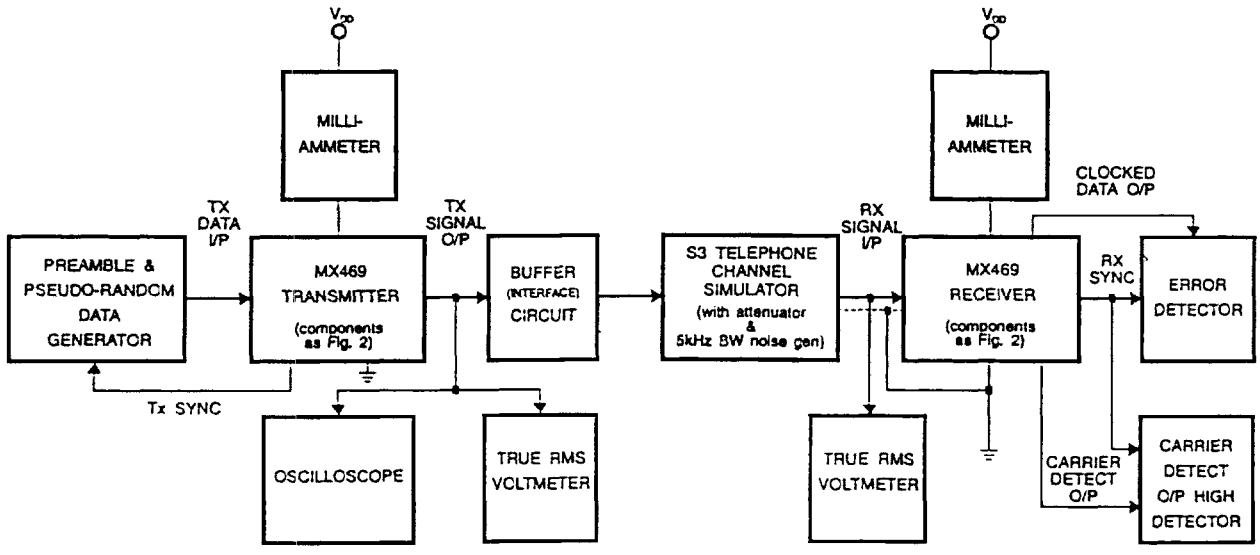


Figure 3 - Suggested MX469 Test Set-Up

Application Information:1200 bps Timing

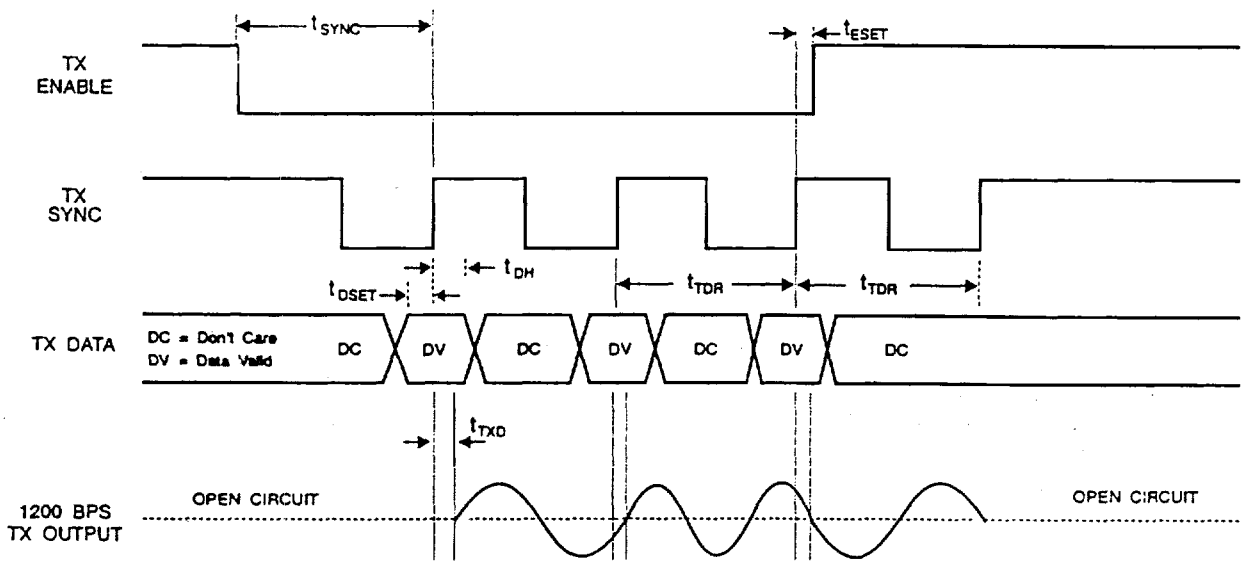


Figure 4 - Transmitter Timing: 1200 bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}		-	416	-	µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0	-	800	µs
Data Set-Up Time	t_{DSET}	1	2.0	-	-	µs
Data Hold Time	t_{DH}		2.0	-	-	µs
TX Delay to O/P Time	t_{TxD}		-	1.2	-	µs
TX Data Rate Period	t_{TDR}		-	833	-	µs
RX Data Rate Period	t_{RDR}		800	-	865	µs
Undetermined State			-	-	2.0	µs
Internal RX Delay	t_{ID}		-	1.5	-	ms

1200bps only

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.

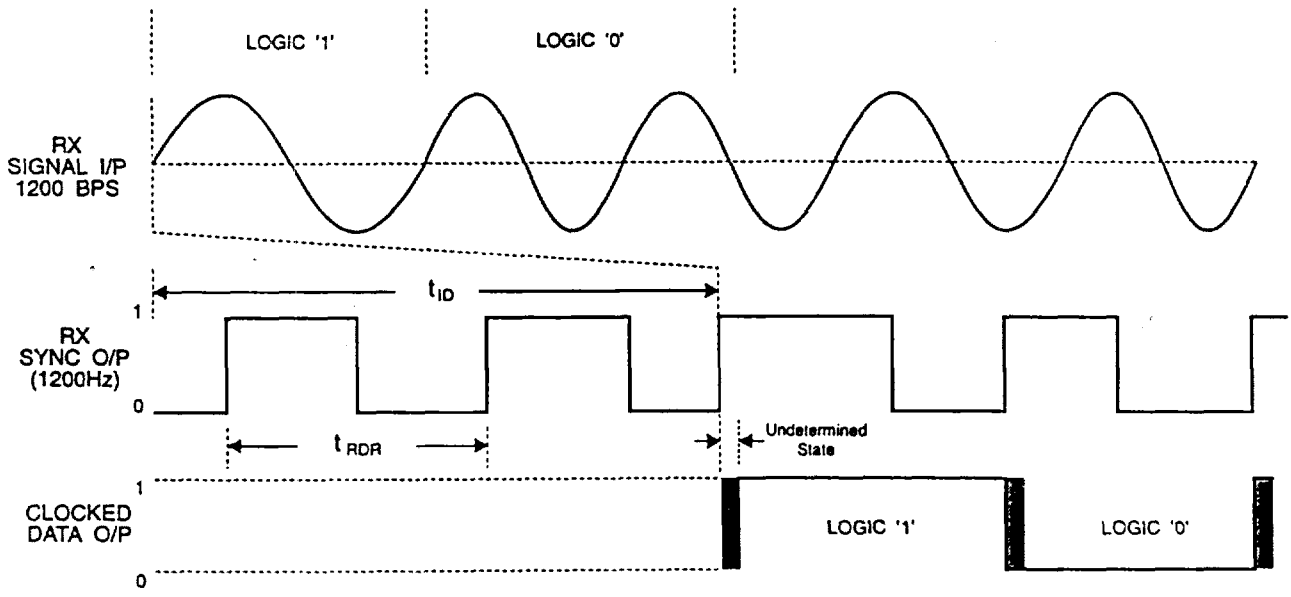


Figure 5 - RX Timing Diagram: 1200 bps

Application Information: 2400 bps Timing

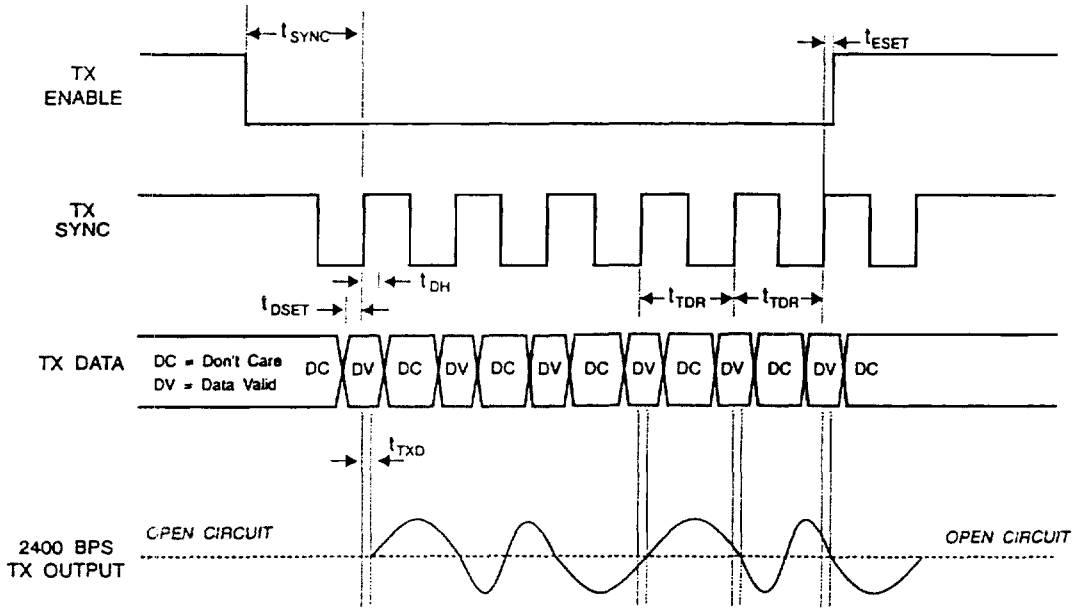


Figure 6 - Transmitter Timing: 2400 bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}		-	208	-	µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0	-	400	µs
Data Set-Up Time	t_{DSET}	1	2.0	-	-	µs
Data Hold Time	t_{DH}		2.0	-	-	µs
TX Delay to O/P Time	t_{TxD}		-	2	-	µs
TX Data Rate Period	t_{TDR}		-	416	-	µs
RX Data Rate Period	t_{RDR}		400	-	433	µs
Undetermined State			-	-	2.0	µs
Internal RX Delay	t_{ID}		-	1.5	-	ms

2400bps only

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.

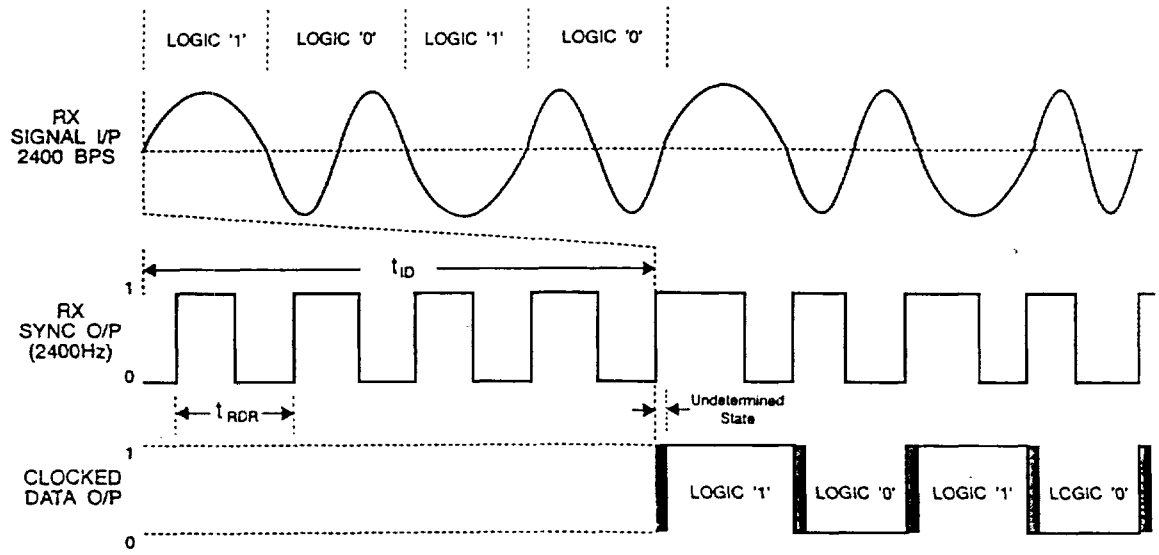


Figure 7 - RX Timing Diagram: 2400 bps

Application Information .....

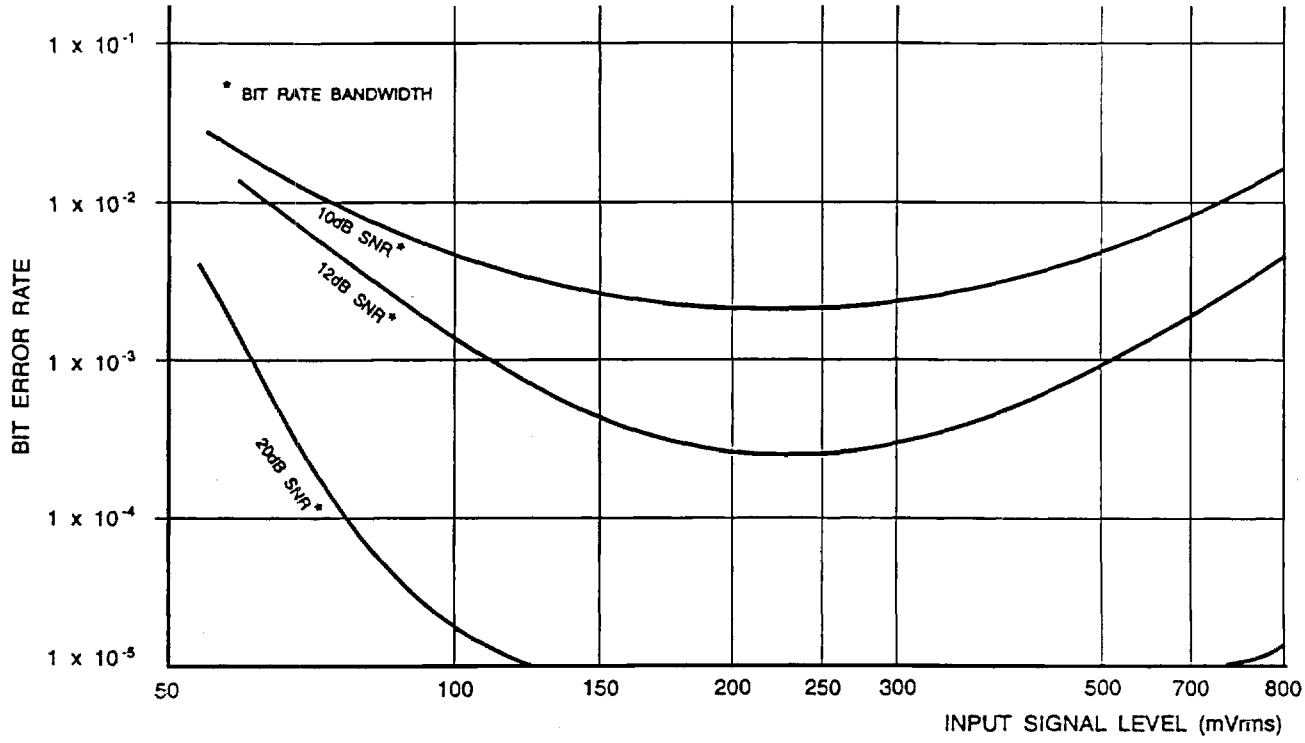


Figure 8 - Typical Variation of Bit Error Rate with Input Level

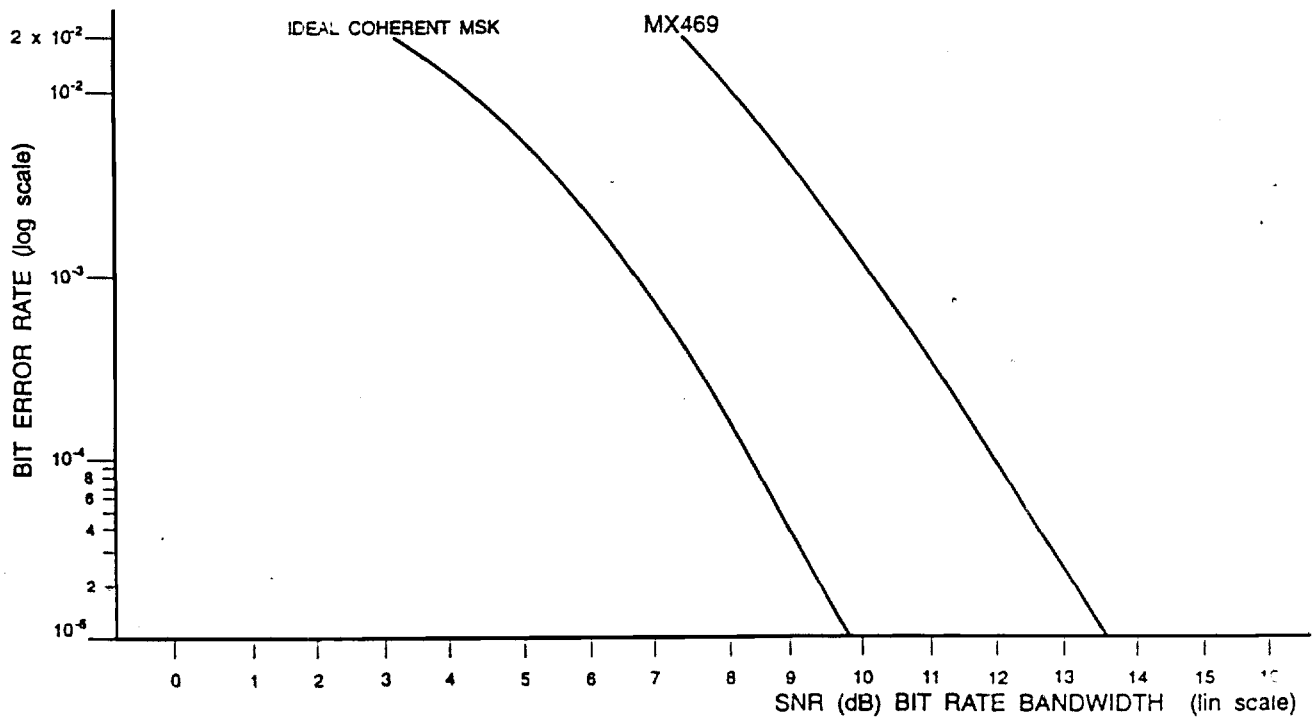


Figure 9 - RX Bit-Error-Rate vs Signal-to-Noise Ratio

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Audio Level 0dB ref = 300 mVrms

Xtal/Clock = 4.032 MHz

Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth
(1200 bps BRB = 1200 Hz
2400 bps BRB = 2400 Hz)

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current	RX Enabled, TX Disabled		-	3.6	-	mA
	RX and TX Enabled		-	4.5	-	mA
	RX and TX Disabled		-	650	-	µA
Logic '1' Level		1	4.0	-	-	V
Logic '0' Level		1	-	-	1.0	V
Digital Output Impedance			-	4.0	-	kΩ
Analog and Digital Input Impedance			100	-	-	kΩ
TX Output Impedance			-	10.0	-	kΩ
On-Chip Xtal Oscillator						
	R_{IN}		10.0	-	-	MΩ
	R_{OUT}		-	10.0	-	kΩ
Inverter d.c. Voltage Gain			-	10.0	-	V/V
Gain Bandwidth Product			-	10.0	-	MHz
Xtal Frequency		2	-	1.008 or 4.032	-	MHz
Dynamic Values						
Receiver						
Signal Input Dynamic Range	SNR = 50dB	3, 4	100	230	1000	mVrms
Bit Error Rate	SNR = 12dB	4	-	7.0	-	10^{-4}
	SNR = 20dB	4	-	1.0	-	10^{-8}
Receiver Synchronization	**SNR =12dB**	7				
Probability of Bit 8 Being Correct		-	99	-	%	
Probability of Bit 16 Being Correct			-	99.5	-	%
Carrier Detect		5				
Sensitivity		7, 8	-	-	150	mVrms
Probability of C.D. Being High						
After Bit 8	(1200 bps) SNR = 12dB	5, 9	-	98	-	%
After Bit 16	SNR = 12dB	5, 9	-	99.5	-	%
0dB Noise	No Signal	9	-	5	-	%
Transmitter Output						
TX Output Level			-	775	-	mVrms
Output Level Variation 1200/1800Hz or 1200/2400Hz			0	-	±1.0	dB
Output Distortion			-	3.0	5.0	%
3rd Harmonic Distortion			-	2.0	3.0	%
Logic '1' Carrier Frequency	1200 bps	6	-	1200	-	Hz
	2400 bps	6	-	1200	-	Hz
Logic '0' Carrier Frequency	1200 bps	6	-	1800	-	Hz
	2400 bps	6	-	2400	-	Hz
Isochronous Distortion						
1200Hz - 1800Hz/1200Hz - 2400Hz			-	25.0	40.0	µs
1800Hz - 1200Hz/2400Hz - 1200Hz			-	20.0	40.0	µs

Characteristics Notes (see previous page)

1. With reference to V_{DD} = 5.0 volts.
2. Xtal frequency (ref. Clock Rate pin), type and tolerance depends upon system requirements.
3. See Figure 5 (variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise in the Bit-Rate Bandwidth.
5. See Figure 2.
6. Dependent upon Xtal tolerance.
7. 10101010101 ...01 pattern.
8. Measured with a 150mVrms input signal (no noise).
9 Reference (0dB) level for C.D. probability measurements is 230mVrms.

Package Outlines

The MX469P plastic dual in-line package is shown in Figure 10, the 'J' (ceramic dual in-line) version in Figure 11, the 'LH' PLCC version in Figure 12 and the 'DW' SOIC (small outline) version in Figure 13.

Pin 1 identification marking is shown on the relevant diagrams. Pins on all package styles number counter-clockwise when viewed from the top (indent side).

Handling Precautions

The MX469 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

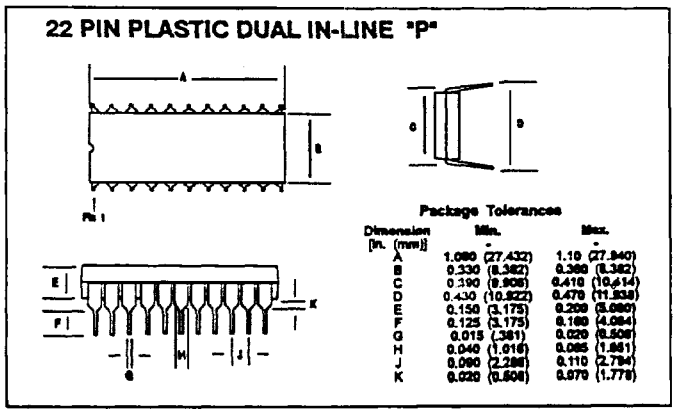


*Figure 10 - **MX469P** 22-pin Plastic DIP*

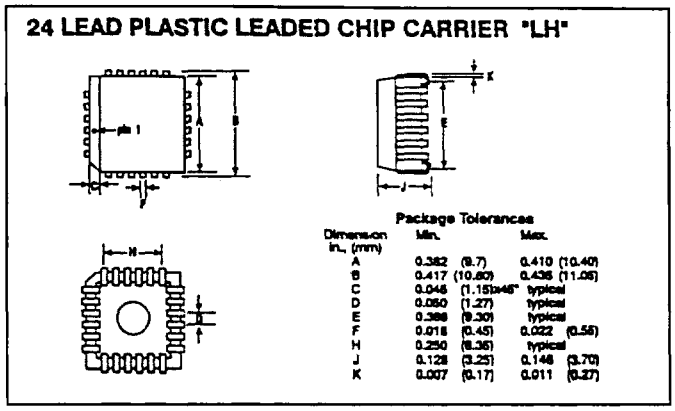


*Figure 12 - **MX469LH** PLCC-24 Package*

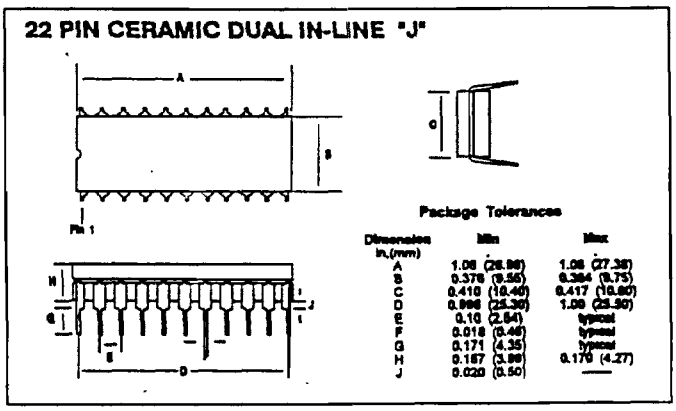


*Figure 11 - **MX469J** 22-pin Ceramic DIP*

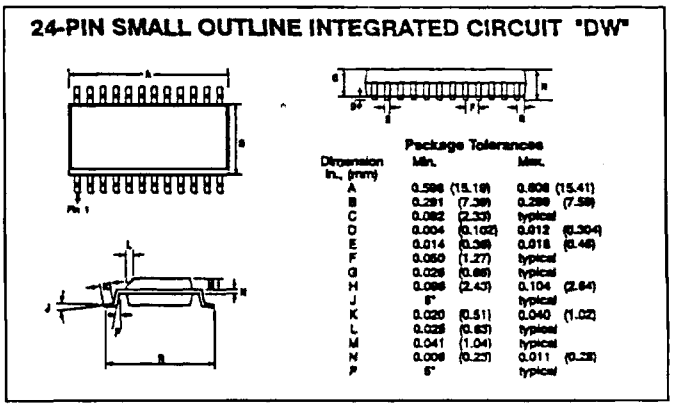


*Figure 13 - **MX469DW** 24-pin SOIC*