HIGH SPEED 1 MEG (128K x 8) CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — t_{ACC} = 25 ns
  - — t_{CE} = 25 ns
- **Immune to Latch-Up**
  - — Up to 200 mA
- **Available in Popular Packages**
  - — DIP, PLDCC, TSOP

GENERAL DESCRIPTION

The WS57C010F is a High Performance 128K x 8 UV Erasable EPROM. It is manufactured using an advanced CMOS process technology enabling it to operate at speeds as fast as 25 ns Address Access Time (t_{ACC}). It was designed using WSI's patented Alternate Metal Virtual Ground (AMG) cell. This innovative memory architecture results in a very high performance EPROM.

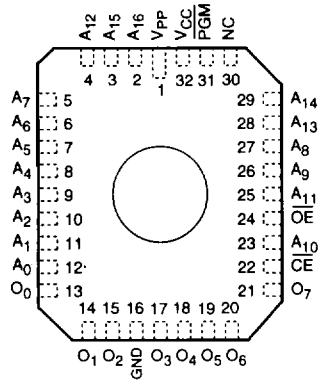
This product, with its high speed capability and high storage capacity is particularly appropriate for use with today's fast DSP processors and high-clock rate microprocessors. In most cases the CPU can operate without wait states. The WS57C010F is also designed for use in modem applications. It is an ideal memory for the newest Rockwell modem chip sets.

The WS57C010F is available in the 600 Mil DIP, the surface mount PLDCC and TSOP. Its standard JEDEC EPROM pinouts provide for an easy upgrade path for current users of the WS57C256F.

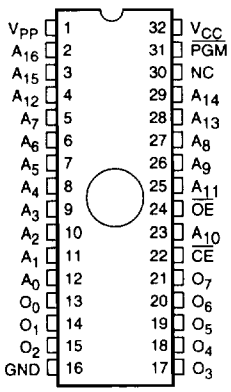
PIN CONFIGURATION

TOP VIEW

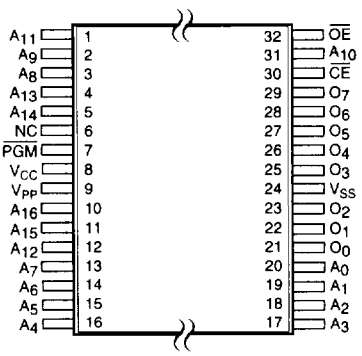
Chip Carrier



CERDIP



TSOP



PRODUCT SELECTION GUIDE

PARAMETER	57C010F-25	57C010F-35	57C010F-45	57C010F-55	57C010F-70
Address Access Time (Max)	25 ns	35 ns	45 ns	55 ns	70 ns
Chip Select Time (Max)	25 ns	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	12 ns	15 ns	20 ns	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 14V

V_{CC} Supply Voltage with Respect to Ground .....–0.6V to +7V

ESD Protection.....>2000V

***NOTICE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%

DC READ CHARACTERISTICS (V_{CC} = 5.0 V ± 0.5 V)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage			–0.3	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CCQ0}	V_{CC} CMOS Standby Quiescent Current	CE ≥ V_{CC} –0.3 V All Pins ≥ V_{CC} –0.3V or ≤ 0.3 V (All Inputs Fixed, No Switching)	Comm'l		100	µA
			Industrial		150	µA
I_{CCSB0}	V_{CC} CMOS Standby Current	CE ≥ V_{CC} –0.3V All Pins ≥ V_{CC} –0.3V or ≤ 0.3 V (Toggling) f ≤ 10 MHz	Comm'l		10	mA
			Industrial		15	mA
I_{CCSB1}	V_{CC} TTL Standby Current	CE ≥ V_{IH} All Pins = V_{IH} or V_{IL} (Toggling) f ≤ 10 MHz	Comm'l		20	mA
			Industrial		25	mA
I_{CC1}	V_{CC} Active Current	CE = V_{IL} f ≤ 10 MHz I_{OUT} = 0 mA (Open Outputs)	Comm'l		25	mA
			Industrial		30	mA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			10	µA
I_{LI}	Input Leakage Current	0 V < V_{IN} < 5.5 V		–10	10	µA
I_{LO}	Output Leakage Current	0 V < V_{OUT} < 5.5 V		–10	10	µA

NOTE: 1. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.

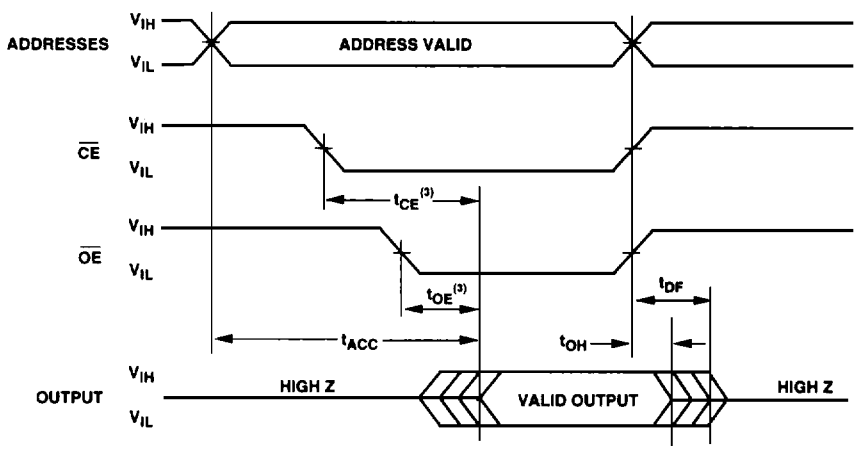
AC READ CHARACTERISTICS (V_{CC} = 5.0 V ± 0.5 V, V_{PP} = V_{CC})

SYMBOL	PARAMETER	TEST CONDITIONS	-25		-35		-45		-55		-70		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, C_L = C_{L1}		25		35		45		55		70	ns
t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}, C_L = C_{L1}		25		35		45		55		70	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}, C_L = C_{L1}		12		15		20		25		30	ns
t_{DF}	Output Disable to Output Float (Note 2)	C_L = C_{L2}		12		15		20		25		30	ns
t_{OH}	Output Hold		0		0		0		0		0		ns

NOTE: 2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.

3

AC READ TIMING DIAGRAM



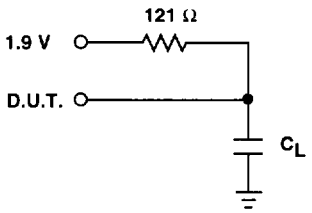
NOTE: 3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE[4] (T_A = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITIONS	TYP[4]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

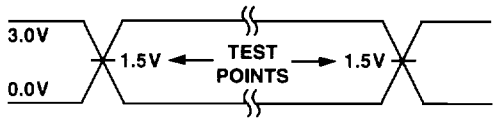
NOTE: 4. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



C_{L1} = 30 pF
C_{L2} = 5 pF

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 5. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 ± 0.25 V, V_{PP} = 12.75 ± 0.25 V. See Notes 6, 7 and 8)

SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		50	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 12 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

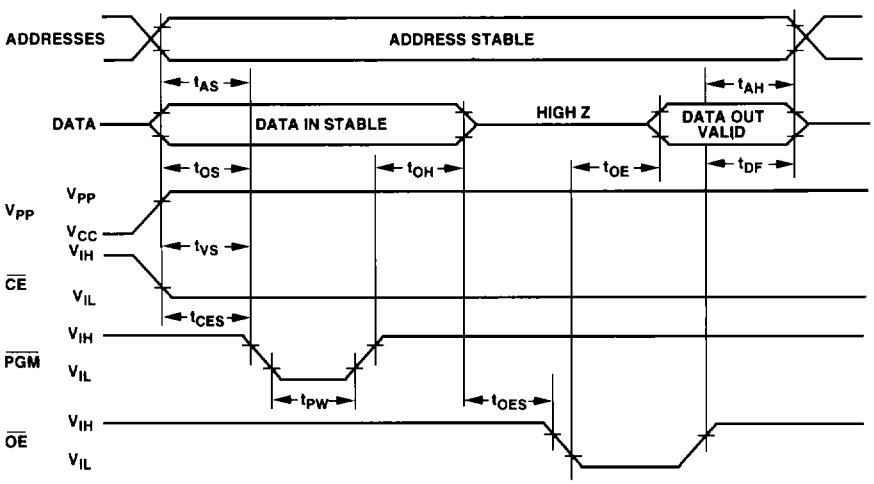
NOTES: 6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
8. During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		55	ns
t_{OE}	Data Valid From Output Enable			55	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	0.1		1	ms

3

PROGRAMMING WAVEFORM



DESIGN FEATURES

The WS57C010F features low power design technology that improves power consumption, input noise immunity, and speed. When none of the inputs switch for an extended period (typically 50 ns), the WS57C010F will automatically go into a standby mode, shutting down most of its internal circuitry. This reduces current consumption. The outputs will maintain the output states that were present before the device entered internal standby mode. When any input changes state, the internal circuits are again enabled and power consumption returns to normal.

These low power design features will operate independently of the status of the chip enable or output enable control signals.

ERASURE

To clear all memory locations of their programmed contents, expose the WS57C010F to an ultraviolet light source. Use a dosage of 30 Wseconds/cm^2 to completely erase the WS57C010F. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 40 to 45 minutes. The WS57C010F should be directly under and about one inch from the source. Remove all filters from the UV light source prior to erasing the EPROM.

Note that the WS57C010F will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, exposure to fluorescent light and sunlight (3000Å to 4000Å) will eventually erase the WS57C010F. Prevent exposure to these light sources to avoid problems with system reliability. To use the product in such an environment cover the package window with an opaque label or substance.

Plastic packaged versions may be programmed one time and cannot be erased.

MODE SELECTION

The modes of operation of the WS57C010F are listed below. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

MODE / PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[9]	X	X	X	5.0 V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0 V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0 V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}[10]	6.25 V	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}[10]	6.25 V	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}[10]	5.0 V	High Z
Signature	Manufacturer[11]	V_{IL}	V_{IL}	X	V_H[10]	V_{IL}	X	5.0 V	23 H
	Device[11]	V_{IL}	V_{IL}	X	V_H[10]	V_{IH}	X	5.0 V	F8 H

NOTES: 9. X can be V_{IL} or V_{IH}.
10. $V_H = V_{PP} = 12.75 \pm 0.25$ V.
11. $A_1 - A_8$, $A_{10} - A_{15} = V_{IL}$.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 6-1

The WS57C010F is programmed using Algorithm E shown on page 6-11.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C010F-25C	25	32 Pin CLLCC	C2	Comm'l	Standard
WS57C010F-25D	25	32 Pin CERDIP, 0.6"	D4	Comm'l	Standard
WS57C010F-25E	25	32 Pin TSOP	E1	Comm'l	Standard
WS57C010F-25J	25	32 Pin PLDCC	J4	Comm'l	Standard
WS57C010F-25L	25	32 Pin CLDCC	L3	Comm'l	Standard
WS57C010F-35C	35	32 Pin CLLCC	C2	Comm'l	Standard
WS57C010F-35CI	35	32 Pin CLLCC	C2	Industrial	Standard
WS57C010F-35D	35	32 Pin CERDIP, 0.6"	D4	Comm'l	Standard
WS57C010F-35DI	35	32 Pin CERDIP, 0.6"	D4	Industrial	Standard
WS57C010F-35E	35	32 Pin TSOP	E1	Comm'l	Standard
WS57C010F-35EI	35	32 Pin TSOP	E1	Industrial	Standard
WS57C010F-35J	35	32 Pin PLDCC	J4	Comm'l	Standard
WS57C010F-35JI	35	32 Pin PLDCC	J4	Industrial	Standard
WS57C010F-35L	35	32 Pin CLDCC	L3	Comm'l	Standard
WS57C010F-35LI	35	32 Pin CLDCC	L3	Industrial	Standard
WS57C010F-45C	45	32 Pin CLLCC	C2	Comm'l	Standard
WS57C010F-45CI	45	32 Pin CLLCC	C2	Industrial	Standard
WS57C010F-45D	45	32 Pin CERDIP, 0.6"	D4	Comm'l	Standard
WS57C010F-45DI	45	32 Pin CERDIP, 0.6"	D4	Industrial	Standard
WS57C010F-45E	45	32 Pin TSOP	E1	Comm'l	Standard
WS57C010F-45EI	45	32 Pin TSOP	E1	Industrial	Standard
WS57C010F-45J	45	32 Pin PLDCC	J4	Comm'l	Standard
WS57C010F-45JI	45	32 Pin PLDCC	J4	Industrial	Standard
WS57C010F-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C010F-45LI	45	32 Pin CLDCC	L3	Industrial	Standard
WS57C010F-55C	55	32 Pin CLLCC	C2	Comm'l	Standard
WS57C010F-55CI	55	32 Pin CLLCC	C2	Industrial	Standard
WS57C010F-55D	55	32 Pin CERDIP, 0.6"	D4	Comm'l	Standard
WS57C010F-55DI	55	32 Pin CERDIP, 0.6"	D4	Industrial	Standard
WS57C010F-55E	55	32 Pin TSOP	E1	Comm'l	Standard
WS57C010F-55EI	55	32 Pin TSOP	E1	Industrial	Standard
WS57C010F-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C010F-55JI	55	32 Pin PLDCC	J4	Industrial	Standard
WS57C010F-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C010F-55LI	55	32 Pin CLDCC	L3	Industrial	Standard
WS57C010F-70C	70	32 Pin CLLCC	C2	Comm'l	Standard
WS57C010F-70CI	70	32 Pin CLLCC	C2	Industrial	Standard
WS57C010F-70D	70	32 Pin CERDIP, 0.6"	D4	Comm'l	Standard
WS57C010F-70DI	70	32 Pin CERDIP, 0.6"	D4	Industrial	Standard
WS57C010F-70E	70	32 Pin TSOP	E1	Comm'l	Standard
WS57C010F-70EI	70	32 Pin TSOP	E1	Industrial	Standard
WS57C010F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard
WS57C010F-70JI	70	32 Pin PLDCC	J4	Industrial	Standard
WS57C010F-70L	70	32 Pin CLDCC	L3	Comm'l	Standard
WS57C010F-70LI	70	32 Pin CLDCC	L3	Industrial	Standard

NOTES: 12. The actual part marking will not include the initials "WS."
13. Products in J and E package are one time programmable.