

Dual Hex DMOS Output Driver with Serial Input Control

Description

The U6815BM is a fully protected driver interface designed in 0.8- μm BCDMOS technology. It is used to control up to 12 different loads by a microcontroller in automotive and industrial applications.

Each of the 6 high-side and 6 low-side drivers is capable to drive currents up to 600 mA. The drivers are freely configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors

can be combined. The IC design especially supports the applications of H-bridges to drive DC motors.

Protection is guaranteed in terms of short-circuit conditions, overtemperature, under- and overvoltage. Various diagnosis functions and a very low quiescent current in standby-mode open a wide range of applications. Automotive qualification referring to conducted interferences, EMC protection and 2 kV ESD protection gives added value and enhanced quality for the exacting requirements of automotive applications.

Features

- Six high-side and six low-side drivers
- Outputs freely configurable as switch, half bridge or H-bridge
- Capable to switch all kinds of loads such as DC motors, bulbs, resistors, capacitors and inductors
- 0.6 A continuous current per switch
- Low-side: $R_{DSon} < 1.5 \Omega$ vs. total temperature range
- High-side: $R_{DSon} < 2.0 \Omega$ vs. total temperature range
- Very low quiescent current $I_s < 20 \mu\text{A}$ in standby mode
- Outputs short-circuit protected
- Overtemperature prewarning and protection
- Under- and overvoltage protection
- Various diagnosis functions such as shorted output, open load, overtemperature and power supply fail
- Serial data interface
- Daisy chaining possible
- Loss of ground protection
- SO28 power package

Ordering Information

Extended Type Number	Package	Remarks
U6815BM-FL	SO28 Power package	

Block Diagram

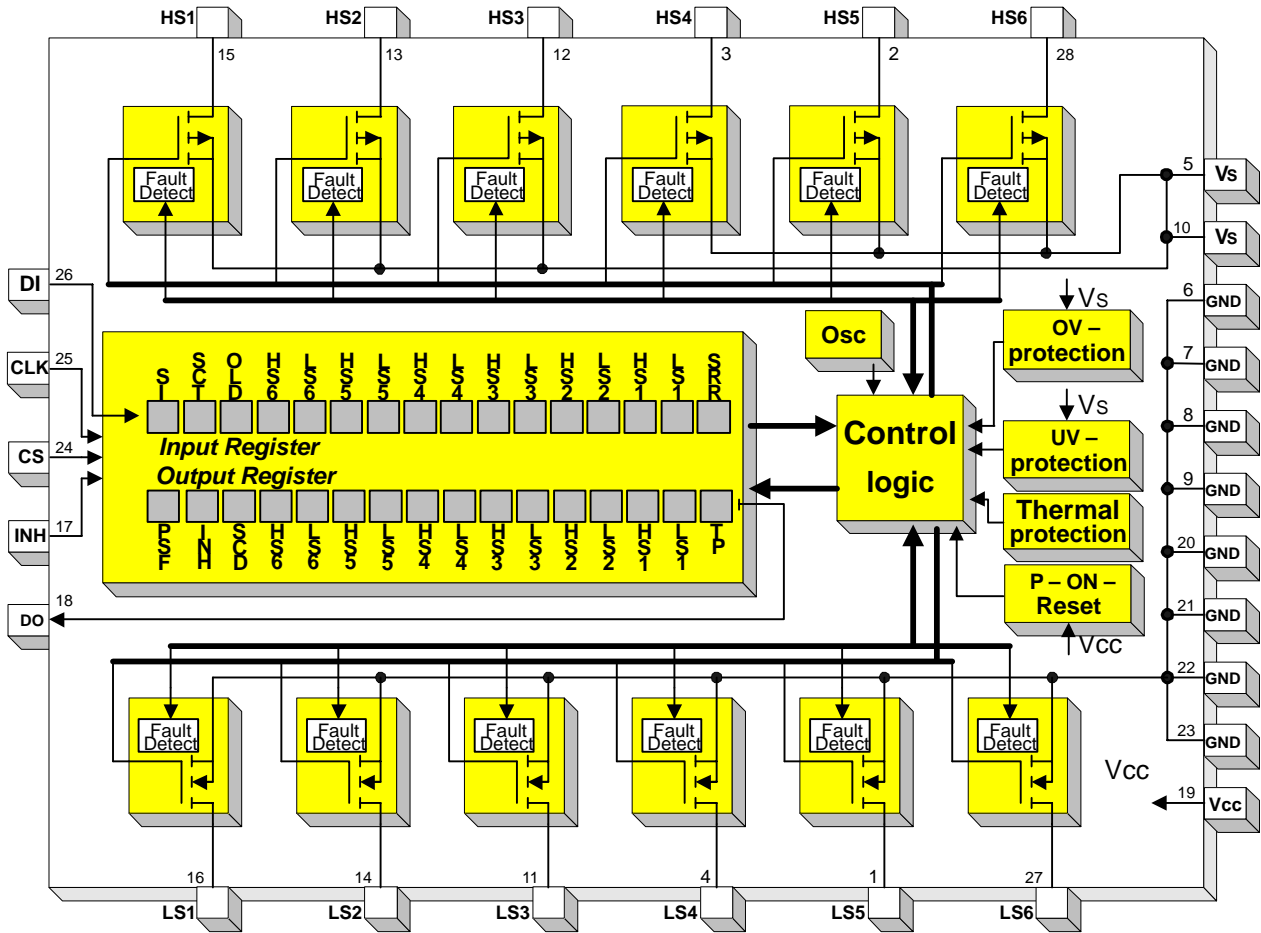


Figure 1. Block diagram

Pin Description

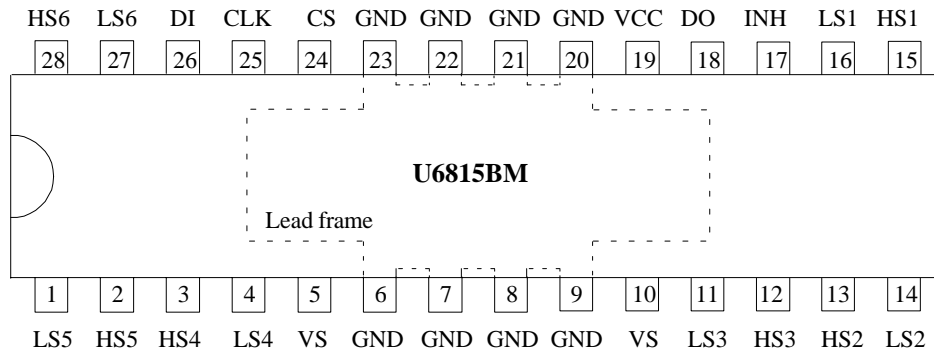


Figure 2. Pinning

Pin	Symbol	Function
1	LS5	Low-side driver output 5; Power-MOS open drain with internal reverse diode: overvoltage protection by active zenering; short-circuit protection; diagnosis for short and open load
2	HS5	High-side driver output 5; Power-MOS open drain with internal reverse diode: overvoltage protection by active zenering; short-circuit protection; diagnosis for short and open load
3	HS4	High-side driver output 4; see Pin 2
4	LS4	Low-side driver output 4; see Pin 1
5	VS	Power supply output stages HS4, HS5, HS6, internal supply; external connection to Pin 10 necessary
6, 7, 8, 9	GND	Ground; reference potential; internal connection to Pin 20 – 23; cooling tab
10	VS	Power supply output stages HS1, HS2 and HS3
11	LS3	Low-side driver output 3; see Pin 1
12	HS3	High-side driver output 3; see Pin 2
13	HS2	High-side driver output 2; see Pin 2
14	LS2	Low-side driver output 2; see Pin 1
15	HS1	High-side driver output 1; see Pin 2
16	LS1	Low-side driver output 1; see Pin 1
17	INH	Inhibit input; 5-V logic input with internal pull down; low = standby, high = normal operating
18	DO	Serial data output; 5-V CMOS logic level tristate output for output (status) register data; sends 16-bit status information to the μC (LSB is transferred first). Output will remain tristated unless device is selected by CS = low, therefore, several ICs can operate on one data output line only.
19	VCC	Logic supply voltage (5 V)
20, 21, 22, 23	GND	Ground; see Pin 6 – 9
24	CS	Chip select input; 5-V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled
25	CLK	Serial clock input; 5-V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register ($f_{\text{max}} = 2 \text{ MHz}$)
26	DI	Serial data input; 5-V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first
27	LS6	Low-side driver output 6; see Pin 1
28	HS6	High-side driver output 6; see Pin 2

Functional Description

Serial Interface

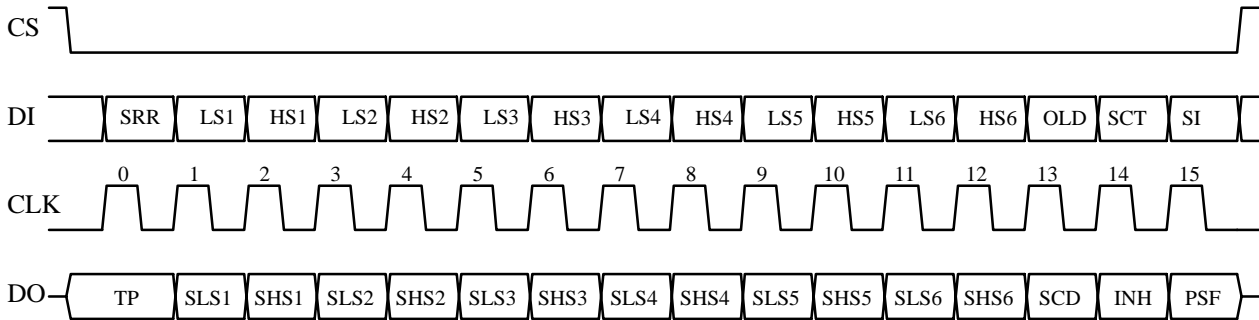


Figure 3. Data transfer

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal.

When CS is high, Pin DO is in tristate condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, SCD and overtemperature shutdown in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	LS4	See LS1
8	HS4	See HS1
9	LS5	See LS1
10	HS5	See HS1
11	LS6	See LS1
12	HS6	See HS1
13	OLD	Open load detection (low = on)
14	SCT	Programmable time delay for short circuit and overvoltage shutdown (short circuit shutdown delay high / low = 100 ms / 12.5 ms, overvoltage shutdown delay high / low = 15 ms / 3.5 ms)
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered)

After power-on reset, the input register has the following status:

Bit 15 (SI)	Bit 14 (SCT)	Bit 13 (OLD)	Bit 12 (HS6)	Bit 11 (LS6)	Bit 10 (HS5)	Bit 9 (LS5)	Bit 8 (HS4)	Bit 7 (LS4)	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L

Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning (overtemperature shut down see remark below)
1	Status LS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
2	Status HS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	Status LS4	Description see LS1
8	Status HS4	Description see HS1
9	Status LS5	Description see LS1
10	Status HS5	Description see HS1
11	Status LS6	Description see LS1
12	Status HS6	Description see HS1
13	SCD	Short circuit detected: set high, when at least one output is switched off by a short circuit condition
14	INH	Inhibit: this bit is controlled by software (bit SI in input register) and hardware inhibit (Pin 17). High = standby, low = normal operation
15	PSF	Power supply fail: over- or undervoltage at Pin VS detected

Remark: Bit 0 to 15 = high: overtemperature shutdown

Power Supply Fail

In case of over- / undervoltage at pin VS, an internal timer is started. When the overvoltage delay time (t_{dOV}) programmed by the SCT Bit, or the undervoltage delay time (t_{dUV}) is reached, the power supply fail bit (PSF) in the output register is set and all outputs are disabled. When normal voltage is present again, the outputs are enabled immediately. The PSF bit remains high until it is reset by the SRR bit in the Input Register.

Open-Load Detection

If the open-load detection bit (OLD) is set to low, a pull up current for each high side switch and a pull down current for each low side switch is turned on (open-load detection current I_{HS1-6} , I_{LS1-6}). If $V_{VS} - V_{HS1-6}$ or V_{LS1-6} is lower than the open-load detection threshold (open-load condition) the corresponding bit of the output in the output register is set to high. Switching on an output stage with OLD bit set to low disables the open-load function for this output.

Overtemperature Protection

If the junction temperature exceeds the thermal prewarning threshold, $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When temperature falls below the thermal prewarning threshold $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16 bit data word: with CS = high to low, the state of TP appears at Pin DO. After the μC has read this information, CS is set high and the data transfer is interrupted without affecting the state of input and output registers.

If the junction temperature exceeds the thermal shutdown threshold $T_{j\ switch\ off}$, the outputs are disabled and all bits in the output register are set high. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{j\ switch\ on}$, and when a high has been written to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

Short-Circuit Protection

The output currents are limited by a current regulator. Current limitation takes place when the overcurrent limitation and shutdown threshold (I_{HS1-6} , I_{LS1-6}) are reached. Simultaneously, an internal timer is started. The shorted output is disabled when during a permanent short the delay time (t_{dSd}) programmed by the short-circuit timer bit (SCT) is reached. Additionally, the short-circuit detection bit (SCD) is set. If the temperature prewarning bit TP in the output register is set during a short, the shorted output is disabled immediately and SCD bit is set. By writing a high to the SRR bit in the input register, the

SCD bit is reset and the disabled outputs are enabled.

Inhibit

There are two ways to inhibit the U6815BM:

1. Set bit SI in the input register to zero
2. Switch Pin 17 (INH) to 0 V

In both cases, all output stages are turned off but the serial interface stays active. The output stages can be activated again by bit SI = 1 or by Pin 17 (INH) switched back to 5 V.

Absolute Maximum Ratings

All values refer to GND pins

Parameter	Symbol	Value	Unit
Supply voltage Pins 5, 10	V_{VS}	-0.3 to 40	V
Supply voltage $t < 0.5$ s; $I_S > -2$ A Pins 5, 10	V_{VS}	-1	V
Supply voltage difference $ V_{S_Pin5} - V_{S_Pin10} $	ΔV_{VS}	150	mV
Supply current Pins 5, 10	I_{VS}	1.4	A
Supply current $t < 200$ ms Pins 5, 10	I_{VS}	2.6	A
Logic supply voltage Pin 19	V_{VCC}	-0.3 to 7	V
Input voltage Pin 17	V_{INH}	-0.3 to 17	V
Logic input voltage Pins 24 to 26	V_{DI}, V_{CLK}, V_{CS}	-0.3 to $V_{VCC} + 0.3$	V
Logic output voltage Pin 18	V_{DO}	-0.3 to $V_{VCC} + 0.3$	V
Input current Pins 17, 24 to 26	$I_{INH}, I_{DI}, I_{CLK}, I_{CS}$	-10 to +10	mA
Output current Pin 18	I_{DO}	-10 to +10	mA
Output current Pins 1 to 4, 11 to 16, Pins 27 and 28	I_{LS1} to I_{LS6} I_{HS1} to I_{HS6}	Internal limited, see output specification	mA
Reverse conducting current (tpulse = 150 μ s) Pins 2, 3, 12, 13, 15 28 towards Pins 5, 10	I_{HS1} to I_{HS6}	17	A
Junction temperature range	T_j	-40 to 150	$^{\circ}$ C
Storage temperature range	T_{STG}	-55 to 150	$^{\circ}$ C

Operating Range

All values refer to GND pins

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pins 5, 10	V_{VS}	$V_{UV}^{1)}$		40 ²⁾	V
Logic supply voltage	Pin 19	V_{VCC}	4.5	5	5.5	V
Logic input voltage	Pin 17, 24 to 26	$V_{INH}, V_{DI}, V_{CLK}, V_{CS}$	-0.3		V_{VCC}	V
Serial interface clock frequency	Pin 25	f_{CLK}			2	MHz
Junction temperature range		T_j	-40		150	$^{\circ}$ C

¹⁾ Threshold for undervoltage detection

²⁾ Output disabled for $V_{VS} > V_{OV}$ (threshold for overvoltage detection)

Thermal Resistance

All values refer to GND pins

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Junction – pin	Measured to GND Pins 6 to 9 and 20 to 23	R_{thJP}			25	K/W
Junction ambient		R_{thJA}			65	K/W

Noise and Surge Immunity

Parameters	Test Conditions	Value
Conducted interferences	ISO 7637-1	level 4 ¹⁾
Interference Suppression	VDE 0879 Part 2	level 5
ESD (Human Body Model)	MIL-STD-883D Method 3015.7	2 kV
ESD (Machine Model)	EOS / ESD – S 5.2	150 V

¹⁾ Test pulse 5: $V_{Smax} = 40$ V

Electrical Characteristics

7.5 V < V_{VS} < 40 V; 4.5 V < V_{VCC} < 5.5 V; INH = High; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$; unless otherwise specified, all values refer to GND pins.

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Current Consumption						
Quiescent current (VS)	$V_{VS} < 16$ V, INH or bit SI = low Pins 5, 10	I_{VS}			40	μA
Quiescent current (VCC)	4.5 V < $V_{VCC} < 5.5$ V, INH or bit SI = low Pin 19	I_{VCC}			20	μA
Supply current (VS) normal operating	$V_{VS} < 16$ V Pins 5, 10 all output stages off,	I_{VS}		0.8	1.2	mA
	all output stages on, no load	I_{VS}			10	mA
Supply current (VCC)	4.5 V < $V_{VCC} < 5.5$ V, normal operating Pin 19	I_{VCC}			150	μA
Internal Oscillator Frequency						
Frequency (Time-base for delay timers)		f_{OSC}	19		45	kHz
Over- and Undervoltage Detection, Power-On Reset						
Power-on reset threshold	Pin 19	V_{VCC}	3.4	3.9	4.4	V
Power-on reset delay time	After switching on V_{VCC}	t_{dPor}	30	95	160	μs
Undervoltage detection threshold	Pins 5, 10	V_{UV}	5.5		7.0	V
Undervoltage detection hysteresis	Pins 5, 10	ΔV_{UV}		0.4		V
Undervoltage detection delay		t_{dUV}	7		21	ms
Overvoltage detection thresh- old	Pins 5, 10	V_{OV}	18		22.5	V

Electrical Characteristics (continued)

7.5 V < V_{VS} < 40 V; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Overvoltage detection hysteresis	Pins 5, 10	ΔV_{OV}		1		V
Overvoltage detection delay	Input register bit 14 (SCT) = high	t _{dOV}	7		21	ms
Overvoltage detection delay	Input register bit 14 (SCT) = low	t _{dOV}	1.75		5.25	ms
Thermal Prewarning and Shutdown						
Thermal prewarning		T _{jPWset}	125	145	165	°C
Thermal prewarning		T _{jPWreset}	105	125	145	°C
Thermal prewarning hysteresis		ΔT_{jPW}		20		K
Thermal shutdown		T _{j switch off}	150	170	190	°C
Thermal shutdown		T _{j switch on}	130	150	170	°C
Thermal shutdown hysteresis		$\Delta T_{j switch off}$		20		K
Ratio thermal shutdown / thermal prewarning		T _{j switch off} / T _{jPW set}	1.05	1.17		
Ratio thermal shutdown / thermal prewarning		T _{j switch on} / T _{jPW reset}	1.05	1.2		
Output Specification (LS1 – LS6, HS1 – HS6) 7.5 V < V_{VS} < V_{OV}						
On resistance	I _{Out} = 600 mA Pins 1, 4, 11, 14, 16, 27	R _{DS On L}			1.5	Ω
On resistance	I _{Out} = -600 mA Pins 2, 3, 12, 13, 15, 28	R _{DS On H}			2.0	Ω
Output clamping voltage	I _{LS1-6} = 50 mA Pins 1, 4, 11, 14, 16, 27	V _{LS1-6}	40		60	V
Output leakage current	V _{LS1-6} = 40 V all output stages off Pins 1, 4, 11, 14, 16, 27	I _{LS1-6}			10	μA
Output leakage current	V _{HS1-6} = 0 V all output stages off Pins 2, 3, 12, 13, 15, 28	I _{HS1-6}	-10			μA
Inductive shutdown energy ¹⁾	Pins 1-4, 11-16, 27, 28	W _{outx}			15	mJ
Output voltage edge steepness	Pins 1-4, 11-16, 27, 28	dV _{LS1-6} /dt dV- HS1-6/dt	50	200	400	mV/μs
Overcurrent limitation and shutdown threshold	Pins 1, 4, 11, 14, 16, 27	I _{LS1-6}	650	950	1250	mA
Overcurrent limitation and shutdown threshold	Pins 2, 3, 12, 13, 15, 28	I _{HS1-6}	-1250	-950	-650	mA

¹⁾ Only valid for version U6815BM-N.

Electrical Characteristics (continued)

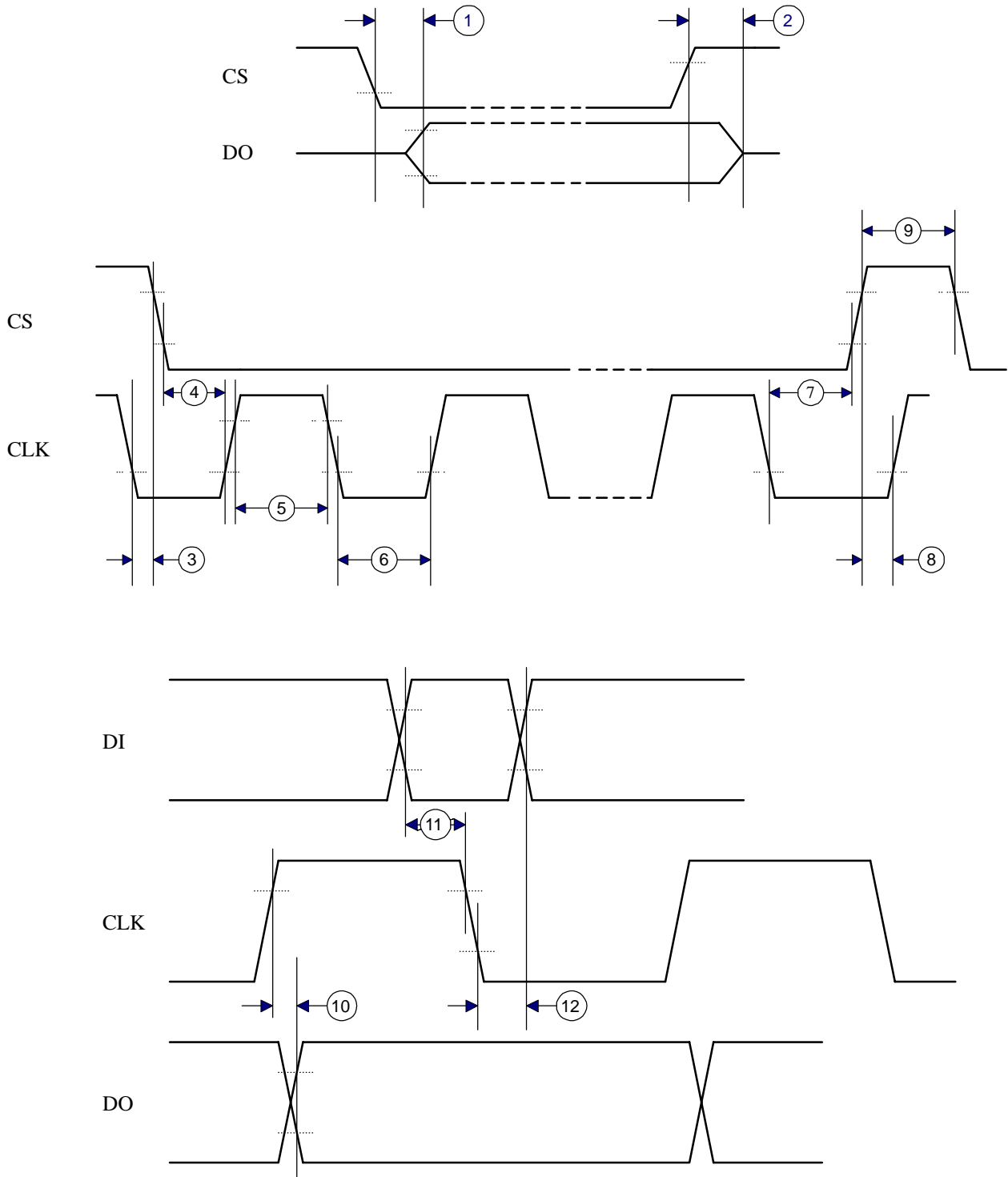
7.5 V < V_{VS} < 40 V; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Overcurrent shutdown delay time	Input register bit 14 (SCT) = high	t _{dSd}	70	100	140	ms
Overcurrent shutdown delay time	Input register bit 14 (SCT) = low	t _{dSd}	8.75		17.5	ms
Open load detection current	Input register bit 13 (OLD) =low, output off Pins 1, 4, 11, 14, 16, 27	I _{LS1-6}	60		200	μA
Open load detection current	Input register bit 13 (OLD) =low, output off Pins 2, 3, 12, 13, 15, 28	I _{HS1-6}	-150		-30	μA
Open load detection current ratio		I _{LS1-6} / I _{HS1-6}	1.2			
Open load detection threshold	Input register bit 13 (OLD) =low, output off Pins 1, 4, 11, 14, 16, 27	V _{LS1-6}	0.6		4	V
Open load detection threshold	Input register bit 13 (OLD) =low, output off Pins 2, 3, 12, 13, 15, 28	V _{VS-} V _{HS1-6}	0.6		4	V
Output Switch on delay ²⁾	R _{Load} = 1 kΩ	t _{don}			0.5	ms
Output Switch off delay ²⁾	R _{Load} = 1 kΩ	t _{doff}			1	ms
Inhibit Input						
Input voltage low level threshold	Pin 17	V _{IL}	0.3 × V _{VCC}			V
Input voltage high level threshold	Pin 17	V _{IH}			0.7 × V _{VCC}	V
Hysteresis of input voltage	Pin 17	ΔV _I	100		700	mV
Pull-down current	V _{INH} = V _{VCC} Pin 17	I _{PD}	10		80	μA
Serial Interface – Logic Inputs DI, CLK, CS						
Input voltage low level threshold	Pins 24-26	V _{IL}	0.3 × V _{VCC}			V
Input voltage high level threshold	Pins 24-26	V _{IH}			0.7 × V _{VCC}	V
Hysteresis of input voltage	Pins 24-26	ΔV _I	50		500	mV
Pull-down current Pin DI, CLK	V _{DI} , V _{CLK} = V _{VCC} Pins 25, 26	I _{PDSI}	2		50	μA
Pull-up current Pin CS	V _{CS} = 0 V Pin 24	I _{PUSI}	-50		-2	μA
Serial Interface – Logic Output DO						
Output-voltage low level	I _{OL} = 3 mA Pin 18	V _{DOl}			0.5	V
Output-voltage high level	I _{OL} = -2 mA Pin 18	V _{DOH}	V _{VCC} -1 V			V
Leakage current (tristate)	V _{CS} = V _{VCC} , 0 V < V _{DO} < V _{VCC} Pin 18	I _{DO}	-10		10	μA

²⁾ Delay time between rising edge of CS after data transmission and switch on output stages to 90% of final level.

Electrical Characteristics (continued)

Parameters	Test Conditions	Timing Chart No.	Symbol	Min.	Typ.	Max.	Unit
Serial Interface – timing							
DO enable after CS falling edge	$C_{DO} = 100 \text{ pF}$	1	t_{ENDO}			200	ns
DO disable after CS rising edge	$C_{DO} = 100 \text{ pF}$	2	t_{DISDO}			200	ns
DO fall time	$C_{DO} = 100 \text{ pF}$	–	t_{DOF}			100	ns
DO rise time	$C_{DO} = 100 \text{ pF}$	–	t_{DOR}			100	ns
DO valid time	$C_{DO} = 100 \text{ pF}$	10	t_{DOVal}			200	ns
CS setup time		4	$t_{CSSethl}$	225			ns
CS setup time	$V_{DO} < 0.2 \times V_{VCC}$	8	$t_{CSSethh}$	225			ns
CS high time	Input register Bit 14 (SCT) = high	9	t_{CSh}	140			ms
CS high time	Input register Bit 14 (SCT) = low	9	t_{CSh}	17.5			ms
CLK high time		5	t_{CLKh}	225			ns
CLK low time		6	t_{CLKl}	225			ns
CLK period time		–	t_{CLKp}	500			ns
CLK setup time		7	$t_{CLKsethl}$	225			ns
CLK setup time		3	$t_{CLKsetlh}$	225			ns
DI setup time		11	t_{DIset}	40			ns
DI hold time		12	t_{DIHold}	40			ns



Inputs DI, CLK, CS: High level = $0.7 \times V_{CC}$, Low level = $0.3 \times V_{CC}$
 Output DO: High level = $0.8 \times V_{CC}$, Low level = $0.2 \times V_{CC}$

Figure 4. Serial interface timing diagram with chart numbers

Application Circuit

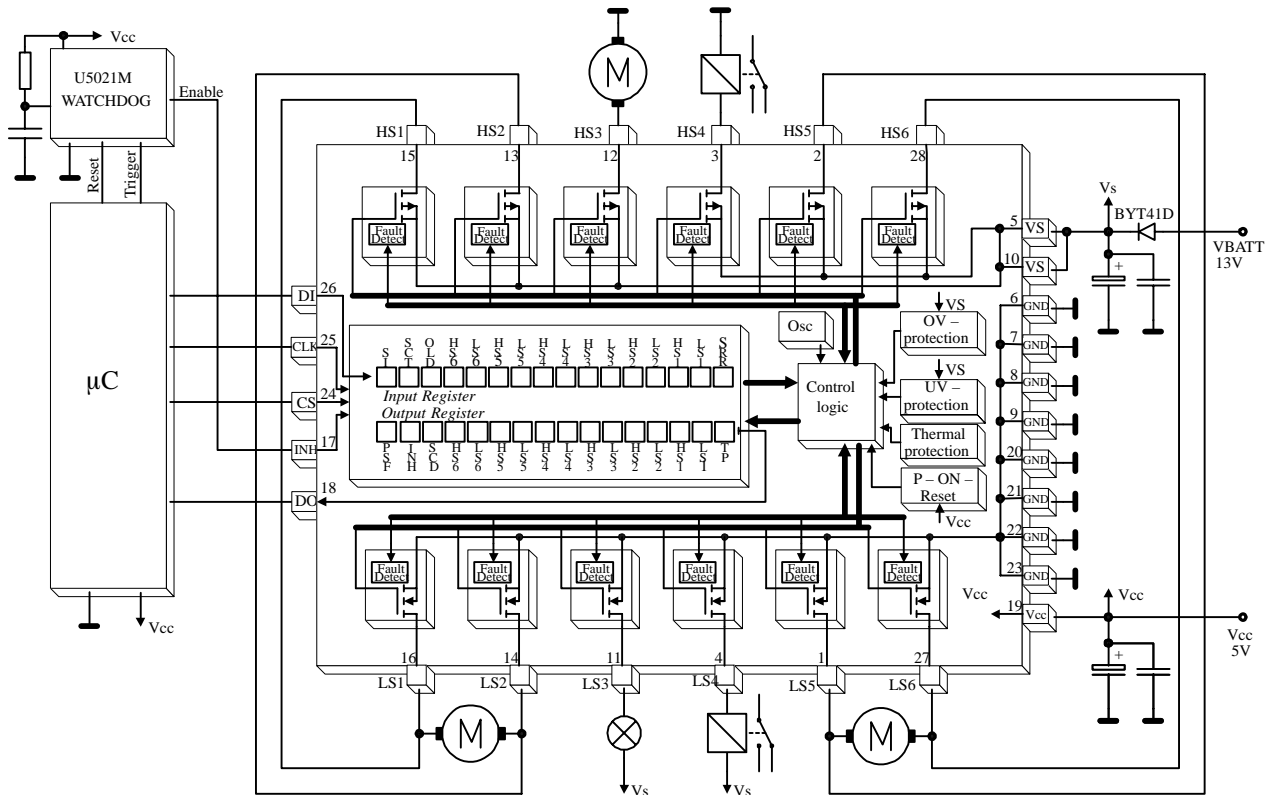


Figure 5. Application circuit

Application Notes

It is strongly recommended to connect the blocking capacitors at V_{CC} and V_S as close as possible to the power supply and GND pins.

Recommended value for capacitors at V_S :
 electrolytic capacitor $C > 22 \mu\text{F}$ in parallel with a ceramic capacitor $C = 100 \text{ nF}$. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current I_{HSx} (see Absolute Maximum Ratings).

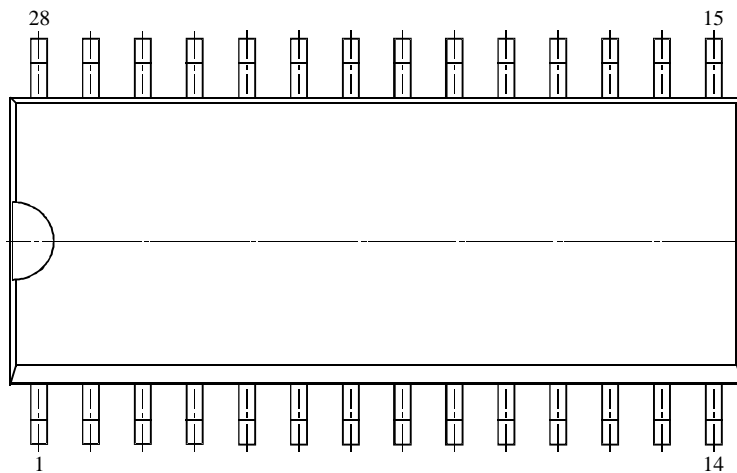
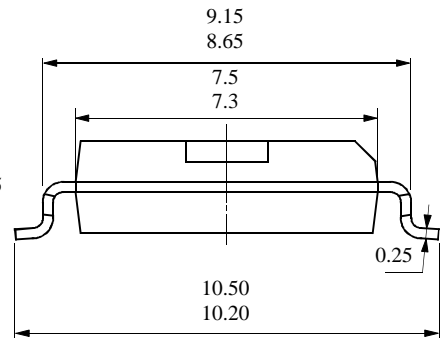
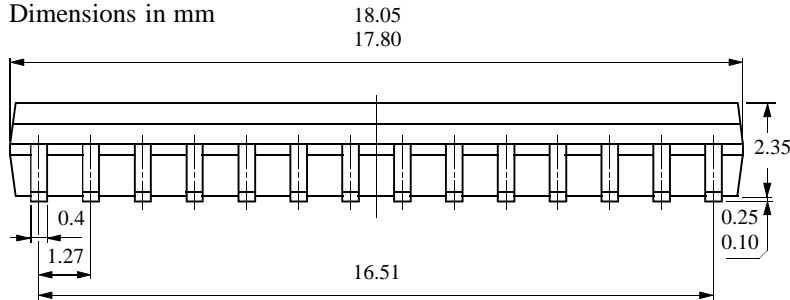
Recommended value for capacitors at V_{CC} :
 electrolytic capacitor $C > 10 \mu\text{F}$ in parallel with a ceramic capacitor $C = 100 \text{ nF}$.

To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to GND pins.

Package Information

Package SO28

Dimensions in mm




technical drawings
according to DIN
specifications

13033

Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Atmel Wireless & Microcontrollers products for any unintended or unauthorized application, the buyer shall indemnify Atmel Wireless & Microcontrollers against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Data sheets can also be retrieved from the Internet: <http://www.atmel-wm.com>

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