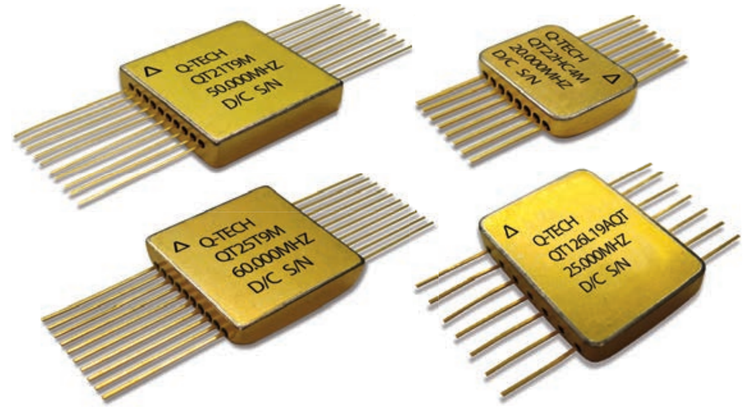
FLAT PACK
CRYSTAL CLOCK OSCILLATORS
-5.2 to -4.5Vdc & 1.8 to 15Vdc - 0.12Hz to 200MHz

Description

Q-Tech's flat pack crystal oscillators consist of a source clock square wave generator, logic output buffers and/or logic divider stages, and a round AT high-precision quartz crystal built in an all metal flat package.



Features

- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- USML Registration # M17677
- Wide frequency range from 0.12Hz to 200MHz
- Available as QPL MIL-PRF-55310/21 (TTL) QT24 only
- Choice of flat packs and pin outs
- Choice of supply voltages
- Choice of output logic options
- AT-Cut crystal
- All metal hermetically sealed package
- Tight or custom symmetry available
- Capacitive load drive capability (Z output)
- Low height
- External tuning capacitor option
- Fundamental and third overtone designs
- Tristate function option D
- Three-point crystal mounts
- Custom design available tailors to meet customer's needs
- Q-Tech does not use pure lead or pure tin in its products
- RoHS compliant

Ordering Information

(Sample part number)

QT25TD9M-60.000MHz

Q	T	25	T	D	9	M	-	60.000MHz

Solder Dip Option:
T = Standard
S = Solder Dip (*)

Package:
(See page 4)

Logic & Supply Voltage:

C =	CMOS +5.0V to +15.0V (**)	
AC =	ACMOS	+5.0V
HC =	HCMOS	+5.0V
T =	TTL	+5.0V
L =	LVHCMOS	+3.3V
N =	LVHCMOS	+2.5V
R =	LVHCMOS	+1.8V
E =	10K ECL	-5.2V
EH =	10KH ECL	-5.2V
EF =	100K/300K ECL	-4.5V
PE =	PECL	+5.0V
LP =	PECL	+3.3V
LW =	LVDS	+3.3V
NW =	LVDS	+2.5V
Z =	Z output	

Output Frequency

Screening Option:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

Frequency vs. Temperature Code:

1 =	± 100ppm at 0ºC to +70ºC
4 =	± 50ppm at 0ºC to +70ºC
5 =	± 25ppm at -20ºC to +70ºC
6 =	± 50ppm at -55ºC to +105ºC
9 =	± 50ppm at -55ºC to +125ºC
10 =	± 100ppm at -55ºC to +125ºC
11 =	± 50ppm at -40ºC to +85ºC
12 =	± 100ppm at -40ºC to +85ºC
19 =	± 15ppm at 23ºC ± 1ºC ± 50ppm at -55ºC to +125ºC reference to F at 23ºC

Tristate Option:
(Standard offering in LW & NW)
Blank = No Tristate
D = Tristate

(*) Hot Solder Dip Sn60/Pb40 per MIL-PRF 55310 is optional for an additional cost

(**) Please specify supply voltage when ordering CMOS

For frequency stability vs. temperature options not listed herein, request a custom part number.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Applications

- Designed to meet today's requirements for all voltage applications
- Wide military clock applications
- Industrial controls
- Microcontroller driver

Packaging Options

- Standard packaging in a locked anti-static cardboard

Other Options Available For An Additional Charge

- Lead forming available on all packages. Please contact for details.
- P. I. N. D. test (MIL-STD 883, Method 2020)
- Lead trimming

All Flat Pack packages are available in surface mount form.

Specifications subject to change without prior notice.

Electrical Characteristics

Parameters		C	AC	HC	T	L (*)	ECL / PECL (**)
Output freq. range (Fo)	QT21, 24, 25, 27	**500Hz — 15MHz**	**500Hz — 125MHz**	**0.12Hz — 125MHz**	**0.12Hz — 125MHz**	**0.12Hz — 160MHz**	**1MHz — 200MHz**
	QT22, 26, 28, 29	**500Hz — 15MHz**	**500Hz — 85MHz**	**500Hz — 85MHz**	**500Hz — 85MHz**	**500Hz — 85MHz**	**8MHz — 85MHz**
Supply voltage (Vdd)		5V ~ 15Vdc ± 10%	5.0Vdc ± 10%			3.3Vdc ± 10%	-5.2Vdc ± 5% (10K / 10KHECL) 5Vdc ± 5% (PECL) 3.3Vdc ± 5% (LVPECL)
Maximum Applied Voltage (Vdd max.)		-0.5 to +18Vdc	-0.5 to +7.0Vdc			-0.5 to +5.0Vdc	0 to -8.0Vdc (10K / 10KHECL) 0 to +8.0Vdc (PECL) 0 to +5.0Vdc (LVPECL)
Freq. stability ($\Delta F/\Delta T$)		See Option codes					
Operating temp. (Topr)		See Option codes					
Storage temp. (Tsto)		-62ºC to + 125ºC					
Operating supply current (Idd) (No Load)		F and Vdd dependent 3 mA max. at 5V up to 5MHz 25 mA max. at 15V up to 15MHz	20 mA max. - 0.12Hz ~ < 16MHz 25 mA max. - 16MHz ~ < 40MHz 35 mA max. - 40MHz ~ < 60MHz 45 mA max. - 60MHz ~ < 85MHz 60 mA max. - 85MHz ~ 125MHz			3 mA max. - 0.12Hz ~ < 500kHz 6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ < 130MHz 50 mA max. - 130MHz ~ 160MHz	45 mA max. - 8MHz ~ < 125MHz 75 mA max. - 125MHz ~ 200MHz
Symmetry (50% of ouput waveform or 1.4Vdc for TTL)		45/55% max. Fo < 4MHz 40/60% max. Fo ≥ 4MHz	45/55% max. Fo < 12MHz 40/60% max. Fo ≥ 12MHz				45/55% max. Fo < 12MHz 40/60% max. Fo ≥ 12MHz
Rise and Fall times (with typical load)		30ns max. (Measured from 10% to 90%)	15ns max. Fo < 15kHz 6ns max. Fo 15kHz ~ 39.999MHz 3ns max. Fo 40MHz ~ 160 MHz (Measured from 10% to 90% CMOS or from 0.8V to 2.0V TTL)				3.5ns max. Fo < 125MHz 3ns max. Fo 125MHz ~ 200MHz (Measured from 20% to 80%)
Output Load		**15pF // 10kΩ**			**10TTL Fo < 20MHz** 6TTL Fo ≥ 20MHz	**15pF // 10kΩ**	50Ω to -2V (10K / 10KH) 50Ω to Vcc -2V (P & LP)
Start-up time (Tstup)		10ms max.					
Output voltage (Voh/Vol)		0.9 x Vdd min.; 0.1 x Vdd max.			2.4V min.; 0.4V max.	0.9 x Vdd min.; 0.1 x Vdd max.	-1.15V min; -1.54V max. (E) 4V min.; 3.37V max. (PE) 2.27V min.; 1.68V max. (LP)
Output Current (Ioh/Iol)		± 1mA typ. at 5V ± 6.8mA typ. at 15V	± 24mA	±8 mA	-1.6mA / TTL +40µA / TTL	± 4mA .	-50mA
Enable/Disable Tristate function		Call for details	VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance			VIH ≥ 0.7 x Vdd Oscillation; VIL ≤ 0.3 x Vdd High Impedance	Call for details
Jitter RMS 1σ (at 25ºC)		8ps typ. - < 40MHz 5ps typ. - ≥ 40MHz				15ps typ. - < 40MHz 8ps typ. - ≥ 40MHz	Integrated phase jitter 12kHz - 20MHz 1ps typ.
Aging (at 70ºC)		± 5ppm max. first year / ± 2ppm typ. per year thereafter					

(*) Available in 2.5Vdc (N) or 1.8Vdc (R)
(**) Please contact Q-Tech for details on 100KECL logic (EF)
Z Output logic can drive up to 200 pF load with typical 6ns rise & fall times (tr, tf)

Electrical Characteristics

Parameters	LW	NW	Notes
Output frequency range (Fo)	**40.000MHz — 200.000MHz**	**80.000MHz — 200.000MHz**	**FP16, FP20**
Supply voltage (Vdd)	3.3Vdc ± 5%	2.5Vdc ± 5%	
Max. Applied Voltage	-0.5Vdc min. | +5Vdc max.		
Frequency stability (ΔF/ΔT)	See Option Codes		
Operating Temperature			
Storage Temperature	-62ºC to +125ºC		
Logic	LVDS		FP16, FP20
Input Current (Measured without Load at max. Vdd)	66 mA max.		
Output Voltage VOL	0.90V min. | 1.1V nom.		
Output Voltage VOH	1.65V min. | 1.45V nom.		
Differential Output Voltage (VOD)	247mV min. | 330 mV nom. | 454mV max.		
Offset Voltage (VOS)	1.125V min. | 1.125V nom. | 1.375V max.		
Output Waveform	Square Wave		
Rise and Fall Time	600ps max.		20% to 80%
Duty Cycle	45% min. | 50% nom. | 55% max.		
Load	100Ω		Connected between Q and QNOT
Frequency Aging after 30 days	±1.5 ppm ±2.0 ppm		40MHz < F < 150MHz F > 150MHz (Note 1)
Frequency Aging/Year	±5 ppm		(Note 2)
Start-up Time	10 ms		
Output Enable VIH	0.7 x Vdd min.		
Output Disable VIL	0.3 x Vdd max.		Output High Impedance

Notes:

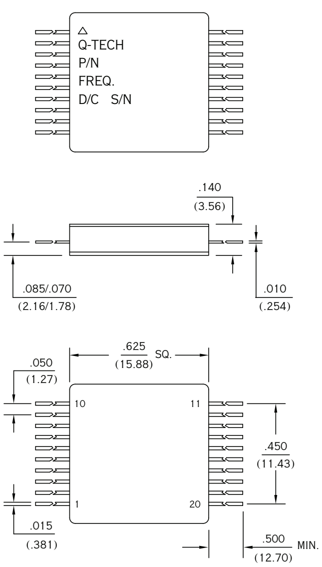
1. Normal frequency aging is up to 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exceeds 30 day aging limit.
2. Aging is ±5ppm after first year and ±2ppm/year thereafter.

Package Outline and Pin Connections

Dimensions are in inches (mm)

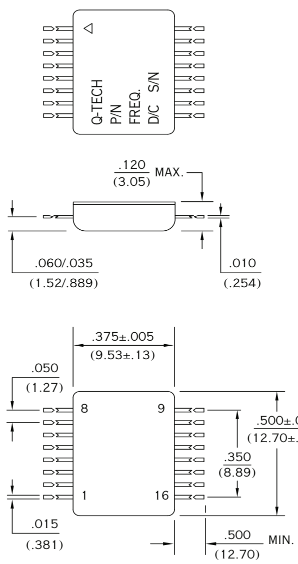
A

QT21



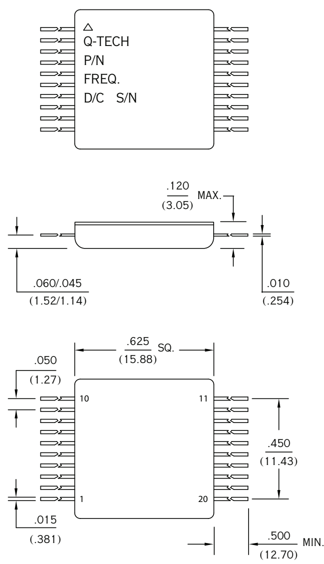
B

QT22



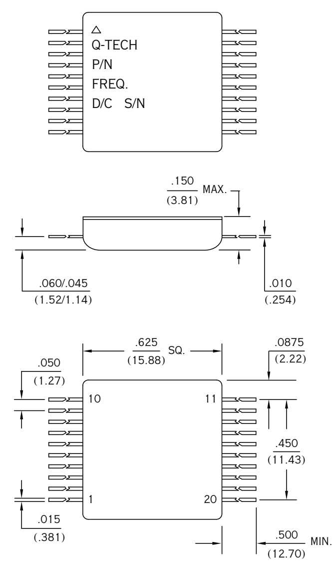
C

QT24



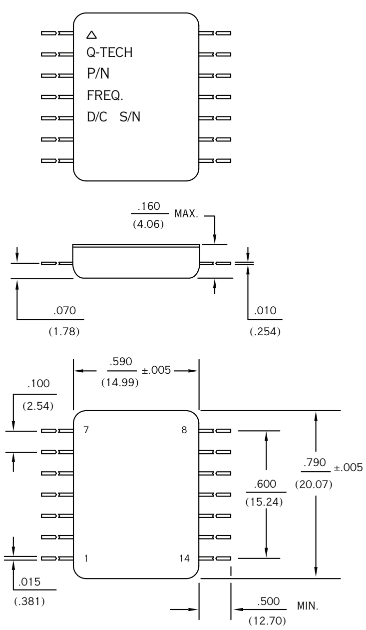
D

QT25



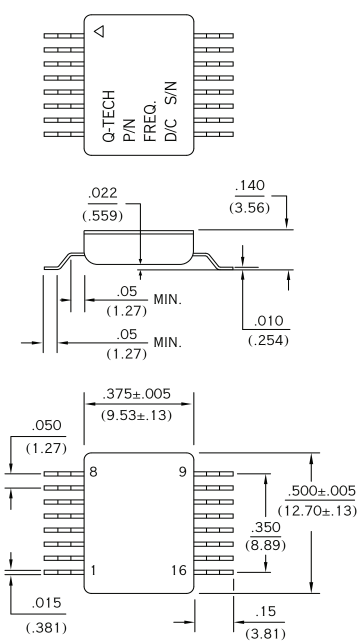
E

QT26



F

QT28



Pin Connections

QT #	Conf	Vcc	GND	Case	Output (*)	E/D or N/C	Equivalent MIL-PRF-55310 Configuration
QT21	A	13	10	10	11	12	N/A
QT22	B	8	9	9	10	11	N/A
QT24	C	13	10	10	11	12	/21 = QT24T
QT25	D	13	10	10	11	12	N/A
QT26	E	14	7	7	8	6	N/A
QT28	F	8	9	9	10	11	N/A

(*) ECL / PECL complimentary output available on pin 12 (except QT22, 26, & 28) with a Q-Tech custom part number

LVDS Pin Connections

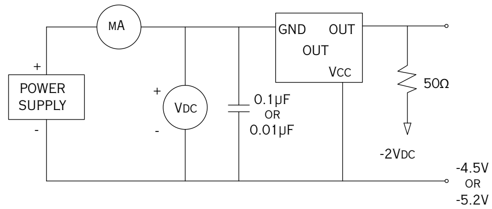
QT #	Conf	Vcc	GND	Case	Output (-)	Output (+)	E/D or N/C
QT21	A	13	10	10	11	12	8
QT22	B	8	9	9	10	11	7
QT24	C	13	10	10	11	12	8
QT25	D	13	10	10	11	12	8
QT26	E	N/A	N/A	N/A	N/A	N/A	N/A
QT28	F	8	9	9	10	11	7

Package Information

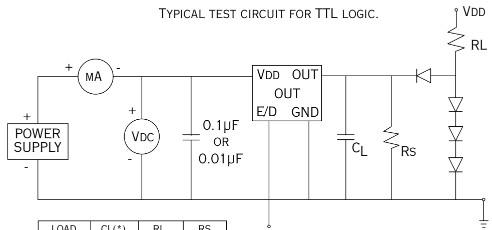
- Package material (Header and Leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches, Nickel Underplate – 100µ ~ 250µ inches
- Cover: Kovar, Gold Plated – 50µ ~ 100µ inches, Nickel Underplate – 70µ ~ 90µ inches
- Package to lid attachment: Seam weld
- Weight: 2.0g typ., 4.0g max.

Test Circuit

TYPICAL TEST CIRCUIT FOR ECL LOGIC.



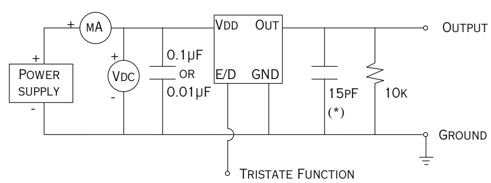
TYPICAL TEST CIRCUIT FOR TTL LOGIC.



LOAD	CL(*)	RL	RS
6 TTL	12PF	430Ω	10KΩ
10 TTL	20PF	270Ω	6KΩ

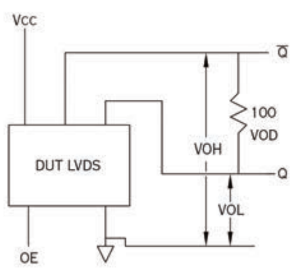
(*) CL INCLIDES THE LOADING EFFECT OF THE OSCILLOSCOPE PROBE.

TYPICAL TEST CIRCUIT FOR CMOS LOGIC



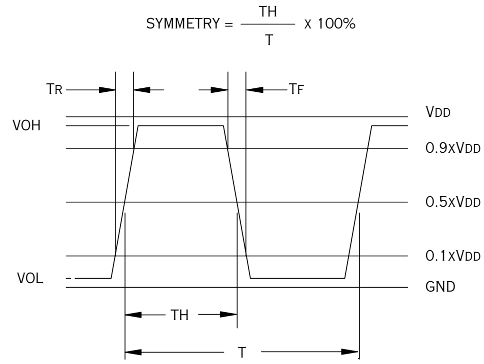
(*) CL INCLUDES PROBE AND JIG CAPACITANCE

The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.



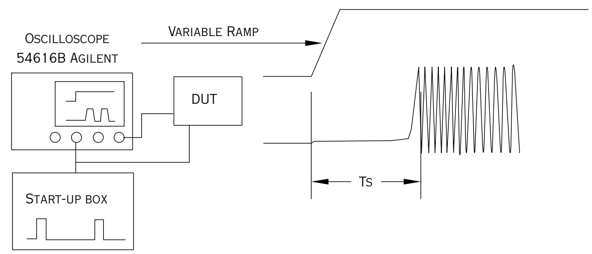
LVDS TERMINATION

Output Waveform (Typical)



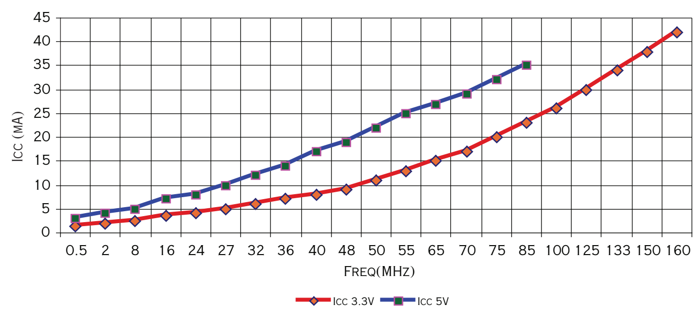
Startup Time

TYPICAL SET-UP FOR START-UP TIME

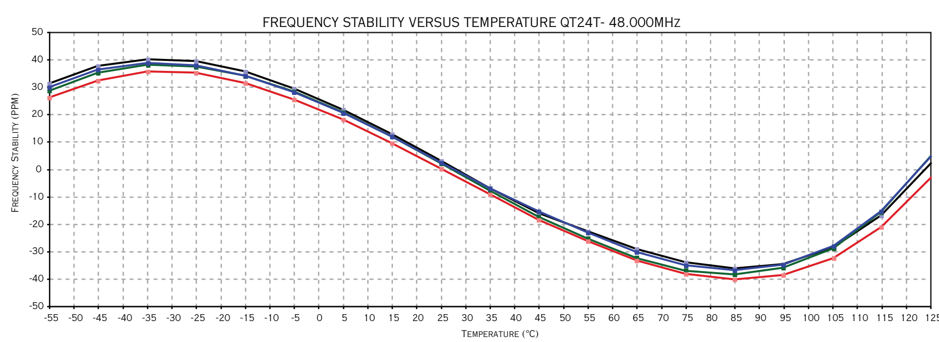


Supply Current

TYPICAL SUPPLY CURRENT ICC (MA) AT 3.3VDC & 5.0VDC CMOS LOGIC NO LOAD



Frequency vs. Temperature Curve



Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

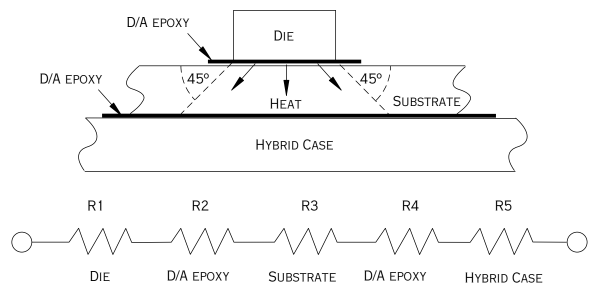
$$RT = R1 + R2 + R3 + R4 + R5$$

The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in°C/W.

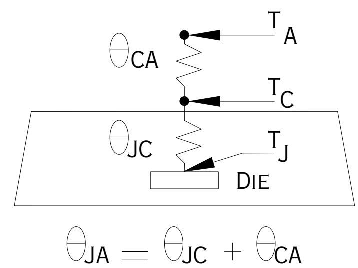
- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- PD(max) = (TJ (max) – TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 – 25)/130 = 1.15W



(Figure 1)



(Figure 2)

Environmental Sptecifications

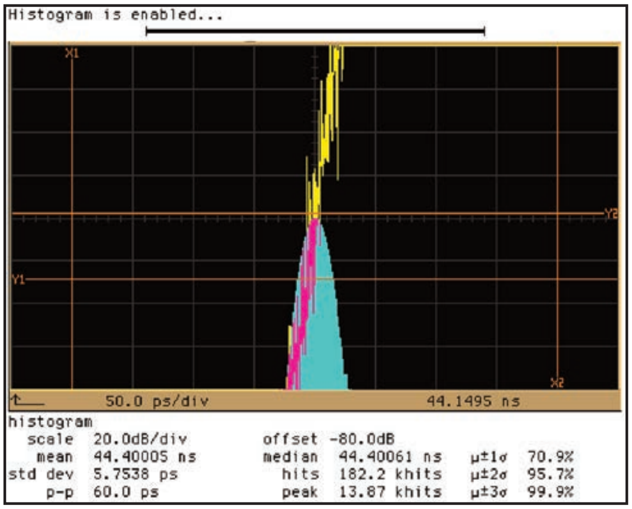
Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our Flat Packs. Q-Tech can also customize screening and test procedures to meet your specific requirements. The Flat Packs are designed and processed to exceed the following test conditions:

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ± 1.5ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. C
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1HBM 0 to 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

Please contact Q-Tech for higher shock requirements

Period Jitter

As data rates increase, effects of jitter become critical with its budgets tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random and deterministic jitter components. Random jitter (RJ) is theoretically unbounded and Gaussian in distribution. Deterministic jitter (DJ) is bounded and does not follow any predictable distribution. DJ is also referred to as systematic jitter. A technique to measure period jitter (RMS) one standard deviation (1σ) and peak-to-peak jitter in time domain is to use a high sampling rate (>8G samples/s) digitizing oscilloscope. Figure shows an example of peak-to-peak jitter and RMS jitter (1σ) of a QT24L-20MHz, at 3.3Vdc.



RMS jitter (1σ): 5.75ps Peak-to-peak jitter: 60ps

Phase Noise and Phase Jitter Integration

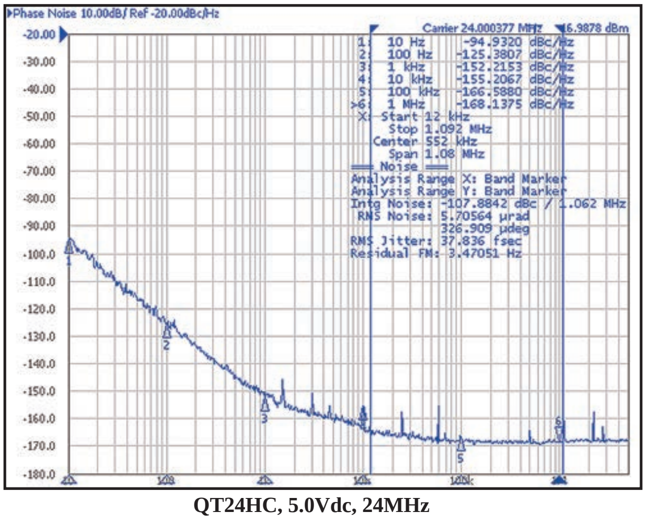
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

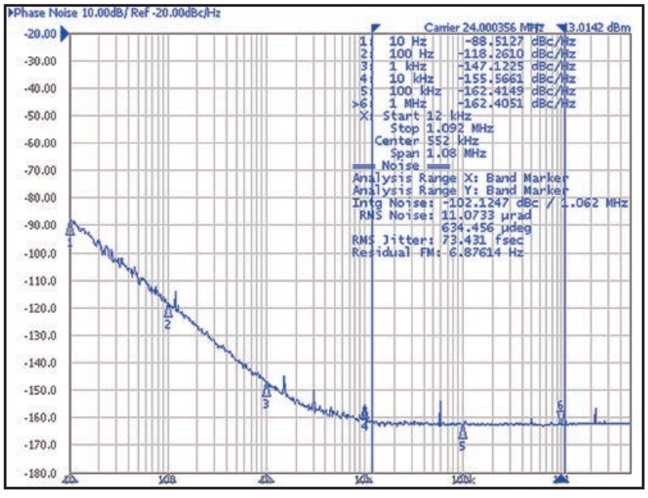
Symbol	Definition
$\int\mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi(f)=(180/\Pi)\times\sqrt{2\int\mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = Sφ (f)/(fosc.360°)	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT24HC, 5.0Vdc, 24MHz and QT24L, 3.3Vdc, 24MHz clock at offset frequencies 10Hz to 5MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



QT24HC, 5.0Vdc, 24MHz



QT24L, 3.3Vdc, 24 MHz

DCO	REV	REVISION SUMMARY	PAGE	DATE
6594	-	Rename document to QPDS-0131 from Flat Pack (Revision F, August 2010) (ECO# 9934)	All	3/28/17
		Add LVDS ordering options, Electrical Characteristics, pinout information, and test circuit	1, 3, 4, 5	
7323	A	Add frequency vs. temperature code 19 in ordering information	1	10/5/17