Rockwell

RC96V24DP and RC14V24DP Integrated Data/Fax/Voice Modem Engine

INTRODUCTION

The Rockwell RC96V24DP and RC14V24DP are low power data/fax/voice modem engines with enhanced Adaptive Differential Pulse Code Modulation (ADPCM) voice coding and decoding in a single VLSI package. The RC96V26DP and RC14V26DP provide additional V.26 support. The RC96V24DP is identical to the RC9624DP with the addition of enhanced ADPCM voice coding and decoding. Table 1 provides a feature comparison among these pin-compatible modem data pumps (MDPs).

Table 1. MDP Feature Comparison

MDP	V.23	ADPCM Voice	V.26	V.17	Bisync*	V.17/V.29 Short Train
RC9624DP	Yes	–	–	–	–	–
RC96V24DP	Yes	Yes	–	–	–	–
RC96V26DP	Yes	Yes	Yes	–	–	–
RC14V24DP	Yes	Yes	–	Yes	Yes	Yes
RC14V26DP	Yes	Yes	Yes	Yes	Yes	Yes

* Binary Synchronous Communication Protocol

These modems operate over the public switched telephone network (PSTN), as well as on point-to-point leased lines.

The RC96V24DP supports data modes meeting the requirements of CCITT V.21, V.22, V.22 bis, and V.23, as well as Bell 212A and 103, and fax modes meeting the requirements of CCITT V.29, V.27 ter, and V.21 channel 2 synchronous.

ADPCM voice coding and decoding provide voice compression and decompression supporting efficient digital storage of messages. Optional coder silence deletion and decoder silence interpolation increase compression rates. A voice pass-through (non-ADPCM) mode allows the host (DTE) to transceive uncompressed audio messages.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device or function in the host controller for products incorporating error correction and T.30 protocols.

The modems include two CMOS VLSI functions—a digital signal processor (DSP) and an integrated analog function (IA)—integrated into a single 68-pin plastic leaded chip carrier (PLCC) or 100-pin plastic quad flat pack (PQFP).

Detailed hardware and software interface information is described in the RC9624DP, RC96V24DP, and RC14V24DP Designer's Guide (Order No. 822 Rev. 2).

The general modem interface is shown in Figure 1.

FEATURES

- Single CMOS VLSI device
- Low power requirements
  - –Single voltage: + 5 Vdc ± 5%
  - –Operating: 190 mW (typical)
  - –Sleep: 10 mW (typical)
- 2-wire operation
  - –Full-duplex (FDX) for data modes
  - –Half-duplex (HDX) for fax modes
- Data configurations
  - –V.21, V.22, V.22 bis, V.23
  - –Bell 212A, Bell 103
  - –V.26, V.26 bis, V.26 Alternative A (RC96V26DP and RC14V26DP)
- Fax configurations
  - –V.29, V.27 ter, V.21 Channel 2
  - –V.17 (RC14V24DP and RC14V26DP)
- Enhanced ADPCM voice compression/decompression
  - –8-bits to 4, 3, or 2 bits per sample
  - –Programmable sample rate
  - –Coder silence deletion
  - –Decoder silence interpolation
  - –Concurrent DTMF reception and tone detection
- Voice pass-through mode
- Dual tone multifrequency (DTMF) detection
- Receive dynamic range: –9 dBm to –43 dBm
- Transmit level: –10 dBm ±1 dB using internal hybrid circuit; attenuation selectable in 1 dB steps
- Multi-mode data/fax detection support
- V.22 bis fallback/fall-forward – 2400/1200 bps
- Serial data: synchronous and asynchronous
- Parallel data: synchronous
  - –HDLC, NRZI
  - –Bisync (RC14V24DP and RC14V26DP)
- Parallel data: asynchronous
- Programmable ring detect
- Programmable dialer
- Programmable tone detect bandpass filters
- Adjustable speaker output to monitor received signal
- Network diagnostics support
- Host bus interface memory for configuration, control, and parallel data; 8086 microprocessor bus compatible
- 5-pin serial data interface; TTL compatible
- Adaptive and compromise equalization
- Local analog, local digital, and remote digital loopbacks
- Answer and originate handshake in data modes
- Training sequences for fax modes
- Leased line operation

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TRANSMIT TIMING

Transmitter timing is selectable between internal (±0.01%), external , or loopback. When external clock is selected, the external clock rate must equal the desired data rate ±0.01% with a duty cycle of 50 ± 20%.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler. The scrambler and descrambler can be enabled or disabled.

RECEIVE LEVEL

The receiver satisfies performance requirements for a received line signal from –9 dBm to –43 dBm. The default RLSD turn-on and RLSD turn-off thresholds are –43 dBm and –48 dBm, respectively. The RLSD threshold levels are programmable in DSP RAM.

Table 3. Dial Digits/Tone Pairs

Dial Digit	Tone 1 (Hz)	Tone 2 (Hz)
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
0	941	1336
*	941	1209
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

Table 2. Configurations, Signaling and Data Rates

Configuration	Modulation[1]	Transmitter Carrier Frequency (Hz) ±0.01% Answer[2]	Transmitter Carrier Frequency (Hz) ±0.01% Originate[2]	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits Per Symbol	Constellation Points	Sample Rate (Samples/Sec.)
Data Modes								
V.26 bis 2400	DPSK	1800	1800	2400	1200	2	4	9600
V.26 2400 A	DPSK	1800	1800	2400	1200	2	4	9600
V.26 1200	DPSK	1800	1800	1200	1200	1	2	9600
V.22 bis	QAM	2400	1200	2400[3]	600	4	16	7200
V.22	DPSK	2400	1200	1200[3]	600	2	4	7200
		2400	1200	600[3]	600	1	2	7200
Bell 212A	DPSK	2400	1200	1200[3]	600	2	4	7200
Bell 103	FSK	2225 M 2025 S	1270 M 1070 S	0-300[4]	0-300[4]	1	1	7200
V.21	FSK	1650 M 1850 S	980 M 1180 S	0-300[4]	0-300[4]	1	1	7500
V.23 Forward Channel	FSK	1300 M 2100 S	1300 M 2100 S	1200	1200	1	1	9600[5]
V.23 Backward Channel	FSK	390 M 450 S	390 M 450 S	75	75	1	1	7200
Fax Modes								
V.17	QAM	1800[6]	1800[6]	14400	2400	6	128	9600
	QAM	1800[6]	1800[6]	12000	2400	5	64	9600
	QAM	1800[6]	1800[6]	9600	2400	4	32	9600
	QAM	1800[6]	1800[6]	7200	2400	3	16	9600
V.29	QAM	1700	1700	9600	2400	4	16	9600
	QAM	1700	1700	7200	2400	3	8	7200
	QAM	1700	1700	4800	2400	2	4	9600
V.27 ter	DPSK	1800	1800	4800	1600	3	8	9600
	DPSK	1800	1800	2400	1200	2	4	9600
V.21 channel 2	FSK	1650 M 1850 S	1650 M 1850 S	300	300	1	1	9600
Dial/Call Progress Mode					600			7200
Tone Generator/ Tone Detector Mode					600			7200

Notes:

1. Modulation legend: QAM Quadrature Amplitude Modulation
   DPSK Differential Phase Shift Keying
   FSK Frequency Shift Keying
2. M indicates a mark condition; S indicates a space condition.
3. Synchronous accuracy = ±0.01%; asynchronous accuracy = –2.5% to +1.0% (+2.3% if extended overspeed is selected).
4. Value is upper limit for serial (e.g., 0-300).
5. 9600 samples per second in V.23 FDX Tx75/Rx1200, or V.23 HDX Tx or Rx 1200;
   7200 samples per second in V.23 FDX Tx1200/Rx75, or V.23 HDX Tx or Rx 75.
6. 1700 Hz carrier option (see bit CRR17 in the RC14V24DP and RC14V26DP Interface Memory Map, Figure 4b).

RECEIVER TIMING

The modem can track a frequency error up to ±0.03% in the associated transmit timing source.

CARRIER RECOVERY

The modem can track a frequency offset up to ±7 Hz in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

RTS-CTS TURN-ON AND TURN-OFF SEQUENCES

RTS ON to CTS ON and RTS OFF to CTS OFF response times are listed in Table 4 (long trains only).

Turn-On Sequences.

When a modem is configured for V.26 bis or V.26 Alternative A, the turn-on sequence consists of two segments. The first segment is continuous unscrambled ones. The second segment may be either continuous unscrambled or scrambled ones depending on whether the scrambler/descrambler is selected. When selected, scrambling in the transmitter and descrambling in the receiver is done in accordance with CCITT V.27 ter. The duration of each segment is programmable in 0.833 ms increments from 0 to 54.6 seconds with a 30 ms default segment duration.

Turn-Off Sequences.

For V.26 bis or V.26 Alternate A, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled or unscrambled ones.

For V.21, the transmitter turns off within 10 ms after RTS goes OFF.

For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 50 ms period of no transmitted energy.

For V.27 ter, the turn-off sequence consists of approximately 7 ms of remaining data and scrambled ones at 1200 baud or approximately 7.5 ms of data and scrambled ones at 1600 baud followed by 20 ms of no transmitted energy.

For V.17, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy.

Table 4. RTS-CTS Response Times

Configuration	Turn On Time	Turn Off Time
Data Modes		
V.26 (All speeds)	Programmable	10 ms
V.22 bis, V.22, and Bell 212A (CC bit = 0)	≤2 ms	≤ 2 ms
V.22 bis, V.22, and Bell 212A (CC bit = 1)	270 ms	≤ 2 ms
V.21 and Bell 103	2-5 ms	10 ms
V.23	11 ms	≤ 2 ms
Fax Modes		
Echo Protector Tone Disabled (NV25 = 1)		
V.29 (All speeds)	253 ms	≤ 2 ms
V.27 ter 4800	898 ms	≤ 2 ms
V.27 ter 2400	1133 ms	9 ms
V.21	20 ms	4 ms
V.17 (All speeds)	1393 ms	5 ms
Echo Protector Tone Enabled (NV25 = 0)		
V.29 (All speeds)	440 ms	≤ 2 ms
V.27 ter 4800	1103 ms	≤ 2 ms
V.27 ter 2400	1338 ms	9 ms
V.21	3095 ms	4 ms
V.17 (All speeds)	1598 ms	5 ms

SERIAL OR PARALLEL INTERFACE

The TPDM bit selects serial or parallel interface.

Serial Interface. The five hardware lines (RXD, TXD, TDCLK, RDCLK, and XTCLK) are supported by four control and status bits in the interface memory (CTS, DSR, RTS, and RLSD).

Parallel Interface. An 8086-compatible parallel microprocessor bus is supported.

VOICE PASS-THROUGH (NON-ADPCM) MODE

Transmit Voice. Transmit voice samples are sent to the modem digital-to-analog converter (DAC) from the host through the transmit data buffer (TBUFFER).

Receive Voice. Received voice samples from the modem analog-to-digital converter (ADC) are read by the host from the receive data buffer (RBUFFER).

ADPCM VOICE MODE

Transmit Voice. Compressed transmit voice is sent to the modem ADPCM codec for decompression then to the DAC by the host through the transmit data buffer.

Receive Voice. Received voice samples from the modem ADC are sent to the ADPCM codec for compression, and then read by the host from the receive data buffer.

ASYNCHRONOUS CONVERSION

Asynchronous mode is selected by the ASYNC bit. The asynchronous character format is 1 start bit, 5 to 8 data bits (WDSZ bits), an optional parity bit (PARSL and PEN bits), and 1 or 2 stop bits (STB bit). Valid character size, including all bits, is 7, 8, 9, 10 or 11 bits per character.

Signaling Rate Range. Basic range (+1% to –2.5%) or Extended overspeed range (+2.3% to –2.5%) is selectable by the EXOS bit.

Break. Break is handled as described in V.22 bis.

SLEEP MODE

Via host control, the modem enters sleep mode (SLEEP=1) which significantly reduces modem power consumption. Return to normal modem operation is accomplished by either applying a reset pulse, or by performing a dummy interface memory write operation.

POWER AND ENVIRONMENTAL REQUIREMENTS

The power requirements are specified in Table 5. The environmental specifications are listed in Table 6.

Table 5. Modem Power Requirements

Voltage	Mode	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
5 VDC ±5%	Operating	38 mA	48 mA
	Sleep	2 mA	2.5 mA
Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 microvolts peak.			

Table 6. Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to 70°C (32°F to 158°F)
Storage	–40°C to 80°C (–40°F to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	– 200 feet to +10,000 feet

HARDWARE INTERFACE

The modem functional hardware interface signals are shown in Figure 2. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{IRQ}$). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The modem pin assignments are shown in Figure 3. The pin assignments are listed by pin number in Table 7.

The hardware interface signal functions are summarized by major interface in Table 8.

The analog and digital interface characteristics are defined in Tables 9 and 10, respectively.

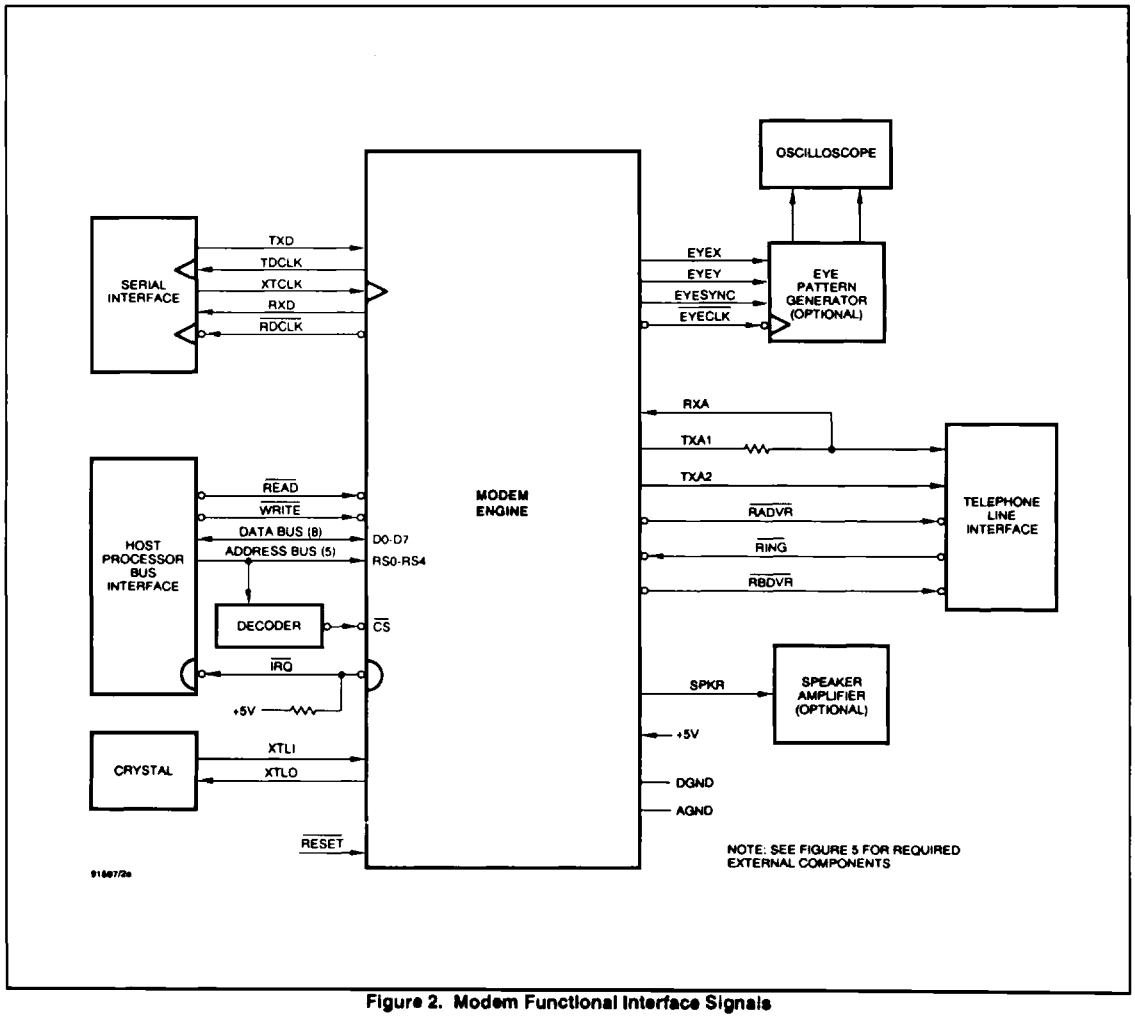
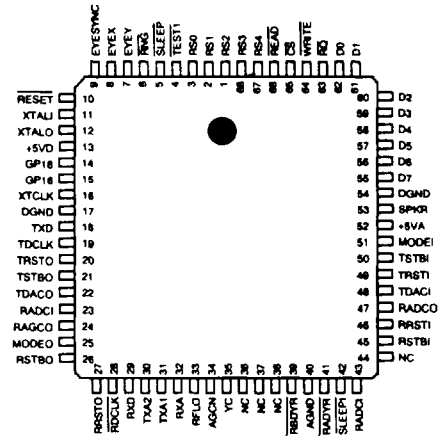
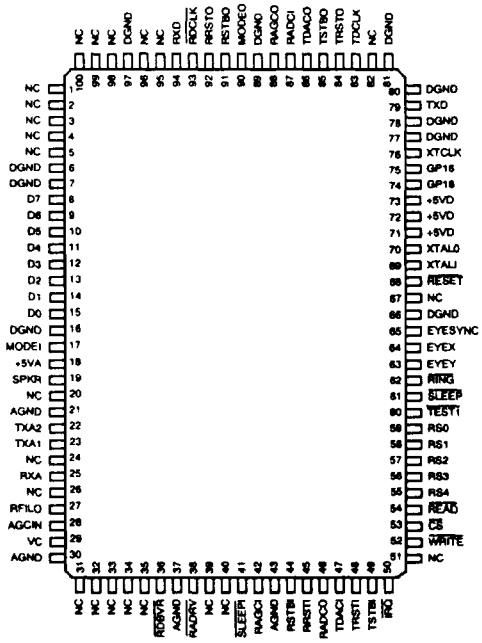


Figure 2. Modem Functional Interface Signals



a. 68-Pin PLCC



b. 100-Pin PQFP

Figure 3. Pin Signals

Table 7. Pin Signals

68-Pin PLCC Pin Number	100-Pin PQFP Pin Number	Signal Name	I/O Type
1	57	RS2	IA
2	58	RS1	IA
3	59	RS0	IA
4	60	TEST1	
5	61	SLEEP	OA
6	62	RING	
7	63	EYEY	OB
8	64	EYEX	OB
9	65	EYESYNC	OB
10	68	RESET	ID
11	69	XTLI	IE
12	70	XTLO	OB
13	71,72,73	+5VD	
14	74	GP18	OA
15	75	GP16	OA
16	76	XTCLK	IA
17,54	6,7,16, 66,77,78, 80,81,89,97	DGND	
18	79	TXD	IA
19	83	TDCLK	OA
20	84	TRSTO	MI
21	85	TSTBO	MI
22	86	TDACO	MI
23	87	RADCI	MI
24	88	RAGCO	MI
25	90	MODEO	MI
26	91	RSTBO	MI
27	92	RRSTO	MI
28	93	RDCLK	OA
29	94	RXD	OA
30	22	TXA2	O(DD)
31	23	TXA1	O(DD)
32	25	RXA	I(DA)
33	27	RFILO	MI
34	28	AGCIN	MI
35	29	VC	
39	36	RBDVR	OD
40	21,30,37,43	AGND	
41	38	RADRV	OD
42	41	SLEEPI	IA
43	42	RAGCI	MI
45	44	RSTBI	MI
46	45	RRSTI	MI
47	46	RADCO	MI
48	47	TDACI	MI
49	48	TRSTI	MI
50	49	TSTBI	MI
51	17	MODEI	MI

Table 7. Pin Signals (Cont'd)

68-Pin PLCC Pin Number	100-Pin PQFP Pin Number	Signal Name	I/O Type
52	18	+5VA	
53	19	SPKR	O(DF)
55	8	D7	IA/OB
56	9	D6	IA/OB
57	10	D5	IA/OR
58	11	D4	IA/OB
59	12	D3	IA/OB
60	13	D2	IA/OB
61	14	D1	IA/OB
62	15	D0	IA/OB
63	50	IRQ	OC
64	52	WRITE	IA
65	53	CS	IA
66	54	READ	IA
67	55	RS4	IA
68	56	RS3	IA
36,37,38,44	1,2,3,4,5,20, 24,26,31,32, 33,34,35,39, 40,51,67,82, 95,96,98,99, 100	No Connect Pins	

Notes:
1. MI = Modem Interconnection.
2. NC = No connection (may have internal connection; leave pin disconnected (open)).
3. I/O types are described in Table 9 (analog signals) and Table 10 (digital signals).

Table 8. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	IE OB	**Crystal/Clock In and Crystal Out.** The DSP must be connected to an external crystal circuit consisting of a crystal (24.00014 MHz for the RC96V24DP and RC96V26DP, and 19.000265 MHz for the RC14V24DP and RC14V26DP) and two capacitors. Alternatively, XTLI, may be driven with a buffered clock (e.g., square wave generator) or a sine wave oscillator.
$\overline{\text{RESET}}$	ID	**Reset.** The active low $\overline{\text{RESET}}$ input resets the internal modem logic. Upon transition of $\overline{\text{RESET}}$ from low-to-high, the DSP interface memory bits are set to the default values.
+ 5VD	PWR	**+ 5V Digital Supply.** +5V ±5% is required.
+ 5VA	PWR	**+ 5V Analog Supply.** +5V ±5% is required.
DGND	GND	**Digital Ground.**
AGND	GND	**Analog Ground.**
		SERIAL INTERFACE
		Five TTL-level hardware interface circuits implement a CCITT V.24-compatible serial data interface with control signals provided through the DSP interface memory.
$\overline{\text{RDCLK}}$	OA	**Receive Data Clock.** In synchronous mode, the modem outputs a Receive Data Clock ($\overline{\text{RDCLK}}$) in the form of 50 ±1% duty cycle square wave. The low-to-high transitions of this output coincide with the center of received data bits.
TDCLK	OA	**Transmit Data Clock.** In synchronous mode, the modem outputs a Transmit Data Clock (TDCLK). The TDCLK clock frequency is data rate ±0.01% with a duty cycle of 50 ± 1%.
XTCLK	IA	**External Transmit Clock.** In synchronous mode, an external transmit data clock input (XTCLK) can be supplied.
RXD	OA	**Received Data.** The modem presents received serial data on the Received Data (RXD) output and to the interface memory Receive Data Register (RBUFFER) in both serial and parallel modes.
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted on the TXD input in serial mode, or from the interface memory Transmit Data Register (TBUFFER) in parallel mode. (See TPDM bit.)
		PARALLEL MICROPROCESSOR INTERFACE
		Address, data, control and interrupt hardware interface signals implement an 8086-compatible parallel microprocessor interface to a host processor. This parallel interface allows the host to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
D0–D7	IA/OA	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem.
$\overline{\text{CS}}$	IA	**Chip Select.** The active low Chip Select ($\overline{\text{CS}}$) input enables parallel data transfer over the microprocessor bus.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers in the modem when $\overline{\text{CS}}$ is low. These lines are typically connected to address lines A0–A4 to address one of 32 8-bit internal interface memory registers (00–1F). The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).
$\overline{\text{READ}}$ $\overline{\text{WRITE}}$	IA	**Read Enable and Write Enable.** Reading or writing is controlled by the host pulsing either $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ input low, respectively, during the microprocessor bus access cycle. During a write cycle, data from the data bus is copied into the addressed DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
$\overline{\text{IRQ}}$	OA	**Interrupt Request.** The $\overline{\text{IRQ}}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{\text{IRQ}}$ output can be enabled in the interface memory to allow immediate indication of change of conditions in the modem. The use of $\overline{\text{IRQ}}$ is optional depending upon modem application.

Table 8. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		HYBRID CIRCUIT
TXA1 TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other.
RXA	I(DA)	**Receive Analog.** RXA is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit.
VC	OA	**Centerpoint Voltage.** VC is a +2.5 VDC centerpoint voltage which serves as the internal "analog ground" reference point.
		TELEPHONE LINE INTERFACE
$\overline{\text{RADVR}}$	OD	**Relay A Driver.** $\overline{\text{RADVR}}$ is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate" voltage of no greater than 4.0 VDC. The $\overline{\text{RADVR}}$ output is controlled by the state of the RA bit, except in pulse dial mode. When RA is a 1, the $\overline{\text{RADVR}}$ output is active which applies current to the relay coil. In a typical application, $\overline{\text{RADVR}}$ is connected to the normally open Off-Hook relay. In this case, $\overline{\text{RADVR}}$ active closes the Off-Hook relay to connect the modem to the telephone line.
$\overline{\text{RBDVR}}$	OD	**Relay B Driver.** $\overline{\text{RBDVR}}$ is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate" voltage of no greater than 4.0 VDC. $\overline{\text{RBDVR}}$ output is controlled by the state of the RB bit. When RB is a 1, the $\overline{\text{RBDVR}}$ output is active which applies current to the relay coil. In a typical application, $\overline{\text{RBDVR}}$ is connected to the normally closed Talk/Data relay. In this case, $\overline{\text{RBDVR}}$ active opens the relay to disconnect the handset from the telephone line.
$\overline{\text{RING}}$	IA	**Ring Frequency.** A low-going edge on the $\overline{\text{RING}}$ input initiates a ring frequency measurement. A valid ring detection is indicated by the RI bit.
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR on/off and three levels of attenuation are controlled by interface memory bits. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier.
		SLEEP MODE SIGNALS
$\overline{\text{SLEEP}}$ $\overline{\text{SLEEPI}}$	OA IA	**Sleep Mode Output and Sleep Mode Input.** $\overline{\text{SLEEP}}$ output high indicates the DSP is operating in its normal mode. $\overline{\text{SLEEP}}$ low indicates that the DSP is in the sleep mode. This signal must be connected to the $\overline{\text{SLEEPI}}$ input to power down the IA in the sleep mode. $\overline{\text{SLEEP}}$ can also be used to control power to other devices (e.g., as a speaker enable).
		DIAGNOSTIC SIGNALS Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEX, EYEY	OB	**Eye Pattern Data X and Eye Pattern Data Y.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope horizontal (X) axis and vertical (Y) axis, respectively. This serial digital data can be converted to analog form using two shift registers and two digital-to-analog converters (DACs).
$\overline{\text{EYECLK}}$ (RRSTO)	OA	**Eye Pattern Clock.** EYECLK is a clock for use by the serial-to-parallel converters. The $\overline{\text{EYECLK}}$ output is a 7200/9600 Hz clock.
EYESYNC	OB	**Eye Pattern Sync.** EYESYNC is a strobe for word synchronization. The falling edge of EYESYNC may be used tc transfer the 8-bit word from the shift register to a holding register. Digital-to-analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Table 8. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		MODEM INTERCONNECT
RFILO	MI	**Receive Filter Output.** RFILO is the output of the internal receive analog filter which must be connected to AGCIN through a 0.1 µF, 20%, DC decoupling capacitor.
AGCIN	MI	**Receive AGC Gain Amplifier Input.** See RFILO.
MODEO (DSP), MODEI (IA)	MI	**Mode Control.** Serial IA mode control bits. Direct modem interconnect line.
TDACO (DSP), TDACI (IA)	MI	**Transmitter DAC Signal.** Transmitter serial digital DAC signal. Direct modem interconnect line.
TSTBO (DSP), TSTBI (IA)	MI	**Transmitter Strobe.** Transmitter 576 kHz digital timing reference. Direct modem interconnect line.
TRSTO (DSP), TRSTI (IA)	MI	**Transmitter Reset.** Transmitter 7200/9600 Hz digital timing reference. Direct modem interconnect line.
RADCI (DSP), RADCO (IA)	MI	**Receiver ADC Signal.** Receiver serial digital ADC signal. Direct modem interconnect line.
RAGCO (DSP), RAGCI (IA)	MI	**Receiver AGC Signal.** Receiver serial digital AGC signal. Direct modem interconnect line.
RSRBO (DSP), RSRBI (IA)	MI	**Receiver Strobe.** Receiver 576 kHz digital timing reference. Direct modem interconnect line.
RRSTO (DSP), RRSTI (IA)	MI	**Receiver Reset.** Receiver 7200/9600 Hz digital timing reference. Direct modem interconnect line.

Table 9. Analog Interface Characteristics

Name	Type	Characteristic	
RXA	I (DA)	Input Impedance: Voltage Range:	> 50K-ohms 2.5 ±1.6 V
TXA1, TXA2	O (DD)	Minimum Load: Maximum Capacitive Load: Output Impedance: Output Voltage: D.C. Offset:	300 ohms 0.01µF < 10 ohms 2.5 ± 1.6 V < 200 mV
SPKR	O (DF)	Minimum Load: Maximum Capacitive Load: Output Impedance: Output Voltage: D.C. Offset:	300 ohms 0.01 µF < 10 ohms 2.5 ± 1.6 V < 20 mV

Table 10. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type IA		2.0	-	V_{CC}		
Type ID		0.8(V_{CC})	-	V_{CC}		
Type IE		-	4.0	-		Note 2.
Input Low Voltage	V_{IL}				Vdc	
Type IA and ID		-0.3	-	0.8		
Type IE		-	1.0	-		Note 2.
Input Leakage Current	I_{IN}				µAdc	
Type IA (Non-multiplexed)		-	-	±2.5		V_{IN} = 0 to V_{CC}
Type IE		-	-	±2.5		V_{IN} = 0 to +5V, V_{CC} = 5.25 V
Input Low Current: Type IB	I_{IL}	-	-	-400	µAdc	V_{CC} = 5.25 V
Output High Voltage	V_{OH}				Vdc	
Types OA and OB		3.5	-	-		I_{LOAD} = - 100 µA
Type OD		-	-	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				Vdc	
Types OA and OC		-	-	0.4		I_{LOAD} = 1.6 mA
Type OB		-	-	0.4		I_{LOAD} = 0.8 mA
Type OD		-	0.75	-		I_{LOAD} = 15 mA
Output High Current: Type OD	I_{OH}	-	-	-0.1	mAdc	
Output Low Current: Type OD	I_{OL}	-	-	100	µAdc	
Output Leakage Current Types OA and OB	I_{LO}	-	-	±10	µAdc	V_{IN} = 0.4 to V_{CC} -1
Capacitive Load: Types IA and ID	C_L	-	5	-	pF	
Capacitive Drive	C_D				pF	
Types OA and OB		-	100	-		
Type OD		-	50	-		
Circuit Type						
Type IA						TTL
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC						Open drain
Type OD						Clock
Three-State (Off) Current	I_{TSI}				µAdc	
Type OA		-	-	±10		V_{IN} = 0.8 V to 4.5 V @ 500 kHz
Type OB and OC		-	-	±10		V_{IN} = 0.8 V to V_{CC} -1 V
Power Dissipation	P_D				mW	
Operating		-	190	240		
Sleep		-	10	12.5		

Notes: 1. Test Conditions: V_{CC} = 5V ± 5%, TA = 0°C to 70°C (unless otherwise noted).
2. Type IE inputs are centered at approximately 2.5 V and swing 1.5 V_{PEAK} in each direction.

SOFTWARE INTERFACE

INTERFACE MEMORY

The DSP communicates with the host by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAP

The memory maps of DSP interface memory identifying the contents of the 32 addressable registers are shown in Figure 4a for the RC96V24DP and RC96V26DP, and in Figure 4b for the RC14V24DP and RC14V26DP. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

INTERFACE MEMORY BIT FUNCTIONS

Table 11 summarizes the functions of the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is denoted by Z (00 through 1F) and the bit number is located by Q (0 through 7, where 0 = LSB).

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0
Interrupt Handling	1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
	1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
RAM Access, Control, and Status	1D	XACC	—	—	—	IOX	XCRD	XWT	XCR
	1C	X RAM ADDRESS (XADD)							
	1B	YACC	—	—	—	—	YCRD	YWT	YCR
	1A	Y RAM ADDRESS (YADD)							
	19	X RAM DATA MSB (XDAM)							
	18	X RAM DATA LSB (XDAL)							
	17	Y RAM DATA MSB (YDAM)							
	16	Y RAM DATA LSB (YDAL)							
—	15	—	—	—	—	—	—	—	—
—	14	—	—	—	—	—	—	—	—
Control	13	TLVL				VOL		TXCLK	
	12	CONFIGURATION (CONF)							
Transmit Data Buffer	11	—	—	—	—	—	—	—	TXP
	10	TRANSMIT DATA BUFFER (TBUFFER)							
Status	0F	RLSD	FED	CTS	DSR	RI	TM	SYNCD	FLAGS
	0E	RTDET	BRKD	PE	FE	OE	SPEED		
	0D	—	PNDET	S1DET	SCR1	U1DET	SADET	—	—
	0C	EDET	—	—	—	DTDIG			
	0B	TONEA	TONEB	TONEC	ATV25	ATBELL	PNSUC	DTDET	BEL103
	0A	—	—	—	—	—	—	—	CRCS
Control	09	NV25	CC	DTMF	ORG	LL	DATA	—	SLEEP
	08	ASYNC	TPDM	—	DDIS	TRFZ	—	RTRN	RTS
	07	RDLE	RDL	L2ACT	—	L3ACT	RB	RA	ABORT
	06	BRKS	EXOS	PARSL		PEN	STB	WDSZ	
	05	ADPCM	DTMFE	FRZSL	TXSQ	TONDT/ CEQE	DCDSEE/ RCEQ	TXVOC	RXVOC
	04	EQRES	SWRES	SDCDE	SCDE	EQFZ	IFIX	AGCFZ	CRFZ
	03	NRZIE	HDLC	SPLIT	SHTR	ARC	SDIS	GTE	—
	02	—	—	—	QDCD		QCD		—
Receive Data Buffer	01	—	—	—	—	—	—	—	RXP
	00	RECEIVE DATA BUFFER (RBUFFER)							

NOTE: — In the "Bit" columns indicates reserved for modem use only.

Figure 4a. RC96V24DP and RC96V26DP Interface Memory Map

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0
Interrupt Handling	1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
	1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
RAM Access, Control, and Status	1D	XACC	—	—	—	IOX	XCRD	XWT	XCR
	1C	X RAM ADDRESS (XADD)							
	1B	YACC	—	—	—	—	YCRD	YWT	YCR
	1A	Y RAM ADDRESS (YADD)							
	19	X RAM DATA MSB (XDAM)							
	18	X RAM DATA LSB (XDAL)							
	17	Y RAM DATA MSB (YDAM)							
	16	Y RAM DATA LSB (YDAL)							
—	15	—	—	—	—	—	—	—	—
—	14	—	—	—	—	—	—	—	—
Control	13	TLVL				VOL		TXCLK	
	12	CONFIGURATION (CONF)							
Transmit Data Buffer	11	—	—	—	—	—	—	—	TXP
	10	TRANSMIT DATA BUFFER (TBUFFER)							
Status	0F	RLSD	FED	CTS	DSR	RI	TM	SYNCD	FLAGS
	0E	RTDET	BRKD	PE	FE	OE	SPEED		
	0D	—	PNDET	S1DET	SCR1	U1DET	SADET	—	SP03
	0C	EDET	—	—	—	DTDIG			
	0B	TONEA	TONEB	TONEC	ATV25	ATBELL	PNSUC	DTDET	BEL103
	0A	—	—	—	PRDET	—	—	—	CRCS
Control	09	NV25	CC	DTMF	ORG	LL	DATA	—	SLEEP
	08	ASYNC	TPDM	CRR17	DDIS	TRFZ	PJDIS	RTRN	RTS
	07	RDLE	RDL	L2ACT	—	L3ACT	RB	RA	ABORT
	06	BRKS	EXOS	PARSL		PEN	STB	WDSZ	
	05	ADPCM	DTMFE	FRZSL	TXSQ	TONDT/ CEQE	DCDSEE/ RCEQ	TXVOC	RXVOC
	04	EQRES	SWRES	SDCDE	SCDE	EQFZ	IFIX	AGCFZ	CRFZ
	03	NRZIE	HDLC	SPLIT	SHTR	ARC	SDIS	GTE	BSYNC
	02	—		—	QDCD		QCD		—
Receive Data Buffer	01	—	—	—	—	—	—	—	RXP
	00	RECEIVE DATA BUFFER (RBUFFER)							

NOTE: — In the "Bit" columns indicates reserved for modem use only.

Figure 4b. RC14V24DP and RC14V26DP Interface Memory Map

Table 11. Interface Memory Bit Functions

Mnemonic	Memory Location	Name/Description
ABORT	07:0	**HDLC Abort.** Controls sending of continuous mark in HDLC mode.
ADPCM	05:7	**Adaptive Differential Pulse Code Modulation.** Enables voice compression when RXVOC=1. Enables voice decompression when TXVOC=1. Available only in Tone mode.
AGCFZ	04:1	**AGC Freeze.** Inhibits updating of the receiver AGC.
ARC	03:3	**Automatic Rate Change Enable.** For V.22 bis, enables automatic on-line rate change sequence. For V.17, enables automatic on-line speed change sequence.
ASYNC	08:7	**Asynchronous/Synchronous.** Selects asynchronous or synchronous data mode.
ATBELL	0B:3	**Bell Answer Tone Detected.** Reports detection status of 2225 Hz answer tone.
ATV25	0B:4	**V25 Answer Tone Detected.** Reports detection status of 2100 Hz answer tone.
BEL103	0B:0	**Bell 103 Mark Frequency Detected.** Reports detection status of 1270 Hz Bell 103 mark.
BRKD	0E:6	**Break Detected.** Reports receipt status of continuous space.
BRKS	06:7	**Break Sequence.** Controls sending of continuous space in parallel asynchronous mode.
BSYNC	03:0	**Bisync Mode.** Selects Binary Synchronous Communication (Bisync) Protocol Support.
CC	09:6	**Controlled Carrier.** Selects controlled or constant carrier mode.
CEQE	05:3	**Compromise Equalizer Enable.** Enables the transmit passband digital compromise equalizer.
CONF	12:0-7	**Modem Configuration Select.** Selects the modem operating mode.
CRCS	0A:0	**CRC Sending.** Reports the sending status of the CRC (2 bytes) in HDLC mode.
CRFZ	04:0	**Carrier Recovery Freeze.** Disables update of the receiver's carrier recovery phase lock loop.
CRR17	08:5	**V.17 Carrier Option Select.** Selects V.17 1700 Hz carrier mode.
CTS	0F:5	**Clear to Send.** Reports that the training sequence has been completed.
DATA	09:2	**Data Mode.** Selects idle or data mode.
DCDSEE	05:2	**Decoder Speech Enhancement Enable.** Enhances voice quality with 2-bit encoding. (ADPCM only.)
DDIS	08:4	**Descrambler Disable.** Disables the receiver's descrambler circuit.
DSR	0F:4	**Data Set Ready.** Reports the data transfer state.
DTDET	0B:1	**DTMF Digit Detected.** Reports that a valid DTMF digit has been detected.
DTDIG	0C:0-3	**Detected DTMF Digit.** Contains the hexadecimal code of the detected DTMF digit.
DTMF	09:5	**DTMF Dial Select.** Selects either DTMF or pulse dialing in the dial mode.
DTMFE	05:6	**DTMF Detector Enable.** When control bit DTMFE is set, the DTMF detector is enabled in the tone configuration. When DTMFE is reset, the DTMF detector is disabled.
EDET	0C:7	**Early DTMF Detect.** Reports detection of the high group frequency of the DTMF tone pair.
EQFZ	04:3	**Equalizer Freeze.** Inhibits the update of the receiver's adaptive equalizer taps.
EQRES	04:7	**Equalizer Reset.** Resets the receiver adaptive equalizer taps to zero.
EXOS	06:6	**Extended Overspeed.** Selects extended overspeed mode in asynchronous mode.
FE	0E:4	**Framing Error.** Reports framing error detection or detection of an ABORT sequence.
FED	0F:6	**Fast Energy Detected.** Reports energy above the turn-on threshold is being detected.
FLAGS	0F:0	**Flag Sequence.** Reports transmission status of the Flag sequence in HDLC mode, or transmission of a constant mark in parallel asynchronous mode.

Table 11. Interface Memory Bit Functions (Cont'd)

Mnemonic	Memory Location	Name/Description
FRZSL	05:5	**Freeze Slew Rate.** When control bit FRZSL is set, the modem will not change the slew rate. When FRZSL is reset, the AGC slew rate is controlled by the modem. (ADPCM only.)
GTE	03:1	**Guard Tone Enable.** Enables transmission of the 1800 Hz guard tone (CCITT configuration only).
HDLC	03:6	**High Level Data Link Control.** Enables HDLC protocol support in parallel data mode.
IFIX	04:2	**Eye Fix.** Forces EYEX and EYEY serial data to be rotated equalizer output.
IOX	1D:3	**I/O Register Select.** Specifies that the X RAM ADDRESS (XADD) is an internal I/O register address.
L2ACT	07:5	**Loop 2 (Local Digital Loopback) Activate.** Selects connection of the receiver's digital output internally to the transmitter's digital input (locally activated digital loopback). Used as a coder to decoder loop in Tone mode with ADPCM.
L3ACT	07:3	**Loop 3 (Local Analog Loopback) Activate.** Selects connection of the transmitter's analog output internally to the receiver's analog input (local analog loopback).
LL	09:3	**Leased Line.** Selects leased line data mode or handshake mode.
NCIA	1F:6	**NEWC Interrupt Active.** Reports that the cause of an interrupt request was completion of a configuration change. (See NEWC and NCIE.)
NCIE	1F:2	**NEWC Interrupt Enable.** Enables the assertion of $\overline{IRQ}$ and the setting of the NCIA bit.
NEWC	1F:0	**New Configuration.** Initiates a new configuration; cleared by the modem upon completion of configuration change. This bit can cause IRQ to be asserted. (See NCIE and NCIA.)
NEWS	1F:3	**New Status.** Reports the detection of a change in selected status bits. This bit can cause $\overline{IRQ}$ to be asserted. (See NSIE and NSIA.)
NRZIE	03:7	**Non-Return to Zero Inverted Enable.** When NRZIE is set, NRZI coding is applied to data before scrambling, and NRZI decoding is performed on data after descrambling. (HDLC mode only.)
NSIA	1F:7	**NEWS Interrupt Active.** Reports that the cause of an interrupt request was a status bit change. (See NEWS and NSIE.)
NSIE	1F:4	**NEWS Interrupt Enable.** Enables the assertion of $\overline{IRQ}$ and the setting of the NSIA bit. (See NEWS.)
NV25	09:7	**Disable V.25 Answer Sequence (Data Modes), Disable Echo Suppressor Tone (Fax Modes).** Disables the transmitting of the 2100 Hz CCITT answer tone when a handshake sequence is initiated in a data mode or disables sending of the echo suppressor tone in a fax mode.
OE	0E:3	**Overrun Error.** Reports overrun status of the Receiver Data Buffer (RBUFFER).
ORG	09:4	**Originate.** Selects originate or answer mode.
PARSL	06:4,5	**Parity Select.** Selects stuff, space, even, or odd parity in the asynchronous parallel data mode.
PE	0E:5	**Parity Error.** Reports parity error status or bad CRC.
PEN	06:3	**Parity Enable.** Enables generation/checking of parity in asynchronous parallel data mode.
PJDIS	08:2	**Phase Jitter Disable.** Disables phase jitter tracker in V.17 mode.
PNDET	0D:6	**PN Sequence Detected.** Status bit PNDET is set to a 1 when the PN Sequence is first detected. PNDET is reset to a 0 upon loss of energy.
PNSUC	0B:2	**PN Success.** Indicates that the receiver has detected the PN portion of the training sequence.
PRDET	0A:4	**Rate Sequence Detection.** When set to 1, the rate sequence has been detected if configured as V.17 receiver.

Table 11. Interface Memory Bit Functions (Cont'd)

Mnemonic	Memory Location	Name/Description
QCD	02:1-2	**Quantizer Select for Coder.** (ADPCM only.) QCD selects coder quantization as follows: QCD 2 1 — Selection 0 0 — 4-bit quantizer 0 1 — 3-bit quantizer 1 0 — 2-bit quantizer 1 1 — Reserved
QDCD	02:3-4	**Quantizer Select for Decoder.** (ADPCM only.) QDCD selects decoder quantization as follows: QDCD 4 3 — Selection 0 0 — 4-bit quantizer 0 1 — 3-bit quantizer 1 0 — 2-bit quantizer 1 1 — Reserved
RA	07:1	**Relay A Activate.** Activates the $\overline{\text{RADRV}}$ output.
RB	07:2	**Relay B Activate.** Activates the $\overline{\text{RBDVR}}$ output.
RBUFFER	00:0-7 01:0-7	**Receive Data/Voice Buffer.** Contains the received byte of data (2 bytes for ADPCM).
RCEQ	05:2	**Receiver Compromise Equalizer Enable.** Controls insertion of the receive passband digital compromise equalizer into the receive path. (Not used in Tone mode.)
RDBF	1E:0	**Receiver Data Buffer Full.** Reports the status (full or not full) of the Receiver Data Buffer (RBUFFER). (See RDBIE and RDBIA.)
RDBIA	1E:6	**Receiver Data Buffer Interrupt Active.** Reports that the cause of an interrupt request is the Receiver Data Buffer (RBUFFER) full. (See RDBF and RDBIE.)
RDBIE	1E:2	**Receiver Data Buffer Interrupt Enable.** Enables the assertion of $\overline{\text{IRQ}}$ and the setting of the RDBIA bit when RBUFFER is full. (See RDBF and RDBIA.)
RDL	07:6	**Remote Digital Loopback Request.** Initiates a request for the remote modem to go into digital loopback.
RDLE	07:7	**Remote Digital Loopback Response Enable.** Enables the modem to respond to the remote modem's digital loopback request.
RI	0F:3	**Ring Indicator.** Reports detection status of a valid ringing signal.
RLSD	0F:7	**Received Line Signal Detector.** Reports detection status of the carrier and the receipt of valid data.
RTDET	0E:7	**Retrain Detected.** Reports detection status of a retrain request sequence.
RTRN	08:1	**Retrain.** Controls sending of the retrain request or automatic rate change to the remote modem.
RTS	08:0	**Request to Send.** Requests the transmitter to send data.
RXP	01:0	**Received Parity Bit.** This status bit is only valid when parity is enabled and word size is set for 8 bits per character. In this case, the parity bit received (or ninth data bit) will be available at this location.
RXVOC	05:0	**Receiver Voice.** Enables reception of voice samples.
S1DET	0D:5	**S1 Sequence Detected.** Reports detection status of the S1 sequence.
SADET	0D:2	**Scrambled Alternating Ones Sequence Detected.** Reports detection status of the Scrambled Alternating Ones sequence.
SCDE	04:4	**Silence Coder Enable.** When control bit SCDE is set and the ADPCM coder is enabled (ADPCM=1, TXVOC=0, RXVOC=1), the modem performs silence detection and deletion. When SCDE is reset, the modem does not perform silence detection and deletion. (ADPCM only.)

Table 11. Interface Memory Bit Functions (Cont'd)

Mnemonic	Memory Location	Name/Description
SCR1	0D:4	**Scrambled Ones Sequence Detected.** Reports detection status of Scrambled Ones sequence.
SDCDE	04:5	**Silence Decoder Enable.** When control bit SDCDE is set and the ADPCM decoder is enabled (ADPCM=1, TXVOC=1, RXVOC=0), the modem performs silence interpolation. When SDCDE is reset, the modem does not perform silence interpolation. Silence must have been previously deleted during coding. (ADPCM only.)
SDIS	03:2	**Scrambler Disable.** Disables the transmitter scrambler.
SHTR	03:4	**Short Train Enable.** Enables short train sequence in V.27 ter, V.29, and V.17.
SLEEP	09:0	**Sleep Mode.** Controls entry into the SLEEP mode. The modem requires a pulse on the $\overline{\text{RESET}}$ pin or a dummy write to interface memory to return to normal operation.
SP03	0D:0	**Speed Indicator MSB.** Most significant bit of Speed Indicator.
SPEED	0E:0-2	**Speed Indication.** Reports the data rate at the completion of a connection.
SPLIT	03:5	**Extended Overspeed TX/RX Split.** Limits transmit data to the basic overspeed rate.
STB	06:2	**Stop Bit Number.** Selects the number of stop bits in asynchronous mode.
SWRES	04:6	**Software Reset.** Causes the modem to reinitialize to its power turn-on state.
SYNCD	0F:1	**Sync Pattern Detected.** Status bit SYNCD is a 1 when SDLC/HDLC flags (7E pattern) are being detected. SYNCD is a 0 when the 7E pattern is not being detected. This bit is valid only in SDLC/HDLC mode.
TBUFFER	10:0-7 11:0-7	**Transmitter Data/Voice Buffer.** Contains the byte to be transmitted in the parallel mode (2 bytes for ADPCM).
TDBE	1E:3	**Transmitter Data Buffer Empty.** Reports the status (empty or not empty) of the Transmit Data Buffer (TBUFFER). (See TDBIE and TDBIA.)
TDBIA	1E:7	**Transmitter Data Buffer Interrupt Active.** Reports that the cause of an interrupt request is the Transmit Data Buffer (TBUFFER) empty. (See TDBE and TDBIE.)
TDBIE	1E:5	**Transmitter Data Buffer Interrupt Enable.** Enables assertion of $\overline{\text{IRQ}}$ and the setting of the TDBIA bit when the TBUFFER is empty. (See TDBE and TDBIA.)
TLVL	13:4-7	**Transmit Level Attenuation Select.** Selects the transmitter analog output level attenuation in 1 dB steps. The host can fine tune the transmit level to a value lying within a 1 dB step in DSP RAM.
TM	0F:2	**Test Mode.** Reports active status of the selected test mode.
TONDT	05:3	**Tone Detector Select.** Selects number of tone detect filters as follows (Tone mode only): **TONDT** — **Selection** 1 — All 3 tone detectors 0 — One tone detector (TONEA)
TONEA	0B:7	**Tone Filter A Energy Detected.** Reports status of energy above the threshold detection by the Call Progress Monitor filter in the Dial Configuration or 1300 Hz FSK tone energy detection by the Tone A bandpass filter in the Tone Detector configuration.
TONEB	0B:6	**Tone Filter B Energy Detected.** Reports status of 390 Hz FSK tone energy detection by the Tone B bandpass filter in the Tone Detector configuration.
TONEC	0B:5	**Tone Filter C Energy Detected.** Reports status of 1650 Hz or 980 Hz (selected by the ORG bit) FSK tone energy detection by the Tone C bandpass filter in the Tone Detector configuration.
TPDM	08:6	**Transmitter Parallel Data Mode.** Selects transmitter parallel or serial mode.
TRFZ	08:3	**Timing Recovery Freeze.** Inhibits the update of the receiver's timing recovery algorithm.
TXCLK	13:0,1	**Transmit Clock Select.** Selects the transmitter data clock (internal, disable, slave, or external).

Table 11. Interface Memory Bit Functions (Cont'd)

Mnemonic	Memory Location	Name/Description
TXP	11:0	**Transmit Parity Bit (or 9th Data Bit).** Control bit TXP contains the stuffed parity bit (or ninth data bit) for transmission when parity is enabled, stuff parity is selected, and word size is set for 8 bits per character. The host must load the stuffed parity bit into TXP before loading the other 8 bits of data in TBUFFER.
TXSQ	05:4	**Transmitter Squelch.** Disables transmission of energy.
TXVOC	05:1	**Transmit Voice.** Enables the sending of voice samples.
U1DET	0D:3	**Unscrambled Ones Detected.** Reports detection status of the Unscrambled Ones sequence.
VOL	13:2-3	**Volume Control.** Two-bit encoded speaker volume selects volume off or one of three volume on levels.
WDSZ	06:0,1	**Data Word Size.** Selects the number of data bits per character in asynchronous mode (5, 6, 7, or 8).
XACC	1D:7	**X RAM Access Enable.** Controls DSP access of the X RAM associated with the address in XADD and the XCR bit. XWT determines if a read or write is performed.
XADD	1C:0-7	**X RAM Address.** Contains the X RAM address used to access the DSP's X Data RAM or X Coefficient RAM (selected by XCR) via the X RAM Data LSB and MSB registers). (See Tables 12a and 12b.)
XCR	1D:0	**X Coefficient RAM Select.** Controls XADD access to the DSP's X Coefficient RAM or the X Data RAM.
XCRD	1D:2	**X RAM Continuous Read.** Enables read of X RAM every sample from the location addressed by XADD independent of the XACC and XWT bits.
XDAL	18:0-7	**X RAM Data LSB.** The least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XDAM	19:0-7	**X RAM Data MSB.** The most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XWT	1D:1	**X RAM Write.** Controls the reading of data from, or the writing of data to, the X RAM Data registers (18 and 19) using the X RAM location addressed by XADD and XCR.
YACC	1B:7	**Y RAM Access Enable.** Controls DSP access of the Y RAM associated with the address in YADD and the YCR bit. YWT determines if a read or write is performed.
YADD	1A:0-7	**Y RAM Address.** Contains the Y RAM address used to access the DSP's Y Data RAM or Y Coefficient RAM (selected by YCR) via the Y RAM Data LSB and MSB registers. (See Tables 12a and 12b.)
YCR	1B:0	**Y Coefficient RAM Select.** Controls YADD access to the DSP's Y Coefficient RAM or the Y Data RAM.
YCRD	1B:2	**Y RAM Continuous Read.** Enables read of Y RAM every sample from the location addressed by YADD independent of the YACC and YWT bits.
YDAL	16:0-7	**Y RAM Data LSB.** The least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YDAM	17:0-7	**Y RAM Data MSB.** The most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YWT	1B:1	**Y RAM Write.** Controls the reading of data from, or the writing of data to, the Y RAM Data registers (16 and 17) using the Y RAM location addressed by YADD and YCR.

DSP RAM ACCESS

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in modem interface memory RAM Address registers (i. e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i. e., XCR and YCR) determine the DSP RAM addresses for data access.

HOST PROGRAMMABLE DATA

The parameters available in DSP RAM are listed in Table 12a for the RC96V24DP and RC96V26DP, and in Table 12b for the RC14V24DP and RC14V26DP, along with the X RAM or Y RAM address and corresponding XCR or YCR bit value. The scaling for the host programmable data is described in the RC9624DP, RC96V24DP, and RC14V24DP Modem Designer's Guide (Order No. 822 Rev. 2).

Table 12a. RC96V24DP and RC96V26DP DSP RAM Parameters

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	0-1E		Adaptive Equalizer Coefficients, Real
	1	0	–	First Coefficient, Real (1) (Data/ Fax)
	1	10	–	Last Coefficient, Real (17) (Data)
	1	1E	–	Last Coefficient, Real (31) (Fax)
2	1		0-1E	Adaptive Equalizer Coefficients, Imag.
	1	–	0	First Coefficient, Imag. (1) (Data/ Fax)
	1	–	10	Last Coefficient, Imag. (17) (Data)
	1	–	1E	Last Coefficient, Imag. (31) (Fax)
3	0	49	–	Rotated Error, Real (RERRX)
4	0	–	49	Rotated Error, Imaginary (RERRY)
5	0	3F	–	Max AGC Gain Word (MAXG)
6	0	71	–	Pulse Dial Interdigit Time (INTERP)
7	0	7C	–	Tone Dial Interdigit Time (INTERT)
8	0	72	–	Pulse Dial Relay Make Time (PONTME)
9	0	7D	–	Pulse Dial Relay Break Time (POFTME)
10	0	7E	–	DTMF Duration (TONTME)
11	0	6C	–	Tone 1 Angle Increment Per Sample (TXDPHI1)
12	0	6D	–	Tone 2 Angle Increment Per Sample (TXDPHI2)
13	0	6E	–	Tone 1 Amplitude (TXAMP1)
14	0	6F	–	Tone 2 Amplitude (TXAMP2)
15	0	73	–	Max Samples Per Ring Frequency Period (RDMAXP)
16	0	74	–	Min Samples Per Ring Frequency Period (RDMINP)
17	0	5E	–	Real Part of Error (ERRX)
18	0	–	5E	Imaginary Part of Error (ERRY)
19	0	–	3D	Rotation Angle for Carrier Recovery (THETA)
20	0	59	–	Rotated Equalizer Output, Real (WREQX)
21	0	–	59	Rotated Equalizer Output, Imaginary (WREQY)
22	0	3C	–	Lower Part of Phase Error (LPER)
23	0	–	3C	Upper Part of Phase Error (UPER)
24	1	3F	–	Upper Part of AGC Gain Word (UGAIN)
25	1	3E	–	Lower Part of AGC Gain Word (LGAIN)
26	1	2E	–	Average Power (AVGPWR)
27	1	2D	–	Phase Error (PHERR)
28	1	2F	–	Tone Power (TONEA) [TPWRA]

MODEM INTERFACE CIRCUIT

The recommended modem interface circuit is shown in Figure 5.

Table 12a. RC96V24DP/RC96V26DP DSP RAM Parameters (Cntd)

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
29	1	30	–	Tone Power (ATBELL, BEL103, or TONEB) [TPWRB]
30	1	31	–	Tone Power (TONEC, ATV25) [TPWRC]
31	1	36	–	Tone Detect Threshold for TONEA (THDA)
32	1	37	–	Tone Detect Threshold for ATBELL, BEL103, or TONEB (THDB)
33	1	38	–	Tone Detect Threshold for TONEC or ATV25 (THDC)
34	1	–	6C	Biquad 1 Coefficient a0 (CBQ10)
	1	–	6D	Biquad 1 Coefficient a1 (CBQ11)
	1	–	6E	Biquad 1 Coefficient a2 (CBQ12)
	1	–	6F	Biquad 1 Coefficient b1 (CBQ13)
	1	–	70	Biquad 1 Coefficient b2 (CBQ14)
	1	–	71–75	Biquad 2 Coefficients a0 – b2
	1	–	76–7A	Biquad 3 Coefficients a0 – b2
	1	–	7B–7F	Biquad 4 Coefficients a0 – b2
	1	–	62–66	Biquad 5 Coefficients a0 – b2
	1	–	67–6B	Biquad 6 Coefficients a0 – b2
35	0	32	–	Turn-on Threshold (EONTHD)
36	1	35	–	Turn-off Threshold (FEOFTAD)
37	1	–	21	RLSD Turn-off Time (FRZLEN)
38	0	70	–	Transmit Level Output Attenuation (TSCALE)
39	1	52	–	Eye Quality Monitor (EQM) [EQMOUT]
40	1	–	51	V.26 Synchronizing Sequence, Segment 1 Duration (L26UI)
41	1	–	50	V.26 Synchronizing Sequence, Segment 2 Duration (SCRBLN)
42	1	–	41	V.26 Turn-off Sequence Duration (TOFFLN)
43	1	–	52	V.26 RLSD Off-to-On Time (L26TRN)
45	0	36	–	Reconstructed Speech Samples (DCDOUTC)
46	1	–	42	Speech Sample Scaling Parameter (ADCS)
47	1	–	43	Host Speech Sample Scaling Parameter (PEMPCF)
48	0	43	–	Host Speech Sample (ADC16)
50	0	1	6A	White Noise Output Scaling Parameter (RANOISE)
51	1	76	–	Minimum Silence Magnitude Threshold (ETHRESH)
52	1	–	6B	Detecting Silence in Speech Parameter (ALPHA)
53	0	1	66	Detecting Speech in Silence Parameter (BETA)
54	0	–	67	Minimum Silence Magnitude Adaptation Parameter (SIGMA)
55	0	45	–	ADPCM Max. Gain (DBTHR)
56	0	–	4D	DAC Output Word (WDAC)
57	1	39	–	AGC Slewrate (SLEWRT)

*XCR if an XRAM address is listed; YCR if a YRAM address is listed.

Table 12b. RC14V24DP and RC14V26DP DSP RAM Parameters

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	7C-AB		Adaptive Equalizer Coefficients, Real
	1	7C	–	First Coefficient, Real (1) (Data/ Fax)
	1	8D	–	Last Coefficient, Real (17) (Data)
	1	AB	–	Last Coefficient, Real (31) (Fax)
2	1		7C-AB	Adaptive Equalizer Coefficients, Imag.
	1	–	7C	First Coefficient, Imag. (1) (Data/ Fax)
	1	–	8D	Last Coefficient, Imag. (17) (Data)
	1	–	AB	Last Coefficient, Imag. (31) (Fax)
3	0	3C	–	Rotated Error, Real (RERRX)
4	0	–	3C	Rotated Error, Imaginary (RERRY)
5	0	3F	–	Max AGC Gain Word (MAXG)
6	0	71	–	Pulse Dial Interdigit Time (INTERP)
7	1	6F	–	Tone Dial Interdigit Time (INTERT)
8	0	72	–	Pulse Dial Relay Make Time (PONTME)
9	1	70	–	Pulse Dial Relay Break Time (POFTME)
10	1	71	–	DTMF Duration (TONTME)
11	0	6C	–	Tone 1 Angle Increment Per Sample (TXDPHI1)
12	0	6D	–	Tone 2 Angle Increment Per Sample (TXDPHI2)
13	0	6E	–	Tone 1 Amplitude (TXAMP1)
14	0	6F	–	Tone 2 Amplitude (TXAMP2)
15	0	73	–	Max Samples Per Ring Frequency Period (RDMAXP)
16	0	74	–	Min Samples Per Ring Frequency Period (RDMINP)
19	0	–	3D	Rotation Angle for Carrier Recovery (THETA)
20	0	3E	–	Rotated Equalizer Output, Real (WREQX)
21	0	–	3E	Rotated Equalizer Output, Imaginary (WREQY)
22	0	3C	–	Lower Part of Phase Error (LPER)
23	0	–	3C	Upper Part of Phase Error (UPER)
24	1	3F	–	Upper Part of AGC Gain Word (UGAIN)
25	1	3E	–	Lower Part of AGC Gain Word (LGAIN)
26	1	2E	–	Average Power (AVGPWR)
27	1	2D	–	Phase Error (PHERR)
28	1	2F	–	Tone Power (TONEA) [TPWRA]

Table 12b. RC14V24DP/RC14V26DP DSP RAM Parameters (Cntd)

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
29	1	30	–	Tone Power (ATBELL, BEL103, or TONEB) [TPWRB]
30	1	31	–	Tone Power (TONEC, ATV25) [TPWRC]
31	1	36	–	Tone Detect Threshold for TONEA (THDA)
32	1	37	–	Tone Detect Threshold for ATBELL, BEL103, or TONEB (THDB)
33	1	38	–	Tone Detect Threshold for TONEC or ATV25 (THDC)
34	1	–	6C	Biquad 1 Coefficient a0 (CBQ10)
	1	–	6D	Biquad 1 Coefficient a1 (CBQ11)
	1	–	6E	Biquad 1 Coefficient a2 (CBQ12)
	1	–	6F	Biquad 1 Coefficient b1 (CBQ13)
	1	–	70	Biquad 1 Coefficient b2 (CBQ14)
	1	–	71–75	Biquad 2 Coefficients a0 – b2
	1	–	76–7A	Biquad 3 Coefficients a0 – b2
	1	67-6B	–	Biquad 4 Coefficients a0 – b2
	1	–	62–66	Biquad 5 Coefficients a0 – b2
	1	–	67–6B	Biquad 6 Coefficients a0 – b2
35	0	32	–	Turn-on Threshold (EONTHD)
36	1	35	–	Turn-off Threshold (FEOFTAD)
37	1	–	21	RLSD Turn-off Time (FRZLEN)
38	0	70	–	Transmit Level Output Attenuation (TSCALE)
39	1	52	–	Eye Quality Monitor (EQM) [EQMOUT]
40	1	–	51	V.26 Synchronizing Sequence, Segment 1 Duration (L26UI)
41	1	–	50	V.26 Synchronizing Sequence, Segment 2 Duration (SCRBLN)
42	1	–	41	V.26 Turn-off Sequence Duration (TOFFLN)
43	1	–	52	V.26 RLSD Off-to-On Time (L26TRN)
45	0	36	–	Reconstructed Speech Samples (DCDOUTC)
46	1	–	42	Speech Sample Scaling Parameter (ADCS)
47	1	–	43	Host Speech Sample Scaling Parameter (PEMPCF)
48	0	42	–	Host Speech Sample (ADC16)
50	0	–	8A	White Noise Output Scaling Parameter (RANOISE)
51	1	96	–	Minimum Silence Magnitude Threshold (ETHRESH)
52	1	–	8B	Detecting Silence in Speech Parameter (ALPHA)
53	0	–	86	Detecting Speech in Silence Parameter (BETA)
54	0	–	87	Minimum Silence Magnitude Adaptation Parameter (SIGMA)
55	0	45	–	ADPCM Max. Gain (DBTHR)
56	0	–	4D	DAC Output Word (WDAC)
57	1	39	–	AGC Slewrate (SLEWRT)

*XCR if an XRAM address is listed; YCR if a YRAM address is listed.

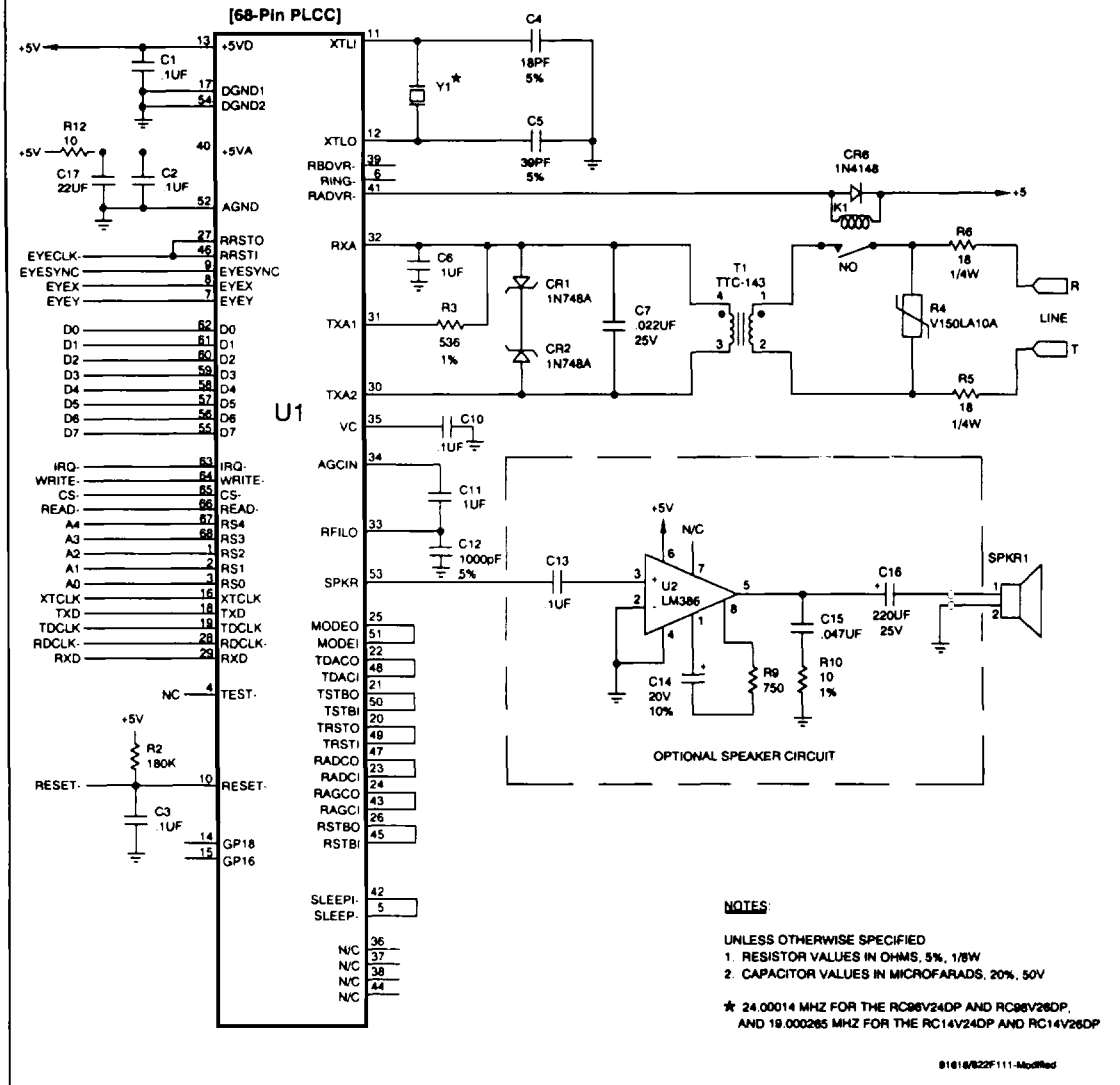


Figure 5. Typical Modem Interface Circuit

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