

MH25608TNA-85L, -10L, -12L, -15L/ MH25608TNA-85H, -10H, -12H, -15H

2097152-BIT(262144-WORD BY 8-BIT)CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

The MH25608TNA is a 2097152 bits CMOS static RAM module organized as 262144-words by 8-bits. It consists of eight industry standard 32K x 8 static RAMs and one decoder.

The stand-by current is low enough for a battery backup application. It is mounted a flat package on a 32-pin dual in line package.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH25608TNA-85L	85ns	80 mA	400 μ A
MH25608TNA-10L	100ns		
MH25608TNA-12L	120ns		
MH25608TNA-15L	150ns		
MH25608TNA-85H	85ns	180 μ A	
MH25608TNA-10H	100ns		
MH25608TNA-12H	120ns		
MH25608TNA-15H	150ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by \bar{S}
- \bar{OE} Prevents Data Contention in the I/O Bus
- Common Data I/O

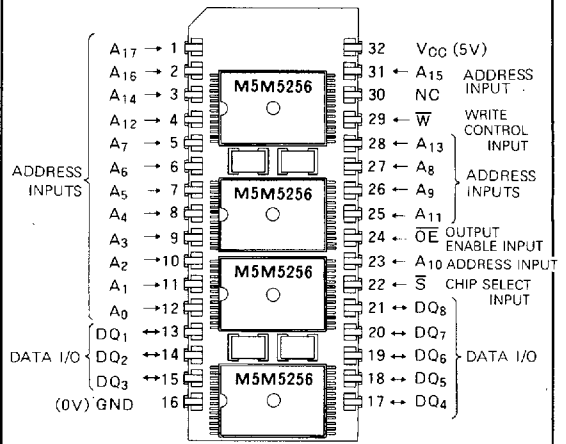
APPLICATION

Small Capacity Memory Units.

FUNCTION

The operation mode of the MH25608TNA is determined by a combination of the device control inputs \bar{S} , \bar{W} and \bar{OE} . Each mode is summarized in the function table. (see next page)

PIN CONFIGURATION (TOP VIEW)



Outline 32N1A

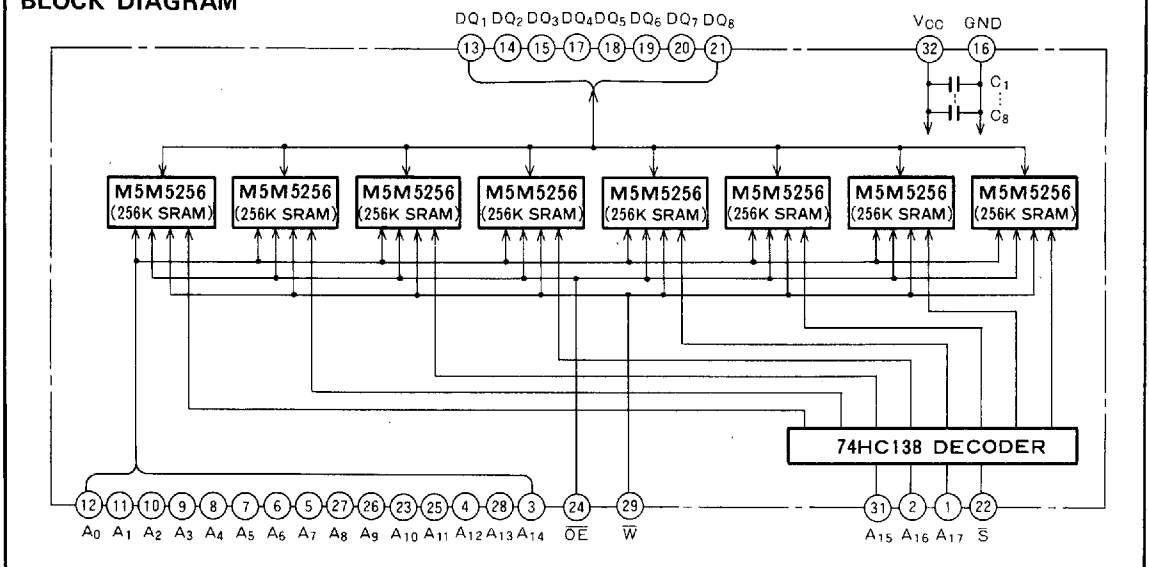
NC: NO CONNECTION

A write cycle is executed whenever the low level \bar{W} overlaps with the low level \bar{S} . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \bar{W} , \bar{S} , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable \bar{OE} directly controls the output stage. Setting the \bar{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \bar{W} at a high level and \bar{OE} at a low level while \bar{S} are in an active state.

When setting \bar{S} at a high level, the chip is in a non-

BLOCK DIAGRAM



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selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \bar{S} . The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

\bar{S}	\bar{W}	\bar{OE}	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	Low input voltage	-0.3		0.8	V
V_{IH}	High input voltage	3.2		$V_{CC}+0.3$	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3 ~ 7	V
V_I	Input voltage		-0.3 ~ $V_{CC}+0.3$	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	700	mW
T_{opr}	Operating temperature		0 ~ 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-40 ~ 100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		3.2		$V_{CC}+0.3$	V
V_{IL}	Low input voltage		-0.3		0.8	V
V_{OH}	High output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_I	Input current	$V_I = 0 \sim V_{CC}$			± 1	μA
I_{OZH}	High level output current in off-state	$\bar{S} = V_{IH}$ or $\bar{OE} = V_{IH}$			1	μA
I_{OZL}	Low level output current in off-state	$V_I/O = 0 \sim V_{CC}$			-1	μA
I_{CC1}	Active supply current (AC. MOS level)	$\bar{S} < 0.2, \bar{W} > V_{CC} - 0.3$ output open other input < 0.2 or $> V_{CC} - 0.3$ Min. cycle		35	75	mA
I_{CC2}	Active supply current (AC. TTL level)	$\bar{S} = V_{IL}, \bar{W} = V_{IH}$ output open other input $= V_{IL}$ or V_{IH} Min. cycle		40	80	mA
I_{CC3}	Stand-by supply current	$\bar{S} \geq V_{CC} - 0.2\text{V}$, A_{15} and A_{16} TNA-L and $A_{17} \leq 0.2$ or $\geq V_{CC} - 0.2$ TNA-H Other inputs $= 0 \sim V_{CC}$			400 180	μA
I_{CC4}	Stand-by supply current	$\bar{S} = V_{IH}$, Other inputs $= 0 \sim V_{CC}$			12	mA
C_i	Input capacitance ($T_a = 25^\circ\text{C}$)	$V_I = \text{GND}$, $V_i = 25\text{mVrms}$, $f = 1\text{MHz}$			60	pF
C_o	Output capacitance ($T_a = 25^\circ\text{C}$)	$V_O = \text{GND}$, $V_O = 25\text{mVrms}$, $f = 1\text{MHz}$			60	pF

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
2: Typical value is $V_{CC} = 5V$, $T_a = 25^\circ\text{C}$

**MH25608TNA-85L,-10L,-12L,-15L/
MH25608TNA-85H,-10H,-12H,-15H**

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SWITCHING CHARACTERISTICS ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, unless otherwise noted)

Read cycle

Symbol	Parameter	Limit												Unit
		MH25608TNA-85L MH25608TNA-85H			MH25608TNA-10L MH25608TNA-10H			MH25608TNA-12L MH25608TNA-12H			MH25608TNA-15L MH25608TNA-15H			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			120			150			ns
$t_a(A)$	Address access time			85			100			120			150	ns
$t_a(S)$	Chip select access time			85			100			120			150	ns
$t_a(OE)$	Output enable access time			45			50			60			75	ns
$t_{dis}(S)$	Output disable time after \bar{S} high			30			35			40			45	ns
$t_{dis}(OE)$	Output disable time after \bar{OE} high			30			35			40			45	ns
$t_{en}(S)$	Output enable time after \bar{S} low	10			10			10			10			ns
$t_{en}(OE)$	Output enable time after \bar{OE} low	10			10			10			10			ns
$t_v(A)$	Data valid time after address change	20			20			20			20			ns

TIMING REQUIREMENTS ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, unless otherwise noted)

Write cycle

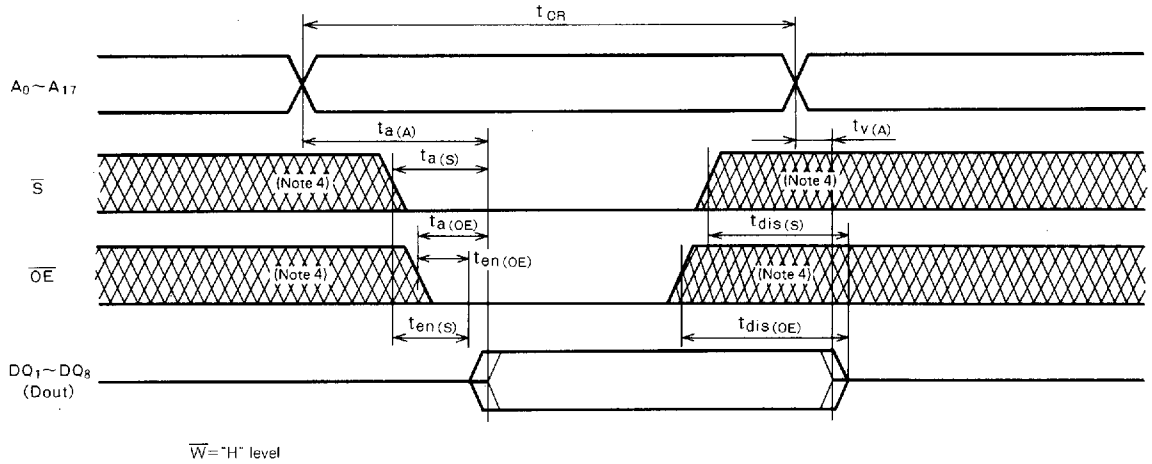
Symbol	Parameter	Limit												Unit
		MH25608TNA-85L MH25608TNA-85H			MH25608TNA-10L MH25608TNA-10H			MH25608TNA-12L MH25608TNA-12H			MH25608TNA-15L MH25608TNA-15H			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			120			150			ns
$t_w(W)$	Write pulse width	60			60			70			80			ns
$t_{su}(A)$	Address set up time	0			0			0			0			ns
$t_{su}(A-\bar{W}H)$	Address set up time with respect to \bar{W} high	75			80			85			90			ns
$t_{su}(S)$	Chip select set up time	75			80			85			90			ns
$t_{su}(D)$	Data set up time	35			35			40			50			ns
$t_h(D)$	Data hold time	0			0			0			0			ns
$t_{rec}(W)$	Write recovery time	0			0			0			0			ns
$t_{dis}(W)$	Output disable time after \bar{W} low			30			35			40			45	ns
$t_{dis}(OE)$	Output disable time after \bar{OE} high			30			35			40			45	ns
$t_{en}(W)$	Output enable time after \bar{W} high	10			10			10			10			ns
$t_{en}(OE)$	Output enable time after \bar{OE} low	10			10			10			10			ns

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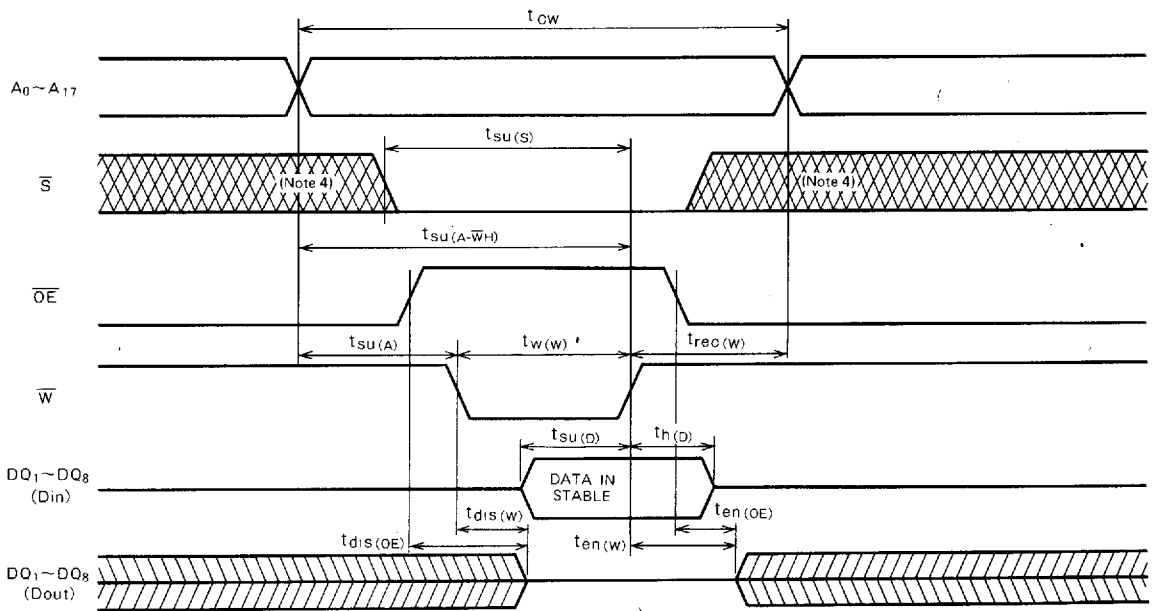
2097152-BIT(262144-WORD BY 8-BIT) CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC) TIMING DIAGRAM

Read cycle



Write cycle (\bar{W} control)

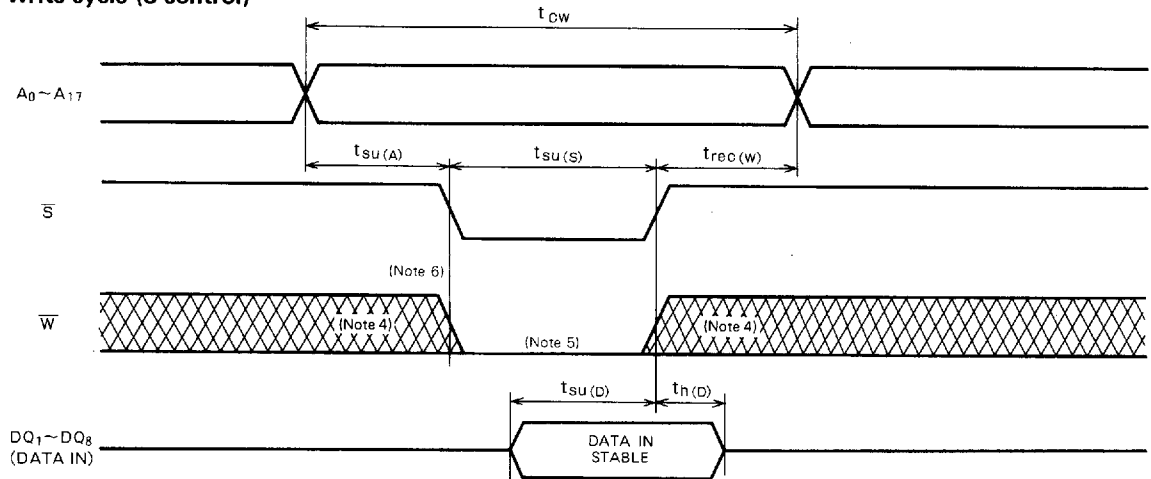


MH25608TNA-85L, -10L, -12L, -15L/ MH25608TNA-85H, -10H, -12H, -15H

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Write cycle (\bar{S} control)



Note 3: Test condition

- Input pulse level: 0.6 ~ 2.4V
- Input pulse rise/fall time: 10ns
- Load: 1 TTL, $C_L = 100\text{pF}$
- Conditions of assessment: 1.5V

- 4: Hatching indicates the state is don't care.
- 5: Writing is executed in overlap of \bar{S} and \bar{W} low.
- 6: If \bar{W} goes low simultaneously with or prior to \bar{S} , the output remains in the high impedance state.
- 7: Don't active inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\bar{S})$	Chip select input \bar{S}	$2.2\text{V} \leq V_{CC(PD)}$	2.2			V
		$2\text{V} \leq V_{CC(PD)} \leq 2.2\text{V}$		$V_{CC(PD)}$		V
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3\text{V}$, A_{15} , A_{16} and $A_{17} < 0.2$ or $> V_{CC} - 0.2$ Other inputs = $0 \sim V_{CC}$	TNA-L		200	μA
			TNA-H		80	

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

