



MT5C6408 883C

MILITARY SRAM

8K x 8 SRAM

T-46-23-12

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-85525, -89691
- JAN M38510/292
- RAD-tolerant (consult factory)

FEATURES

- High speed: 15, 20, 25, 30 and 35ns
- Battery backup - 2 volt data retention
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with CE1 and CE2
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

OPTIONS

- Timing
 - 15ns access
 - 20ns access
 - 25ns access
 - 30ns access
 - 35ns access
 - 45ns access
 - 55ns access
 - 70ns access

MARKING

- 15
- 20
- 25
- 30
- 35
- 45*
- 55*
- 70*

Packages

- Ceramic DIP (300 mil)
- Ceramic DIP (600 mil)
- Ceramic LCC (28 leads)
- Ceramic LCC (32 leads)
- Ceramic Flat Pack (28 leads)

- C
- CW
- EC
- ECW
- F

Two Volt Data Retention

L

* Electrical characteristics identical to those provided for the 35ns access devices.

GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

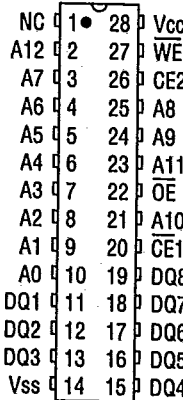
For flexibility in high speed memory applications, Micron offers chip enable (CE) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (WE) and CE inputs are both LOW. Reading is accomplished when WE remains HIGH and CE goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

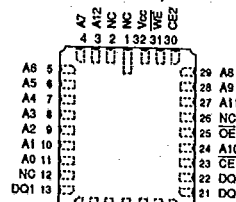
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

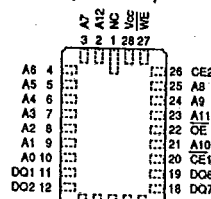
28L/300 DIP



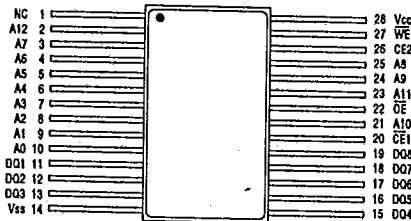
32L/LCC (C-12A)



28L/LCC (C-11A)



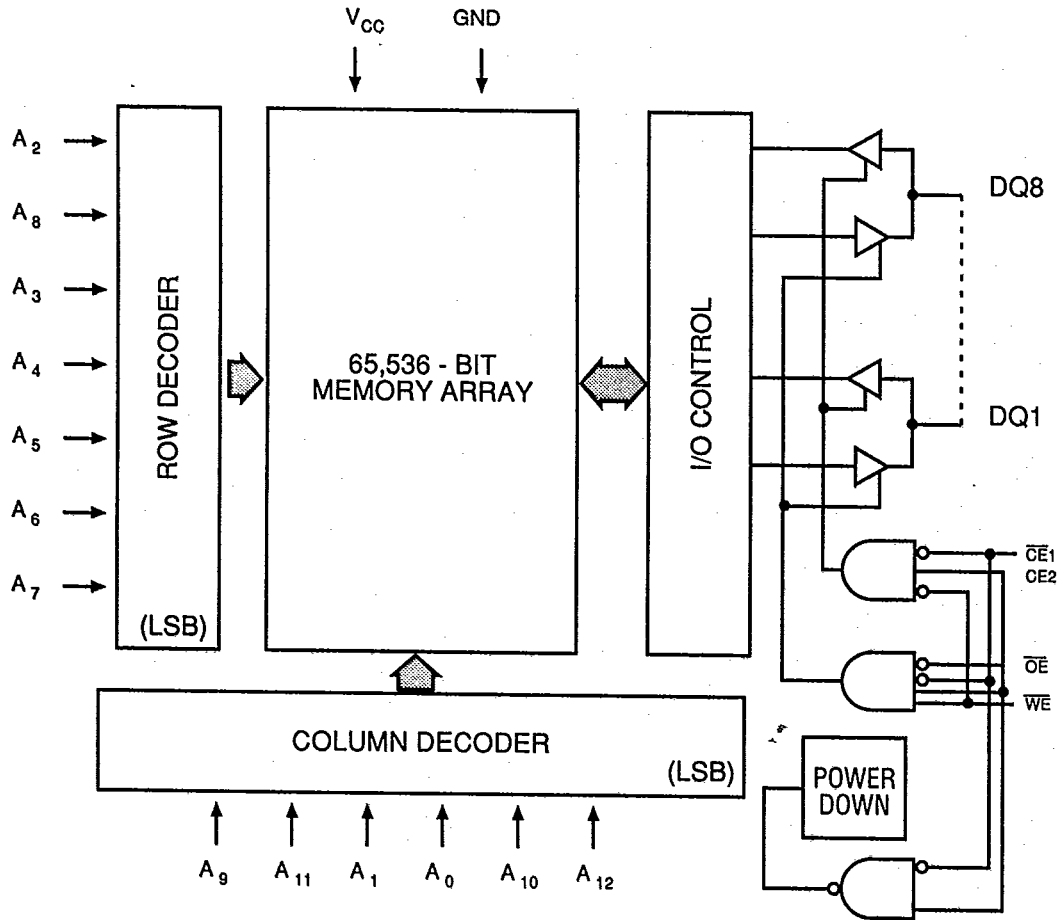
28L Flat Pack (F-12)



FAST SRAM

FUNCTIONAL BLOCK DIAGRAM

FAST SRAM



TRUTH TABLE

MODE	CE1	CE2	WE	OE	DQ	POWER
STANDBY	H	X	X	X	HIGH Z	STANDBY
STANDBY	X	L	X	X	HIGH Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
READ	L	H	H	H	HIGH Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any input or DQ relative to Vss ..-2.0 to +7.0V
 Voltage on Vcc supply relative to Vss-1.0V to +7.0V
 Storage Temperature-65°C to +150°C
 Power Dissipation 1 Watt
 Short Circuit Output Current 50mA
 Lead Temperature (soldering, 10 seconds) +260°C
 Junction Temperature +175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
 (-55°C ≤ T_C ≤ 125°C; Vcc = 5V ± 10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ Vcc	I _{LI}	-10	10	μA	
Output Leakage Current	Outputs Disabled, 0V ≤ V _{OUT} ≤ Vcc	I _{LO}	-10	10	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1

FAST SRAM

DESCRIPTION	CONDITIONS	SYMBOL	MAX					UNITS	NOTES
			-15	-20	-25	-30	-35		
Power Supply Current: Operating	CE ≤ V _{IL} , Vcc = Max., Outputs Open	I _{CC}	130	120	110	100	90	mA	3
Power Supply Current: Standby	CE ≥ V _{IH} , Vcc = Max., f = $\frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I _{SBT1}	50	40	35	30	30	mA	
	CE ≥ V _{IH} , all other inputs ≤ V _{IL} or ≥ V _{IH} , Vcc = Max., f = 0Hz	I _{SBT2}	25	25	25	25	25	mA	
	CE ≥ (Vcc - 0.2), Vcc = Max., all other inputs ≤ 0.2V or ≥ (Vcc - 0.2V), f = 0Hz	I _{SBC2}	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C, f = 1MHz, Vcc = 5V	C _I		8	pF	4
Output Capacitance		C _O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Note 5) $(-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}; V_{CC} = 5V \pm 10\%)$

DESCRIPTION	SYM	-15		-20		-25		-30		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle													
READ cycle time	t_{RC}	15		20		25		30		35		ns	
Address access time	t_{AA}		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		15		20		25		30		35	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		3		3		3		ns	
Chip disable to output in high Z	t_{HZCE}		10		15		15		20		20	ns	6,7
Chip enable to power-up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		15		20		25		30		35	ns	
Output enable access time	t_{AOE}		12		15		15		20		20	ns	
Output enable to output in low Z	t_{LZOE}	0		0		0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		10		15		15		20		20	ns	6
WRITE Cycle													
WRITE cycle time	t_{WC}	15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	13		15		20		25		25		ns	
Address valid to end of write	t_{AW}	15		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	13		15		20		25		25		ns	
Data set-up time	t_{DS}	10		12		15		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	10	0	12	0	15	0	15	0	15	ns	6

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AC TEST CONDITIONS

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

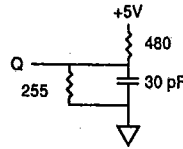


Fig. 1 OUTPUT LOAD EQUIVALENT

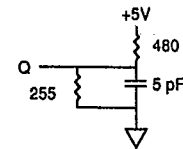


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

- All voltages referenced to V_{ss} (GND).
- 3.0V for pulse width < 20ns.
- I_{cc} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{TRC(MIN)} = \frac{1}{TWC(MIN)} = \text{Hz}$.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- ^tHZCE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from

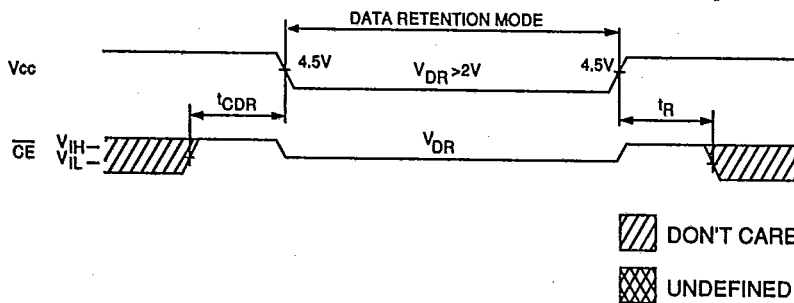
- steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE.
- WE is HIGH for READ cycle.
- Device is continuously selected. All chip enables held in their active state.
- Address valid prior to or coincident with latest occurring chip enable.
- ^tRC = Read cycle time.

FAST SRAM

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNIT	NOTES
V _{cc} for Retention Data		V _{DR}	2	—	V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	I _{ccDR}		300	μA	
Chip Deselect to Data Retention Time		^t CDR	0	—	ns	4
Operation Recovery Time		^t R	^t RC		ns	4, 11

LOW V_{cc} DATA RETENTION WAVEFORM

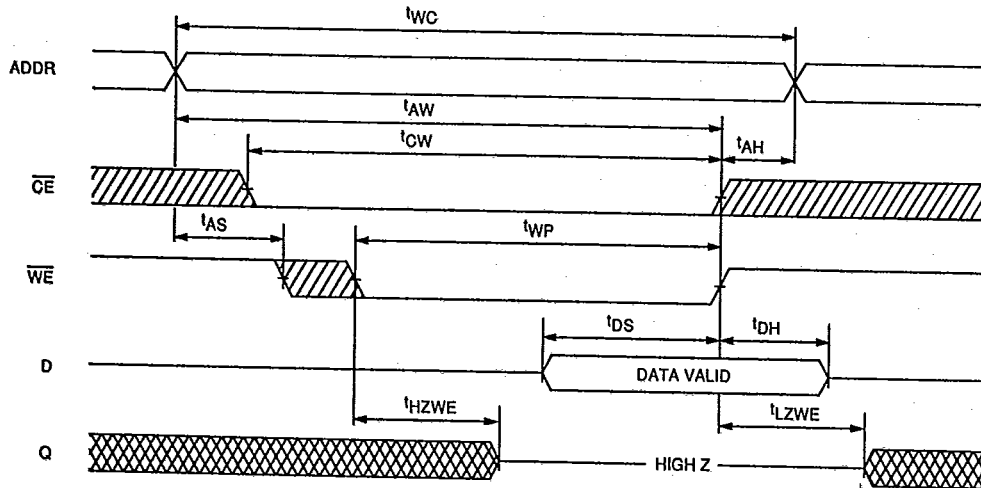


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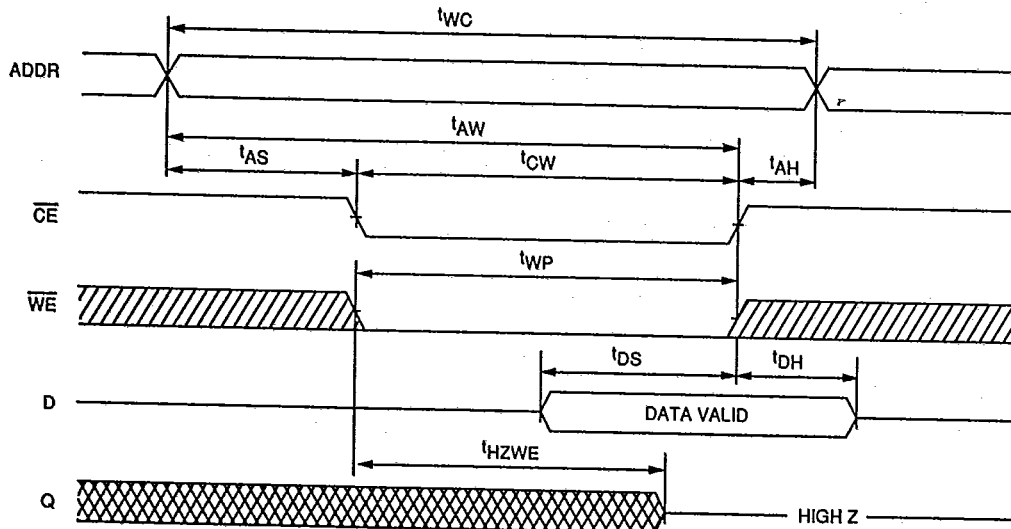
MICRON
TECHNOLOGY INC



MT5C6408 883C

WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



 DON'T CARE
 UNDEFINED

FAST SDRAM

MICRON
TECHNOLOGY INC**MT5C6408 883C****ELECTRICAL TEST REQUIREMENTS**

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per method 5005, Table I)
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8

* PDA applies to subgroup 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes which may affect input or output capacitance.

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