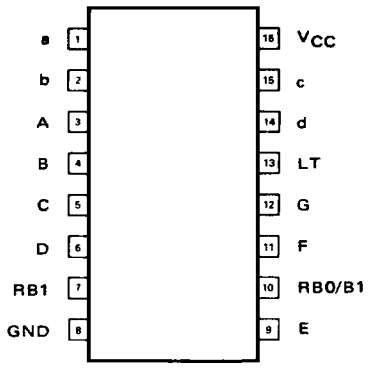
8T06 B,F,W

DESCRIPTION

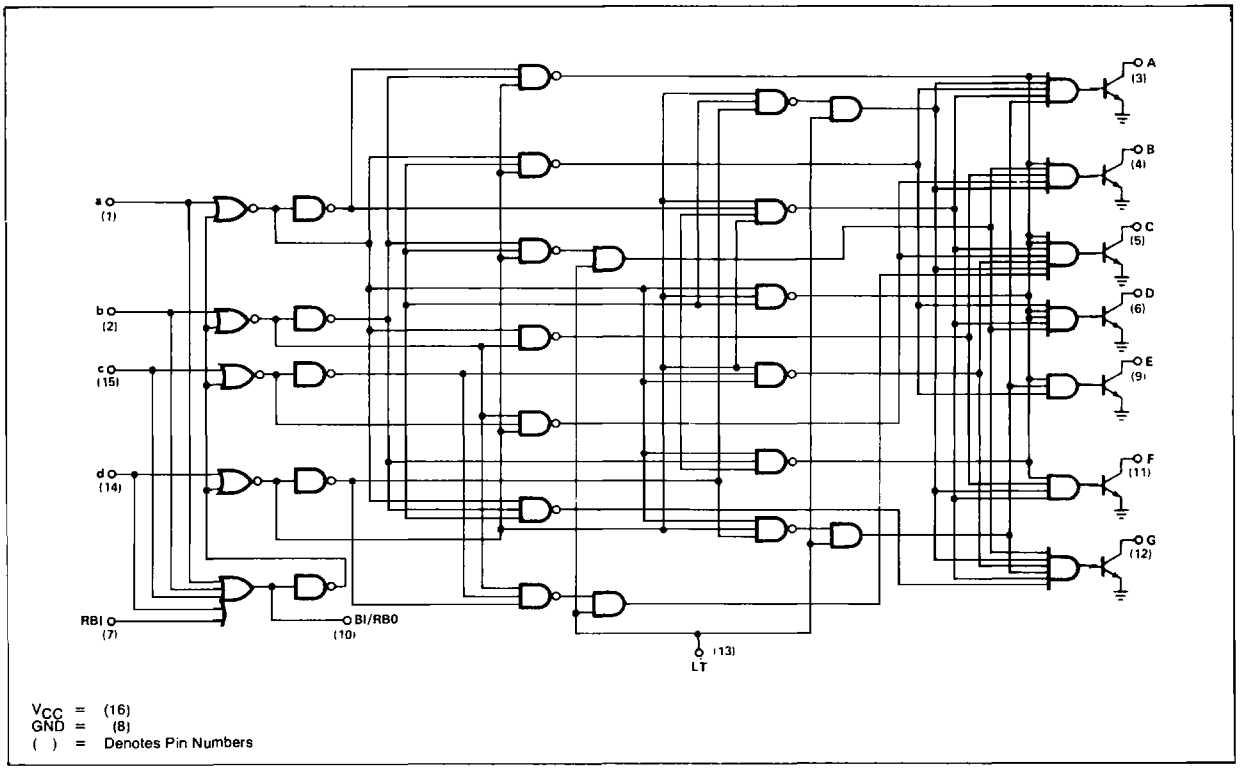
The 8T06 is a monolithic MSI circuit consisting of the necessary logic to decode a 4-bit BCD code to drive 7-segment indicators directly. Open-collector outputs are used for high current source applications, such as driving common cathode LED displays and discrete active components. The 8T06 seven segment decoder/driver accepts a 4-bit binary code and decodes all possible inputs as decimals 0-9 or selected signs and letters. Auxiliary inputs are provided for maximum versatility. The ripple blanking inputs (RBI) and the ripple blanking output (RBO) may be used for automatic leading and/or trailing-edge zero suppression. The RBO output also acts as an overriding blanking input (BI) which may be used for intensity modulation or strobing of the display. A lamp test (LT) input is provided to check the integrity of the display by activating all outputs independent of the input code.

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM

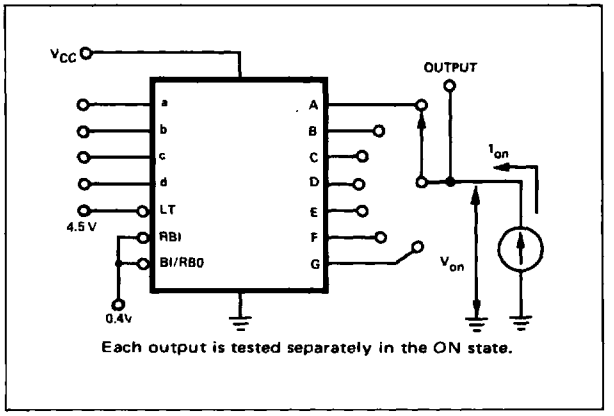


V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

INTERFACE

8T06 B,F,W

TEST FIGURE FOR "0" OUTPUT VOLTAGE



Each output is tested separately in the ON state.

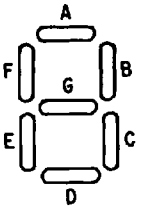
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							DISPLAY CHARACTER
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0[1,2]	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0[1,2]	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1[2]	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	-
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	°
1	1	0	1	1	X	1	0	0	1	0	0	0	0	,
1	1	1	0	1	X	1	0	0	0	1	1	1	0	[
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

* COMMA

X = Don't care, either "1" or "0". BI/RBO is an internally wired OR output.

NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when ab,c,d, RBI terminals are low, or damage may occur to the unit.



SCHEMATIC DIAGRAM