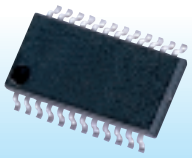
TPD7001BF

● *4-channel Low-Side N-ch Power-MOSFET Driver for ABS Applications*

The IC incorporates a circuit which monitors the voltage between the power MOSFET drain and source. It supports an intelligent function for power MOSFET protection and diagnosis.

Features

- Low-side N-channel power MOSFET driver (input capacitance: 15 nF max)
- Incorporates a power MOSFET overcurrent protection function.
- Incorporates induction load energy clamping function.
- INHIBIT option using enable input, open collector output.
- SSOP 24-pin package for packing in embossed-tape



SSOP-24PIN

Maximum Rating (T_a = 25°C)

Characteristic		Symbol	Rating	Unit
Supply Voltage	DC	V_{DH} (1)	25	V
	Pulse	V_{DH} (2)	30 (1 s)	
Supply Voltage		V_{DL}	10	V
Output Voltage		V_{OPOUT}	10	V
Input Voltage		V_{IN}	−0.5 to 7	V
Output Current		I_{OPOUT}	20	mA
Power Dissipation	T_a = 25°C	P_D	0.5	W
Operating Temperature		T_{opr}	−40 to 110	°C
Junction Temperature		T_j	150	°C
Storage Temperature		T_{stg}	−55 to 150	°C

Electrical Characteristics (T_j = −40 to 110°C, V_{DH} = 13 V, V_{DL} = 5 ± 0.5 V)

Characteristic		Symbol	Terminal	Test Condition	Min	Typ.	Max	Unit
Operating Voltage		V_{DH}	V_{DH}	—	8	13	18	V
		V_{DL}	V_{DL}		4.5	5	5.5	
Current Dissipation		I_{DH}	I_{DH}	V_{IN} = 0 V, V_{DH} = 13 V, Output Off	—	2	5	mA
		I_{DL}	I_{DL}	V_{IN} = 0 V, V_{DL} = 5 V, Output Off	—	8	12	
Input Voltage		V_{IL}	IN / ENB / OPIN	When Output Off	—	—	1.5	V
		V_{IH}		When Output On	3.5	—	—	
Input Current		I_{IL}	IN / ENB / OPIN	V_{IN} = 0 V	—	—	1	µA
		I_{IH}		V_{IN} = 5 V	—	100	200	
High-Level Output Voltage 1		$V_{OH\,1}$	V_{GS}	V_{IN} = 5 V, I_O = 0 A, V_{DH} < 14 V	—	—	V_{DH}	V
High-Level Output Voltage 2		$V_{OH\,2}$	V_{GS}	V_{IN} = 5 V, I_O = 0 A, V_{DH} ≧ 14 V	12	—	15	V
Low-Level Output Voltage		V_{OL}	V_{GS}	V_{IN} = 0 V, I_O = 0 A	—	—	0.5	V
V_{DS} Detection Voltage		V_{DS}	V_{DS}	—	—	1.0	—	V
Diagnostic Resistance		R_{DIAG}	DIAG	—	—	10	—	kΩ
Diagnostic Output Voltage	"L" Level	V_{DIAG}	DIAG	V_{DL} = 5 V	—	—	0.4	V
Diagnostic Output Current	"H" Level	I_{DIAG}	DIAG	V_{DIAG} = 5 V	—	—	10	µA
Optional Output Voltage		V_{OPL}	OPOUT	I_{OP} = 10 mA	—	—	0.4	V
Optional Off Current		I_{OPH}	OPOUT	V_{OPOUT} = 5 V	—	—	10	µA
Zener Voltage between Drain and Gates		V_{CLAMP}	V_{DS}	I_{DS} = 5 mA, V_{CLAMP} = V_{DS}–V_{GS}	30	35	40	V
Switching Time	When On	t_{PLH}	V_{GS}	C_L = 3000 pF (capacitance between V_{GS} and GND pins)	—	—	100	µs
	When Off	t_{PLH}			—	—	100	

Operation

(1) When normal

● **At external power MOS on**

When 3.5 V or more is applied to the IN and ENB pins, the V_{GS} pin goes high and 1 mA (Typ.) constant current drives the power MOS gate.
A V_{GS} mask circuit is built in to prevent erroneous detection of overcurrent in the transient area before the power MOS comes sufficiency on from off state. This circuit is set so that overcurrent is not erroneously detected before the V_{GS} rises to 6.5 V (Typ.).
DIAG output a voltage that is the inverse of the V_{DS} state. The power MOS and its load state can be checked by monitoring the input voltage and the DIAG output.

● **External power MOS off**

When the input voltage of IN or ENB falls to 1.5 V or below, the V_{GS} pin goes low, the external power MOS gate is discharged, and the MOSFET turns off.
The ENB pin has priority over the IN pin. When ENB is low, the V_{GS} pin does not go on even if a high level input voltage is applied to IN.

(2) At Overcurrent

If the V_{DS} pin voltage (the voltage between the power MOS drain and source) is around 1.0 V or above (V_{DS} typical detection voltage) while high level input voltage is applied to the IN and ENB pins, overcurrent to the external power MOS is detected and the V_{GS} output is a instantly shut down and latched. Setting the input voltage back to low level releases the latch.
When the voltage reaches the V_{DS} detection voltage or above, DIAG outputs low level.

(3) At load open

As a pull-down resistor is connected to the V_{DS} pin, when the load is open the V_{DS} pin is always low and high level is output to DIAG.

(4) OPTION function

The OPTION function is controlled by two input pins: OPIN and ENB. ENB has priority over OPIN. When high level voltage is input to OPIN or ENB, the OPOUT pin goes high impedance. This function can be used as a pre-diver for lamps and mechanical relays.

(5) At VDL low voltage

TPD7001BF incorporates a low-voltage lock circuit for locking the V_{GS} and DIAG outputs when V_{DL} falls. This circuit is designed to operate around V_{DL} = 2.8 V (Typ.) or lower. When the circuit is in operation, ENB is locked at low level to cut off the V_{GS} output.

Truth table

State	IN	ENB	V_{DS}	DIAG
Normal	L	H	H	L
	H		L	H
	L	L	H	L
	H		H	L
Overcurrent	L	H	H	L
	H		H	L
	L	L	H	L
	H		H	L
Load Short Circuit	L	H	H	L
	H		H	L
	L	L	H	L
	H		H	L
Power MOS Short Circuit	L	H	L	H
	H		L	H
	L	L	L	H
	H		L	H
Load Open	L	H	L	H
	H		L	H
	L	L	L	H
	H		L	H

OPIN	ENB	OUTPUT
L	H	L
H	H	HZ
L	L	L
H	L	L

*OPOUT is an NPN open collector.
*HZ: High impedance
*ENB is active high.
*DIAG monitors V_{DS} regardless of IN or ENB.