

Description

IDT's RapidWave RWM6050 modem IC is an IEEE 802.11ad based multi-gigabit mixed signal wireless SoC solution targeted to the wireless network infrastructure in the mmWave frequency band. The device enables highly differentiated solutions for network operators and wireless ISP vendors through a range of value added features while minimizing the overall system-level CAPEX and OPEX for the customers.

The network architects can reduce the overall system-level cost and power by leveraging RWM6050's dual modem architecture with quad-channel converters, mixed signal PLL and VCO, on-chip network synchronization, and a high performance PCIe interface with integrated SerDes supporting data rates up to 10Gbps per device.

The RWM6050 based wireless solution enables operators to offer better cost per GB to their consumers by leveraging advanced QoS features, range enhancement techniques, and interference mitigation functions based on flexible scheduling, channelization, wide-band signal processing (1.76GBaud per modem) and real-time radio control interface for a range RF devices in multiple frequency bands. The device simplifies network deployment models by offering both TDD and FDD based PtP and PtMP architectures with various scheduling techniques and autonomous phased array beamforming, making this an ideal solution for roof-top access and backhaul in E-band (71–86 GHz), 5G Small Cell LTE backhaul in Ka-band (28GHz) and fixed wireless access in V-band (57–71 GHz).

The RWM6050 supports both x86 and ARM architectures and comes with a well-defined software API that delivers a rich set of attributes and functionality configurable within the modem and reduces the time to market for the OEMs.

Typical Applications

- Small cell backhaul
- mmWave mesh networking and distribution network
- Residential broadband access
- Residential broadband backhaul and aggregation
- Enterprise and smart city networking

Features

Dual Modem Support

- PHY Subsystem
 - Symbol Rate up to 1.76GBaud per modem
 - Modulation order up to 64-QAM half band or 16-QAM full band
 - Beamforming support with Phased Array Antenna
 - Extensions to support long-distance transmission
 - Mixed Signal Front End with integrated converters
 - IEEE 802.11ad single carrier PHY
- MAC Subsystem
 - Flexible real-time scheduler
 - Secured networking based on AES-GCM
 - IEEE 1588v2 transparent clock support

Interfaces

- PCI Express Gen2
- Flash SPI
- I²C/SPI/UART
- GPIO
- JTAG
- Analog Front End: integrated DACs and ADCs

For a complete list of device features, see [Features – Complete List](#).

Block Diagram

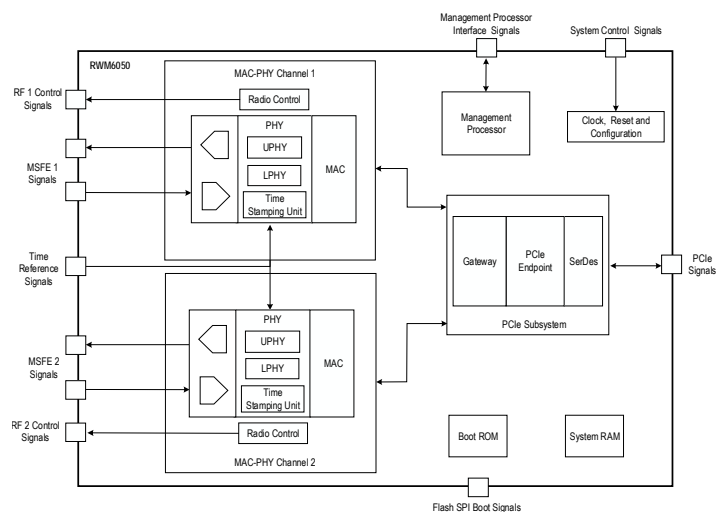


Table of Contents

1.	Functional Overview	6
1.1	Block Diagram.....	6
1.2	Features – Complete List.....	7
1.2.1	Dual PHY Subsystems	7
1.2.2	Dual MAC Subsystems.....	8
1.2.3	Interfaces.....	8
1.2.4	Mixed Signal Front End	8
1.3	MAC PHY Channel Architecture	8
1.4	Typical Applications	9
2.	Pin Assignments	10
2.1	Pin Descriptions.....	11
2.1.1	Functional Signals	11
2.1.2	Supply Signals.....	20
2.1.3	Ground Signals.....	22
3.	Electrical Specifications	23
3.1	Absolute Maximum Ratings	23
3.2	Recommended Operating Conditions.....	24
3.3	Supply Currents and Power	25
3.4	Power Supply Sequencing.....	25
3.4.1	Ramp-up Time.....	25
3.4.2	Power-Up Sequencing.....	25
3.4.3	Power-Down Sequencing.....	26
3.5	DC Electrical Characteristics	26
3.5.1	LVC MOS I/Os.....	26
3.5.2	LVDS I/O	27
3.6	LVC MOS and LVDS I/O AC Specifications	27
3.6.1	AC Timing Test Conditions.....	27
3.6.2	Reference Clock Timing Specification	28
3.6.3	Reset Signal Timing Specifications	30
3.6.4	JTAG Signal Timing Specifications	30
3.6.5	Radio Control Interface Signal Timing Specifications.....	32
3.6.6	Flash SPI (FSPI) Boot Interface Signal Timing Specifications	35
3.6.7	System SPI Interface Signal Timing Specifications.....	36
3.6.8	I ² C Interface Signal Timing Specifications	37
3.7	Mixed Signal Front End Interface Characteristics.....	38
3.7.1	MSFE ADC Specifications.....	38
3.7.2	MSFE DAC Specifications.....	40
3.7.3	MSFE Reference Clock.....	41
3.7.4	MSFE External Matching Recommendations.....	44
3.8	PCIe Interface Characteristics	46
3.8.1	PCIe Reference Clock.....	46
3.8.2	PCIe Differential Receiver and Transmitter Specifications.....	47
4.	System Clocking.....	50
4.1	System Oscillator.....	50
4.2	System PLLs.....	50
4.3	PHY Clocks.....	50

5.	Package Specifications.....	52
5.1	Package Information.....	52
5.2	Package Outline Drawings.....	52
5.3	Thermal Characteristics.....	52
6.	Marking Diagram.....	54
7.	Ordering Information.....	54
	Revision History.....	55

List of Figures

Figure 1. RWM6050 Block Diagram.....	6
Figure 2. Dual RWM6050 Wireless Node – N-E-W-S Configuration.....	9
Figure 3. Single RWM6050 Wireless Leaf Node.....	9
Figure 4. Pin Assignments – Top View	10
Figure 5. Circuit for the System XTAL	28
Figure 6. Single-ended System Reference Clock	29
Figure 7. JTAG (Debug and Test) Signal Timings	31
Figure 8. RCI LVCMOS AC Timing Diagram	32
Figure 9. RCI LVDS AC Timing Diagram	33
Figure 10. RCIx_GPIO_n, n = 2:6, AC Timing Diagram – SDR Operation	34
Figure 11. RCIx_GPIO_n, n = 2:6, AC Timing Diagram – DDR Operation	34
Figure 12. FSPI AC Timing Diagram.....	35
Figure 13. System SPI AC Timing Diagram.....	36
Figure 14. I ² C AC Timing Diagram.....	38
Figure 15. Differential MSFE Reference Clock with AC Coupling - An Example	41
Figure 16. Single-ended MSFE Reference Clock Coupling	42
Figure 17. Circuit for the MSFE XTAL.....	43
Figure 18. Equivalent Circuit for MSFE DAC Outputs.....	44
Figure 19. Equivalent Circuit for MSFE ADC Inputs – DC Coupled ^[1]	45
Figure 20. Equivalent Circuit for MSFE ADC Inputs – AC Coupled	45
Figure 21. PHY Clocks – RWM6050 Master, RF Slave	50
Figure 22. PHY Clocks – RF Master, RWM6050 Slave	51
Figure 23. PHY Clocks – RWM6050 and RF Slave	51

List of Tables

Table 1.	Signal Function Key	11
Table 2.	System Control Signals	11
Table 3.	PCIe Interface Signals	13
Table 4.	Auxiliary Signals	13
Table 5.	Radio Control Interface (RCI) Signals	14
Table 6.	Flash SPI Boot Interface Signals	15
Table 7.	Management Processor Interface Signals	16
Table 8.	MSFE Signals	18
Table 9.	JTAG/Test Signals	19
Table 10.	DNC Signals	19
Table 11.	Power Supply and Reference Signals	20
Table 12.	Ground Signals	22
Table 13.	Absolute Maximum Ratings	23
Table 14.	Recommended Operating Conditions	24
Table 15.	Supply Currents and Power	25
Table 16.	1.8V LVCMOS I/O DC Parameters	26
Table 17.	LVDS I/O DC Parameters	27
Table 18.	LVCMOS AC Test Conditions for VDDIO = 1.8V	27
Table 19.	LVDS AC Test Conditions for LVDS_VDDIO = 1.8V	27
Table 20.	Recommended Values for System XTAL Oscillator	28
Table 21.	Reference Clock Specification	29
Table 22.	Reset Signal Timing Specifications	30
Table 23.	Debug JTAG Signal Timing Specifications	30
Table 24.	Test JTAG Signal Timing Specifications	31
Table 25.	RCI LVCMOS AC Timing Parameters	32
Table 26.	RCI LVDS AC Timing Parameters	33
Table 28.	RCIx_GPIO_n, n = 2:6, AC Timing Parameters – DDR Operation	34
Table 27.	RCIx_GPIO_n, n = 2:6, AC Timing Parameters – SDR Operation	34
Table 29.	FSPI Interface AC Timing Parameters	35
Table 30.	System SPI Interface AC Timing Parameters	36
Table 31.	I ² C Interface Signal Timing Specifications	37
Table 32.	ADC Characteristics	38
Table 33.	ADC Full-scale Input Configuration	39
Table 34.	IQ DAC Characteristics	40
Table 35.	MSFE Reference Clock Specifications	41
Table 36.	Recommended Values for Single-ended MSFE Reference Clock Coupling	42
Table 37.	Recommended Values for MSFE XTAL Oscillator	43
Table 38.	PCIe PCIE_CLKP/PCIE_CLKN Requirements	46
Table 39.	PCIe Differential Receiver Specifications	47
Table 40.	PCIe Differential Transmitter Specifications	48
Table 41.	Package Information	52
Table 42.	Junction to Board/Case Thermal Characteristics (Theta JB/JC)	52
Table 43.	Junction to Ambient Thermal Characteristics (Theta JA)	53
Table 44.	With External Heat Sink	53

1. Functional Overview

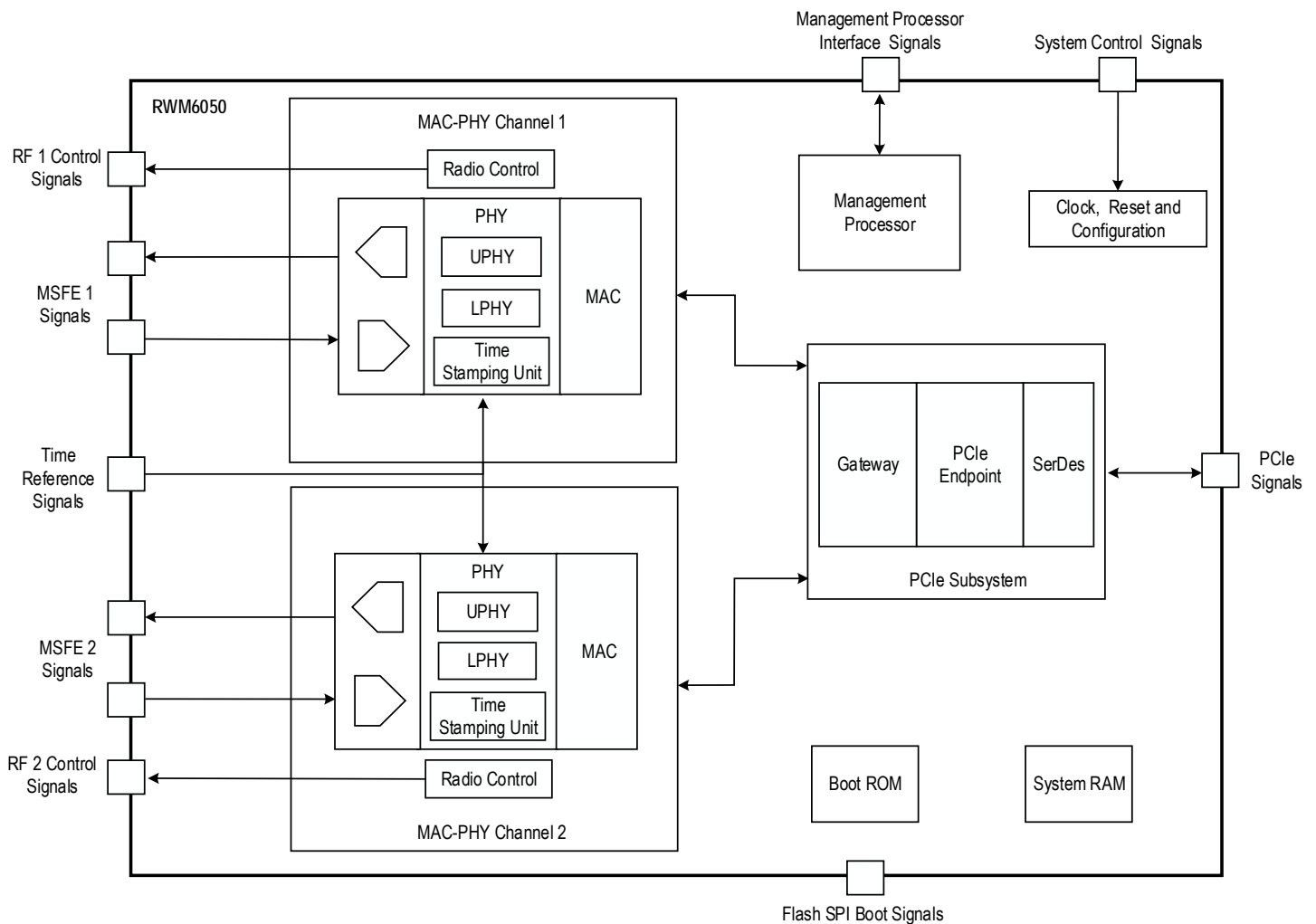
1.1 Block Diagram

A high-level block diagram of the RWM6050 is shown in [Figure 1](#). The device supports two independent MAC PHY channels, each with the capability to process wireless signals with up to 2.16GHz channel spacing and interfaces with an external host CPU over the common PCIe subsystem that can support data rates up to 10GBaud.

Each MAC PHY channel is comprised of the following functional blocks:

- Physical Layer processor (PHY), containing a dual-channel mixed signal front-end (MSFE), Lower PHY (LPHY), and Upper PHY (UPHY) processing functions
- MAC processor (MAC), containing upper and lower MACs and a set of hardware off-load engines
- Radio control interface (RCI), containing radio control and management functions for phased array RF transceivers

Figure 1. RWM6050 Block Diagram



In addition to the MAC PHY channels, the RWM6050 contains the following common functional blocks:

- One supervisory RISC processor
- High-speed PCIe Gen2 interface for connection to an appropriate host
- Common system RAM
- Primary Boot ROM
- System interfaces such as I2C, SPI, UART, and JTAG
- PLLs for clock generation
- System peripherals such as system timers, a real-time clock, and a watchdog supervisor

1.2 Features – Complete List

1.2.1 Dual PHY Subsystems

1.2.1.1 Firmware Supporting

- 802.11ad MCS 0 ($\pi/2$ DBPSK)
- 802.11ad MCS 1–5 ($\pi/2$ BPSK)
- 802.11ad MCS 6–9 ($\pi/2$ QPSK)
- 802.11ad MCS 10–12 ($\pi/2$ 16-QAM)
- Extended MCS 12 ($\pi/2$ 64-QAM)
- Optimized PHY for long range beamforming

1.2.1.2 Lower PHY

- First stage DSP processing
 - Radio artifact compensation
 - DC offset
 - IQ imbalance
 - Time and frequency synchronization
 - Receiver automatic gain control (AGC)
 - Programmable digital channel bandwidth:
 - Full band
 - Half-band
 - Quarter-band
 - Programmable digital intermediate frequency (IF) within baseband channel in half-band and quarter-band modes
 - IQ data pulse shaping
 - Channel estimation
- Radio interface control
- Time stamping unit

1.2.1.3 Upper PHY

- Vector Processing Elements
- FFT/IFFT units: 512 points
- Single Carrier Frequency Domain Equalization (SC-FDE)
- LDPC encode/decode unit: configurable maximum number of decoding iterations

1.2.2 Dual MAC Subsystems

- Flexible data plane and real-time scheduler
 - Encryption based on AES-GCM
 - Static and Dynamic Scheduling
 - CBAP and SP scheduling
- Network Synchronization using IEEE 1588v2 transparent clock

1.2.3 Interfaces

- PCI Express Base Specification (Revision 2.1)
 - Two lanes
 - 5 or 2.5GT/s per lane
 - 256-byte maximum payload size
 - Two physical functions
- SPI Flash Interface
 - Boot from SPI NOR Flash
 - Single, Dual, Quad I/O modes up to 50MHz
- UART with flow control
- JTAG
- General purpose I/Os
- Multi-vendor radio control interface

1.2.4 Mixed Signal Front End

- IQ DACs and IQ ADCs
 - 7-bit DAC and 7-bit ADC
 - ENOB: 6-bit
 - Sample clock: 3.52, 1.173, or 0.880GHz
- Differential IQ signaling
- 3.52 GHz PLL
 - Jitter < 1.0ps
 - Typical reference: 54MHz

1.3 MAC PHY Channel Architecture

The PHY Channel is a heterogeneous multiprocessing technology. It uses multiple levels of parallelism and pipelining with an optimum mixture of programmable and fixed function units. This architecture allows a conventional software model to control the PHY processing resources in an optimally efficient way, while providing a “Region of Programmability” to cover the various modulation and coding schemes. The reference firmware can also be extended for special modulation schemes or custom algorithms, for example equalization or beamforming. The PHY differs from a conventional wireless processor pipeline design because it has a scalable multiprocessor arrangement in the PHY section. The design and operating model of the cluster of PHY Parallel Processing Units (PPUs) enables the very intensive DSP load required for the modulation and coding of multi-gigabit data rates to be controlled by a conventional embedded software model.

The MAC function is similarly comprised of a hardware/software processing scheme with all data path and latency critical functions implemented in hardware. Other functions run as software on an array of embedded RISC processors. This hybrid of software and hardware enables the use of a wide range of MAC protocol and frame formats, including 802.11ad compatible schemes.

1.4 Typical Applications

Typical applications for the RWM6050 include the following:

- Small cell backhaul
- mmWave mesh networking and distribution network
- Residential broadband access
- Residential broadband backhaul and aggregation
- Enterprise and smart city networking

Figure 2 shows a backhaul wireless node using two RWM6050 devices in a North/East/West/South (N-E-S-W) configuration. Each RWM6050 can support two 90° sectors simultaneously. The RWM6050 connects to a local NPU Processor via PCIe to provide bridge/switch capabilities between the MACs, and to a local wired CPE connection. This dual TDD PHY/MAC modem supports 360° azimuth coverage with four mmWave RF/Antenna arrays.

Figure 2. Dual RWM6050 Wireless Node – N-E-W-S Configuration

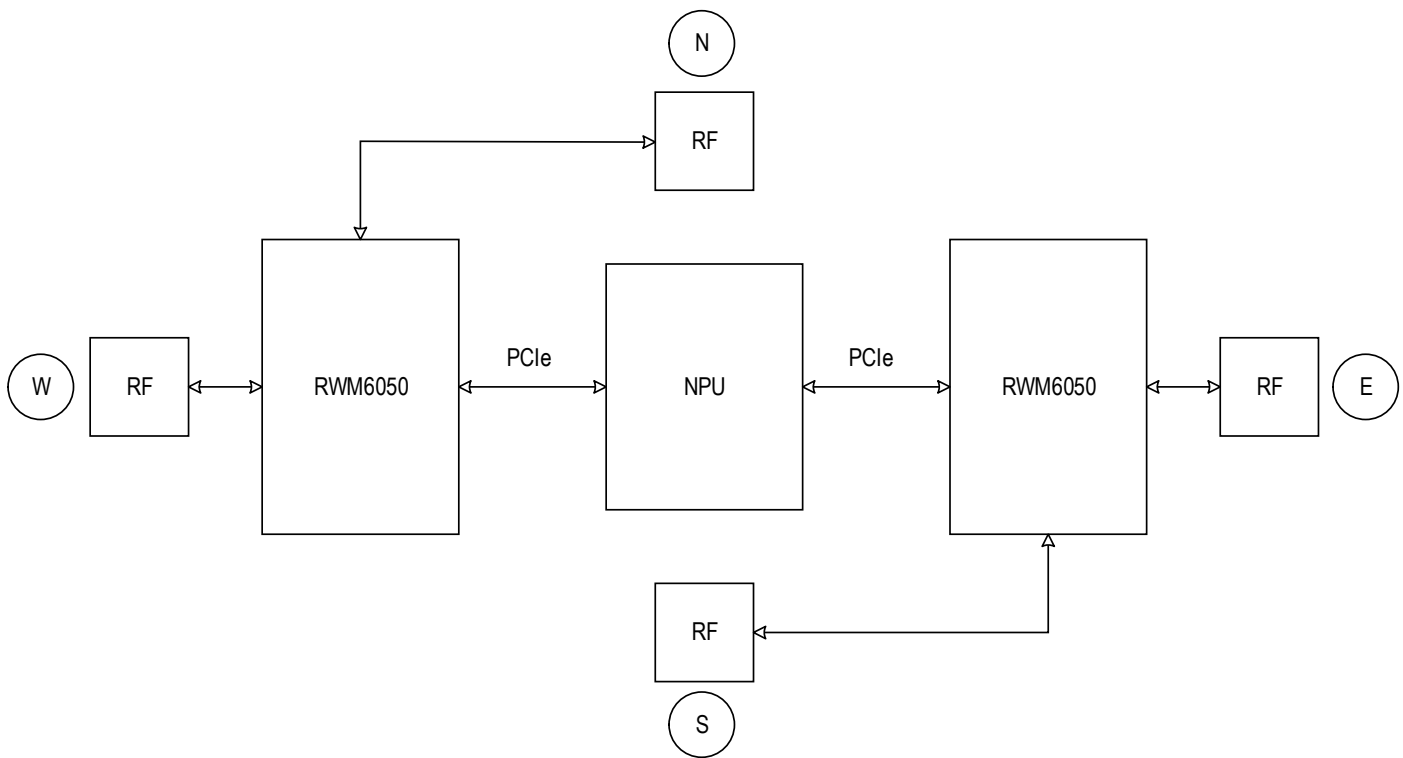
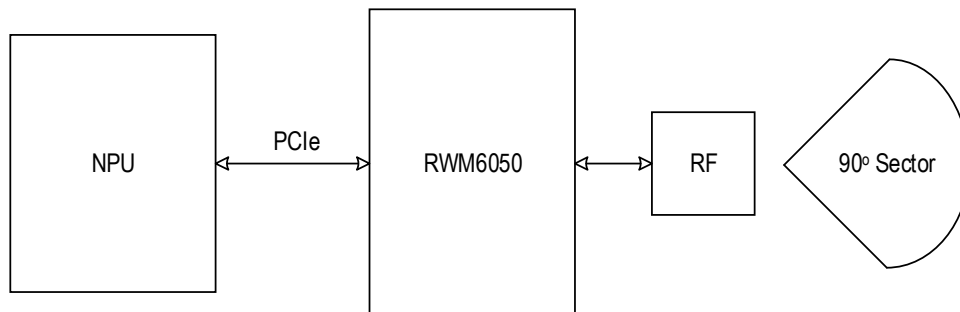


Figure 3 shows a backhaul wireless node using a single RWM6050 module. One MAC in the RWM6050 supports one active 90° sector with a local NPU providing bridge/switch capabilities to a local wired CPE connection.

Figure 3. Single RWM6050 Wireless Leaf Node



2. Pin Assignments

Figure 4. Pin Assignments – Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22		
A	VSSIO	SPL_CS_N	DNC	A4	A5	DNC	DNC	PCIE_CLKP	PCIE_TX0_N	PCIE_RX0_N	PCIE_RX0_P	PCIE_TX1_N	PCIE_RX1_N	PCIE_PERS_T_N	VSS	SYSOSC_X0	SYSOSC_X1	RESET_N	PWM_0	I2C_SCL	I2C_SDA	VSSIO	A	
B	SPL_SCLK	SPL_MISO	A2	A3	VSS	A6	VSS	PCIE_CLKN	VSS	PCIE_TX0_P	VSS	PCIE_TX1_P	VSS	PCIE_RX1_P	PCIE_WAKEN	REFCLK_TSY_NC0	REFCLK_TSY_NC1	VSSIO	PWM_1	JTAG_TDO	JTAG_TCK	RESET_OUT	B	
C	SPL_MOSI	GPIO_0	A1	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	PCIE_CLKREN	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	JTAG_TDI	JTAG_TMS	MODE0	C
D	GPIO_1	GPIO_2	VDDIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	VSSIO	PLL1_VDDH	VSSIO	VSSIO	PLL0_VDDH	VSSIO	VDDIO	JTAG_SELECT	JTAG_TRST_N	MODE1	D	D	
E	GPIO_3	GPIO_4	GPIO_5	VSS	VSSIO	A7	VSS	AUX_VP2	VSS	PCIE_VPH	VSS	PCIE_RBIA_S	VSS	PLL1_VDDA	PLL1_VSSA	PLL0_VSSA	PLL0_VDDA	RCIO_CS_N7_S	VSSIO	DEBUG_TCK	FSPL_CLK	FSPL_CS_N	E	
F	GPIO_6	GPIO_7	GPIO_8	VSSIO	VSSIO	VSSIO	AUX_VPH	VSS	AUX_VP1	VSS	PCIE_VPTX	VSS	PCIE_VP	PLL1_DVDD	PLL1_DVSS	PLL0_DVSS	PLL0_DVDD	RCIO_CS_N6_S	VDDIO	VSSIO	FSPL_D0	FSPL_D1	F	
G	GPIO_9	GPIO_10	VSSIO	VSSIO	VSSIO	TSENSE_AVDDH	TSENSE_AVSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VSSIO	VDD	VSSIO	RCIO_CS_N5_S	RCIO_CS_N4_S	DEBUG_TDO	FSPL_D2_WP_N	FSPL_D3_HN	G	
H	GPIO_11	GPIO_12	VDDIO	VSSIO	VSSIO	VSSIO	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	RCIO_CS_N3_S	VSSIO	DEBUG_TDI	UART_RTS	UART_RX	H	
J	GPIO_13	GPIO_14	GPIO_15	RC1_CS_N6_S	RC1_CS_N7_S	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	RCIO_CS_N2_S	RCIO_MISO7_S	DEBUG_TMS	UART_CTS	UART_TX	J	
K	RC1_GPIO0	RC1_GPIO1	RC1_GPIO2	RC1_CS_N4_S	RC1_CS_N5_S	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSSIO	VSSIO	DEBUG_TRSTN	RCIO_GPIO1	RCIO_GPIO0	K	
L	RC1_GPIO3	RC1_GPIO4	RC1_GPIO5	RC1_CS_N2_S	RC1_CS_N3_S	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	RCIO_GPIO5	RCIO_GPIO4	RCIO_GPIO3	RCIO_GPIO2	L	
M	RC1_CS_N0_N	RC1_CS_N0_P	LVDS_VDDIO	VSSIO	RC1_MISO7_S	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	LVDS_VDDIO	VSSIO	RCIO_CS_N0_P	RCIO_CS_N0_N	M	
N	RC1_SCLK_N	RC1_SCLK_P	RC1_GPIO6	RC1_GPIO7	RC1_GPIO8	VDDIO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	RCIO_GPIO8	RCIO_GPIO7	RCIO_GPIO6	RCIO_SCLK_P	RCIO_SCLK_N	N	
P	RC1_MOSI0_N	RC1_MOSI0_P	VSSIO	LVDS_VDDIO	RC1_GPIO9	VSSIO	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	RCIO_GPIO9	LVDS_VDDIO	VSSIO	RCIO_MOSI0_P	RCIO_MOSI0_N	P	
R	RC1_MOSI1_N	RC1_MOSI1_P	RC1_REF	RC1_SCLK_S	RC1_CS_N0_S	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	RCIO_CS_N0_S	RCIO_SCLK_S	RCIO_REF	RCIO_MOSI1_P	RCIO_MOSI1_N	R	
T	RC1_MOSI2_N	RC1_MOSI2_P	RC1_MISO0_S	RC1_MISO1_S	RC1_VDDIO	MSFE1_AVSS	MSFE1_PLL_AVDD	MSFE1_AVSS	MSFE1_OSC_AVDDH	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVDD	MSFE1_AVSS	MSFE1_OSC_AVDDH	MSFE1_AVSS	MSFE1_PLL_AVDDH	MSFE1_AVSS	MSFE1_AVDDH	VSSIO	RCIO_MISO1_S	RCIO_MISO0_S	RCIO_MOSI2_P	RCIO_MOSI2_N	T
U	RC1_MOSI3_N	RC1_MOSI3_P	RC1_MOSI0_S	RC1_MOSI1_S	VSSIO	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_PLL_AVDDH	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE1_OSC_AVDDH	MSFE1_AVSS	MSFE1_PLL_AVDDH	MSFE1_AVSS	MSFE1_AVDDH	RCIO_VDDIO	RCIO_MOSI1_S	RCIO_MOSI0_S	RCIO_MOSI3_P	RCIO_MOSI3_N	U
V	RC1_CS_N1_N	RC1_CS_N1_P	RC1_MOSI2_S	RC1_MOSI3_S	RC1_CS_N1_S	MSFE1_AVSS	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE1_AVDD	MSFE1_AVSS	MSFE1_AVDDH	MSFE1_AVSS	RCIO_CS_N1_S	RCIO_MOSI3_S	RCIO_MOSI2_S	RCIO_CS_N1_P	RC1_CS_N1_N	V
W	VSSIO	LVDS_VDDIO	VSSIO	VDDIO	MSFE1_AVSS	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_AVDDH	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	VDDIO	VSSIO	LVDS_VDDIO	VSSIO	W	
Y	MSFE1_ADC_IN	MSFE1_AVSS	RC1_MISO6_S	RC1_MISO5_S	RC1_MISO4_S	RC1_MISO3_S	RC1_MISO2_S	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	RCIO_MISO2_S	RCIO_MISO3_S	RCIO_MISO4_S	RCIO_MISO6_S	MSFE1_AVSS	MSFE1_ADC_IN	Y
AA	MSFE1_ADC_IP	MSFE1_ADC_VCM	MSFE1_AVSS	MSFE1_CLK_OUT	MSFE1_AVSS	MSFE1_AVSS	DNC	DNC	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	MSFE1_AVSS	DNC	DNC	MSFE1_AVSS	MSFE1_AVSS	MSFE1_CLK_OUT	MSFE1_AVSS	MSFE1_ADC_VCM	MSFE1_ADC_IP	AA
AB	MSFE1_AVSS	MSFE1_ADC_ON	MSFE1_ADC_OP	MSFE1_REF_LKN	MSFE1_REF_LKP	MSFE1_VDD	MSFE1_XI	MSFE1_DAC_ON	MSFE1_DAC_OP	MSFE1_DAC_IN	MSFE1_DAC_IP	MSFE1_DAC_IP	MSFE1_DAC_IN	MSFE1_DAC_OP	MSFE1_DAC_ON	MSFE1_XI	MSFE1_XD	MSFE1_REF_CLKP	MSFE1_REF_CLKN	MSFE1_ADC_OP	MSFE1_ADC_ON	MSFE1_AVSS	AB	

2.1 Pin Descriptions

2.1.1 Functional Signals

Table 1. Signal Function Key

Symbol	Meaning
I	LVC MOS input
O	LVC MOS output
IO	LVC MOS input/output
LVDS_I	LVDS input
LVDS_O	LVDS output
CML_I	CML input
GND	Ground
A	Analog
P	Power supply
PU	Weak pull-up
PD	Weak pull-down
Prog-PU	Programmable pull-up/down Default setting: Weak pull-up
Prog-PD	Programmable pull-up/down Default setting: Weak pull-down
Prog	Programmable pull-up/down
OD	Open-drain output
ST	Schmitt trigger input

Table 2. System Control Signals

Signal Name	Ball	Type		Voltage	Description
RESET_N	A18	I	ST-PU	1.8	Active-low asynchronous system reset input. This pin is a Schmitt trigger input with an internal pull-up.
RESET_OUT	B22	O	-	1.8	Reset indication output. This signal is high when the RWM6050 is being reset.
SYSOSC_XI	A17	I	-	1.8	Crystal Connection input. Accepts a 25MHz reference from a clock oscillator or a resonant crystal.
SYSOSC_XO	A16	O	-	1.8	Crystal Connection output. This pin should be connected to a crystal. If a clock oscillator is connected to SYSOSC_XI, then this pin must be left unconnected.

Table 2. System Control Signals (Cont.)

Signal Name	Ball	Type		Voltage	Description
MODE0	C22	I	PD	1.8	<p>Boot configuration inputs. The RWM6050 boot mode is determined by the state of the pins as follows:</p> <ul style="list-style-type: none"> ▪ 00: <ul style="list-style-type: none"> – Primary boot: From the internal Boot ROM – Secondary boot: From FSPI interface. The Flash memory must have valid RWM6050 code. ▪ 01: Reserved. ▪ 10: Reserved. ▪ 11: Suspend Boot. This mode prevents the RWM6050 from booting. Use this mode to program the flash memory through the Debug JTAG interface. For more information, see “Programming the FSPI Flash Device via Debug JTAG” in the <i>RWM6050 User Manual</i>. <p>These pins are static inputs and must be set to the required state when the RESET_N is asserted low.</p>
MODE1	D22	I	PD	1.8	
REFCLK_TSYNC0	B16	I	Prog	1.8	<p>External timing reference input for use with IEEE1588v2.</p> <ul style="list-style-type: none"> ▪ REFCLK_TSYNC0: This signal provides the reference clock for the RWM6050 time-stamping unit. The required frequency of this signal is nominally 100MHz. ▪ REFCLK_TSYNC1: This signal carries the pulse-per-second (PPS) signal. It is required to pulse high every fixed period to provide physical representation of time.
REFCLK_TSYNC1	B17	I	Prog	1.8	
DEBUG_TCK	E20	I	ST	1.8	Debug IEEE 1149.1/1149.6 test access port: Clock input. This signal is a Schmitt trigger input.
DEBUG_TDI	H20	I	ST-PU	1.8	Debug IEEE 1149.1/1149.6 test access port: Serial data input. This signal is a Schmitt trigger input with internal pull-up.
DEBUG_TDO	G20	O	OD	1.8	Debug IEEE 1149.1/1149.6 test access port: Serial data output.
DEBUG_TMS	J20	I	ST-PU	1.8	Debug IEEE 1149.1/1149.6 test access port: Test mode select input. This signal is a Schmitt trigger input with internal pull-up.
DEBUG_TRSTN	K20	I	ST-PD	1.8	Debug IEEE 1149.1/1149.6 test access port: This active-low reset input signal is a Schmitt trigger input with internal pull-down.

Table 3. PCIe Interface Signals

Signal Name	Ball	Type		Voltage	Description
PCIE_CLKN	B8	LVDS_I	-	1.8	PCIe differential reference clock. The required nominal PCIE_CLKP/PCIE_CLKN frequency is 100MHz.
PCIE_CLKP	A8		-	1.8	
PCIE_RX0_N	A10	LVDS_I	-	1.8	PCIe differential receive inputs – Receive Lane 0
PCIE_RX0_P	A11		-	1.8	
PCIE_RX1_N	A13	LVDS_I	-	1.8	PCIe differential receive inputs – Receive Lane 1
PCIE_RX1_P	B14		-	1.8	
PCIE_TX0_N	A9	LVDS_O	-	1.8	PCIe differential transmit outputs – Transmit Lane 0
PCIE_TX0_P	B10		-	1.8	
PCIE_TX1_N	A12	LVDS_O	-	1.8	PCIe differential transmit outputs – Transmit lane 1
PCIE_TX1_P	B12		-	1.8	
PCIE_CLKREQN	C13	IO	ST-OD	1.8	PCIe reference clock request signal. This active-low signal has an open-drain output and Schmitt trigger input.
PCIE_PERSTN	A14	I	ST	1.8	PCIe functional reset input.
PCIE_WAKEN	B15	IO	ST-OD	1.8	PCIe wake request. This active-low signal has an open-drain output and Schmitt trigger input.
PCIE_RBIAS	E12	A	-	1.8	External reference resistor connection pin. Attach a $200 \pm 1\%$ Ohm resistor to ground with a temperature coefficient of resistance α of 1% over 100°C. The external resistor is automatically used for calibration when the RWM6050 comes out of reset.

Table 4. Auxiliary Signals

Signal Name	Ball	Type		Voltage	Description
A1	C3	I	PD	1.8	This signal should be tied to ground through a 1KOhm pull-down resistor.
A2	B3	IO	-	1.8	This signal should be tied to ground through a 1KOhm pull-down resistor.
A3	B4	LVDS_I	-	1.8	This signal should be tied to ground through a 50Ohm pull-down resistor.
A4	A4		-	1.8	This signal should be tied to ground through a 50Ohm pull-down resistor.
A5	A5	LVDS_I	-	1.8	This signal should be tied to ground through a 50Ohm pull-down resistor.
A6	B6		-	1.8	This signal should be tied to ground through a 50Ohm pull-down resistor.
A7	E6	A	-	1.8	This signal should be tied to ground through a 200Ohm resistor.

Table 5. Radio Control Interface (RCI) Signals^[a]

Signal Name ^[b]	Ball	Type		Voltage	Description
RCIx_SCLK_N	N22, N1	LVDS_O	-	1.8	Differential clock output for RF management interface. When the Radio Control Interface is configured to operate in QPSI-Like mode, the RCIx_SCLK_N/P is a free running signal with a configurable frequency of up to 200MHz.
RCIx_SCLK_P	N21, N2		-	1.8	
RCIx_CSN0_N	M22, M1	LVDS_O	-	1.8	Differential chip select 0 output for RF management interface. When enabled, this signal is asserted low to initiate a management transaction to the connecting RF device.
RCIx_CSN0_P	M21, M2		-	1.8	
RCIx_CSN1_N	V22, V1	LVDS_O	-	1.8	Differential chip select 1 output for RF management interface. When enabled, this signal is asserted low to initiate a management transaction to the connecting RF device.
RCIx_CSN1_P	V21, V2		-	1.8	
RCIx_MOSI0_N	P22, P1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 0.
RCIx_MOSI0_P	P21, P2		-	1.8	
RCIx_MOSI1_N	R22, R1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 1.
RCIx_MOSI1_P	R21, R2		-	1.8	
RCIx_MOSI2_N	T22, T1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 2.
RCIx_MOSI2_P	T21, T2		-	1.8	
RCIx_MOSI3_N	U22, U1	LVDS_O	-	1.8	Differential data output for RF management interface – Bit 3.
RCIx_MOSI3_P	U21, U2		-	1.8	
RCIx_SCLK_S	R19, R4	O	-	1.8	RCIx Single-ended full swing clock output for RF management interface. When the Radio Control Interface is configured to operate in QSPI/SPI mode, the RCIx_SCLK_S runs when the RCIx_CSNx_S is asserted low. The frequency of RCIx_SCLK_S is tunable from 31.42 to 73.33MHz.
RCIx_CSN _n _S	R18, R5 V18, V5 J18, L4 H18, L5 G19, K4 G18, K5 F18, J4 E18, J5	O	-	1.8	RCIx single-ended full swing chip select <i>n</i> output for RF management interface. First row lists balls of RCI0, second row lists balls of RCI1. When enabled, this signal is asserted low to initiate a management transaction to the connecting RF device.
RCIx_MOSI0_S	U20, U3	O	-	1.8	RCIx single-ended full swing data output for the RF management interface – Bit 0.
RCIx_MOSI1_S	U19, U4	O	-	1.8	RCIx single-ended full swing data output for the RF management interface – Bit 1.
RCIx_MOSI2_S	V20, V3	O	-	1.8	RCIx single-ended full swing data output for the RF management interface – Bit 2.
RCIx_MOSI3_S	V19, V4	O	-	1.8	RCIx single-ended full swing data output for the RF management interface – Bit 3.

Table 5. Radio Control Interface (RCI) Signals^[a] (Cont.)

Signal Name ^[b]	Ball	Type		Voltage	Description
RCIx_MISO _n _S	T20, T3 T19, T4 Y16, Y7 Y17, Y6 Y18, Y5 Y19, Y4 Y20, Y3 J19, M5	I	-	1.8	RCIx single-ended full swing data input for the RF management interface corresponding to chip select n. This signal carries the read data from the connecting RF device in both QPSI/SPI and QPSI-Like modes.
RCIx_GPIO0	K22, K1	IO	Prog	1.8	RCIx general purpose and timed I/O for the RF management interface.
RCIx_GPIO1	K21, K2	IO	Prog	1.8	
RCIx_GPIO2	L22, K3	IO	Prog	1.8	
RCIx_GPIO3	L21, L1	IO	Prog	1.8	
RCIx_GPIO4	L20, L2	IO	Prog	1.8	
RCIx_GPIO5	L19, L3	IO	Prog	1.8	
RCIx_GPIO6	N20, N3	IO	Prog	1.8	
RCIx_GPIO7	N19, N4	IO	Prog	1.8	
RCIx_GPIO8	N18, N5	IO	Prog	1.8	
RCIx_GPIO9	P18, P5	IO	Prog	1.8	

[a] This interface should be configured as described in the *RWM6050 User Manual* to operate either in SPI mode using the single-ended signals, or in SPI-Like mode using the LVDS signals. In both modes, the data of a read transaction is carried by the single-ended signal, RCIx_MISO1_S/ RCIx_MISO0_S.

[b] RCIx implies both RCI0 and RCI1 interfaces, which are identical; ball names correspond to RCI0 and RCI1 in that order. RCI0 and RCI1 interfaces can be configured independently

Table 6. Flash SPI Boot Interface Signals

Signal Name	Ball	Type		Voltage	Description
FSPI_CLK	E21	O	-	1.8	Flash SPI clock output with a configurable frequency of up to 50MHz. This signal is tri-stated during device reset.
FSPI_CSN	E22	O	-	1.8	Flash SPI chip select. This signal is asserted low to initiate a transaction. This signal is tri-stated during device reset.
FSPI_D0	F21	IO	-	1.8	Flash SPI – data in, Bit 0. This signal carries data in bit 0. It can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.

Table 6. Flash SPI Boot Interface Signals

Signal Name	Ball	Type		Voltage	Description
FSPI_D1_DO	F22	IO	-	1.8	Flash SPI – data in, Bit 1. This signal carries: <ul style="list-style-type: none"> Data in, Bit 1, when the interface is configured to operate in dual or quad configuration, or Data out serial data This signal can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.
FSPI_D2_WPN	G21	IO	-	1.8	Flash SPI – data in, Bit 2. This signal: <ul style="list-style-type: none"> Carries data in, Bit 2, when the interface is configured to operate in quad configuration Drives the flash active-low Write-Protect signal This signal can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.
FSPI_D3_HN	G22	IO	-	1.8	Flash SPI – data in, Bit 3. This signal carries: <ul style="list-style-type: none"> Data in, Bit 3, when the interface is configured to operate in quad configuration, or Drives the flash active-low Hold signal This signal can also be configured as a GPIO with direction and values controlled by registers. This signal is tri-stated during device reset.

Table 7. Management Processor Interface Signals

Signal Name	Ball	Type		Voltage	Description
SPI Interface					
SPI_SCLK	B1	O	-	1.8	Management processor SPI clock output signal with a configurable frequency of up to 62.5MHz.
SPI_CSN	A2	O	-	1.8	Management processor SPI Chip Select. This signal is asserted low to initiate a transaction.
SPI_MISO	B2	I	-	1.8	Management processor SPI Master In Slave Output Data.
SPI_MOSI	C1	O	-	1.8	Management processor SPI Master Out Slave In Data.
UART Interface					
UART_RX	H22	I	-	1.8	Management processor UART serial data receive.
UART_TX	J22	O	-	1.8	Management processor UART serial data transmit.
UART_CTS	J21	I	PU	1.8	Management processor UART Clear-To-Send flow control signal.
UART_RTS	H21	O	-	1.8	Management processor UART Request-to-Send flow control signal.

Table 7. Management Processor Interface Signals (Cont.)

Signal Name	Ball	Type	Voltage	Description	
I2C Interface					
I2C_SCL	A20	IO	ST-OD	1.8	Management processor I ² C serial clock with a maximum frequency of 400kHz. This signal has an open-drain output and Schmitt trigger input. It requires an external pull-up resistor.
I2C_SDA	A21	IO	ST-OD	1.8	Management processor I2C serial data. This signal has an open-drain output and Schmitt trigger input. It requires an external pull-up resistor.
PWM Interface					
PWM_0	A19	O	-	1.8	Management processor – Pulse Width Modulation waveform output 0. This signal changes state: <ul style="list-style-type: none"> ▪ From high to low when an internal 32-bit counter clocked at 250MHz equals a configured value. ▪ From low to high when the 32-bit counter wraps around at a configured value.
PWM_1	B19	O	-	1.8	Management processor – Pulse Width Modulation waveform output 1. This signal changes state: <ul style="list-style-type: none"> ▪ From high to low when an internal 32-bit counter clocked at 250MHz equals a configured value. ▪ From low to high when the 32-bit counter wraps around at a configured value.

Table 7. Management Processor Interface Signals (Cont.)

Signal Name	Ball	Type	Voltage	Description
GPIO Interface				
GPIO_0	C2	IO	Prog-ST	1.8
GPIO_1	D1	IO	Prog-ST	1.8
GPIO_2	D2	IO	Prog-ST	1.8
GPIO_3	E1	IO	Prog-ST	1.8
GPIO_4	E2	IO	Prog-ST	1.8
GPIO_5	E3	IO	Prog-ST	1.8
GPIO_6	F1	IO	Prog-ST	1.8
GPIO_7	F2	IO	Prog-ST	1.8
GPIO_8	F3	IO	Prog-ST	1.8
GPIO_9	G1	IO	Prog-ST	1.8
GPIO_10	G2	IO	Prog-ST	1.8
GPIO_11	H1	IO	Prog-ST	1.8
GPIO_12	H2	IO	Prog-ST	1.8
GPIO_13	J1	IO	Prog-ST	1.8
GPIO_14	J2	IO	Prog-ST	1.8
GPIO_15	J3	IO	Prog-ST	1.8

General purpose I/Os. Directions and pull-ups/pull-downs are programmable.

Table 8. MSFE Signals

Signal Name ^[a]	Ball	Type	Voltage	Description	
MSFEx_ADC_IN	Y22, Y1	I	A	MSFEx high-speed differential ADC I-channel input. This signal can be swapped in digital domain.	
MSFEx_ADC_IP	AA22, AA1	I	A		
MSFEx_ADC_QN	AB21, AB2	I	A	MSFEx high-speed differential ADC Q-channel input. This signal can be swapped in digital domain.	
MSFEx_ADC_QP	AB20, AB3	I	A		
MSFEx_ADC_VCM	AA21, AA2	O	A	MSFEx high-speed ADC VCM output. This signal provides internally generated common-mode voltage for use with DC coupled circuits.	
MSFEx_DAC_IN	AB13, AB10	O	A	MSFEx high-speed differential DAC I-channel output. This signal can be swapped in digital domain.	
MSFEx_DAC_IP	AB12, AB11	O	A		
MSFEx_DAC_QN	AB15, AB8	O	A	MSFEx high-speed differential DAC Q-channel output. This signal can be swapped in digital domain.	
MSFEx_DAC_QP	AB14, AB9	O	A		
MSFEx_CLKOUT	AA19, AA4	O	-	1.8	MSFEx single-ended reference clock output from the integrated crystal oscillator.

Table 8. MSFE Signals (Cont.)

Signal Name ^[a]	Ball	Type		Voltage	Description
MSFEx_REFCLKN	AB19, AB4	I	CML_I	1.8	MSFEx IQ DAC and ADC differential reference clock inputs. The required typical clock frequency is 54MHz.
MSFEx_REFCLKP	AB18, AB5	I		1.8	
MSFEx_XI	AB16, AB7	I	A		MSFEx Crystal Connection. Input to high-Q integrated 54MHz crystal oscillator. This signal can be driven with a single-ended reference input clock.
MSFEx_XO	AB17, AB6	O	A		MSFEx Crystal Connection. Output from the integrated crystal oscillator.

[a] MSFEx implies both MSFE0 and MSFE1 interfaces, which are identical; ball names correspond to MSFE0 and MSFE1 in that order.

Table 9. JTAG/Test Signals

Signal Name	Ball	Type		Voltage	Description
JTAG_TCK	B21	I	ST	1.8	IEEE 1149.1/1149.6 test access port. Clock input. This signal is a Schmitt trigger input.
JTAG_TDI	C20	I	ST-PU	1.8	IEEE 1149.1/1149.6 test access port. Serial data input. This signal is a Schmitt trigger input with internal pull-up.
JTAG_TDO	B20	O	OD	1.8	IEEE 1149.1/1149.6 test access port. Serial data output.
JTAG_TMS	C21	I	ST-PU	1.8	IEEE 1149.1/1149.6 test access port. Mode select input. This signal is a Schmitt trigger input with internal pull-up.
JTAG_TRSTN	D21	I	ST-PD	1.8	IEEE 1149.1/1149.6 test access port. Reset input. This signal is a Schmitt trigger input with internal pull-down.
JTAG_SELECT	D20	I	PD	1.8	JTAG Select. Access to the JTAG TAP controller in the PCIe PHY is controlled by the state of this pin: <ul style="list-style-type: none"> ▪ 0 = PCIe TAP controller is chained in series following the boundary scan TAP controller ▪ 1 = Exclude PCIe TAP controller. Only the boundary scan TAP controller is accessible. Note: JTAG_SELECT must be set to 1 during boundary scan.

Table 10. DNC Signals

Signal Name	Ball	Description
DNC	A3, A6, A7, AA7, AA8, AA15, AA16	Do not connect signals.

2.1.2 Supply Signals

Table 11. Power Supply and Reference Signals

Signal Name	Ball	Description
VDD	R6, H7, K7, M7, P7, G8, J8, L8, N8, R8, H9, K9, M9, P9, G10, J10, L10, N10, R10, H11, K11, M11, P11, G12, J12, L12, N12, R12, H13, K13, M13, P13, J14, L14, N14, R14, H15, K15, M15, P15, G16, J16, L16, N16, R16, K17, M17, P17	These pins provide 0.9V with respect to VSS for the core digital logic.
VDDIO	D3, H3, W4, J6, L6, N6, G14, H17, L18, D19, F19, W19	These pins provide 1.8V with respect to VSSIO for the digital I/Os.
RCIO_VDDIO	U18	These pins provide 1.8V with respect to VSSIO for the digital RCIO/1 CMOS I/Os.
RCI1_VDDIO	T5	
LVDS_VDDIO	W2, M3, P4, M19, P19, W21	These pins provide 1.8V with respect to VSSIO for the RCIO/1 LVDS I/Os.
AUX_VP1	F9	This pin provides 0.9V auxiliary analog supply 1 with respect to VSS.
AUX_VPH	F7	This pin provides 1.8V auxiliary high voltage supply with respect to VSS.
AUX_VP2	E8	This pin provides 0.9V auxiliary analog supply 2 with respect to VSS.
PCIE_VP	F13	This pin provides 0.9V analog supply with respect to VSS for the PCIe.
PCIE_VPH	E10	This pin provides 1.8V analog supply with respect to VSS for the PCIe.
PCIE_VPTX	F11	This pin provide 0.9V with respect to VSS for the PCIe PHY transmit.
PLL0_DVDD	F17	This pin provide 0.9V with respect to PLL0_DVSS for the system PLL0 digital logic.
PLL1_DVDD	F14	This pin provide 0.9V with respect to PLL1_DVSS for the system PLL1 digital logic
PLL0_VDDH	D17	This pin provide 1.8V with respect to PLL0_AVSS for the system PLL0 analog circuitry
PLL0_VDDA	E17	This pin provide 0.9V with respect to PLL0_AVSS for the system PLL0 analog circuitry
PLL1_VDDH	D14	This pin provide 1.8V with respect to PLL1_AVSS for the system PLL1 analog circuitry
PLL1_VDDA	E14	This pin provide 0.9V with respect to PLL1_AVSS for the system PLL1 analog circuitry

Table 11. Power Supply and Reference Signals (Cont.)

Signal Name	Ball	Description
MSFE0_AVDD	T12, U13, V14	This pin provide 0.9V with respect to MSFE0_AVSS for the MSFE0 ADC/DAC.
MSFE0_PLL_AVDD	T16	This pin provide 0.9V with respect to MSFE0_AVSS for the MSFE0 PLL.
MSFE0_AVDDH	W15, V16, U17, W17	This pin provide 1.8V with respect to MSFE0_AVSS for the MSFE0 ADC/DAC.
MSFE0_OSC_AVDDH	T14	This pin provide 1.8V with respect to MSFE0_AVSS for the MSFE0 oscillator.
MSFE0_PLL_AVDDH	U15	This pin provide 1.8V with respect to MSFE0_AVSS for the MSFE0 PLL
MSFE1_AVDD	V9, U10, T11	This pin provide 0.9V with respect to MSFE1_AVSS for the MSFE1 ADC/DAC.
MSFE1_PLL_AVDD	T7	This pin provide 0.9V with respect to MSFE1_AVSS for the MSFE1 PLL.
MSFE1_AVDDH	U6, W6, V7, W8	This pin provide 1.8V with respect to MSFE1_AVSS for the MSFE1 ADC/DAC.
MSFE1_OSC_AVDDH	T9	This pin provide 1.8V with respect to MSFE1_AVSS for the MSFE1 oscillator.
MSFE1_PLL_AVDDH	U8	This pin provide 1.8V with respect to MSFE1_AVSS for the MSFE1 PLL
TSENSE_AVDDH	G6	This pin provide 1.8V with respect to TSENSE_AVSS for the Temperature Sensor analog circuitry.
RCI0_REF	R20	This pin provide a reference 1.2V with respect to VSSIO for the RCI0 LVDS I/Os.
RCI1_REF	R3	This pin provide a reference 1.2V with respect to VSSIO for the RCI1 LVDS I/Os.

2.1.3 Ground Signals

Table 12. Ground Signals

Signal Name	Ball	Description
VSS	B5, K6, M6, B7, E7, J7, L7, N7, R7, F8, H8, K8, M8, P8, B9, E9, G9, J9, L9, N9, R9, F10, H10, K10, M10, P10, B11, E11, G11, J11, L11, N11, R11, F12, H12, K12, M12, P12, B13, E13, G13, J13, L13, N13, R13, H14, K14, M14, P14, A15, J15, L15, N15, R15, H16, K16, M16, P16, J17, L17, N17, R17, M18, E4	These pins provide the reference shared ground for the digital core logic and PCIe.
VSSIO	A1, W1, G3, P3, W3, D4, M4, U5, H6, P6, G15, G17, K18, T18, C19, F20, M20, P20, W20, A22, W22, C17, C16, C15, H19, K19, E19, C12, D12, C11, D11, C10, D10, C9, D9, C8, D8, C7, D7, C6, D6, C5, D5, C4, E5, F6, F5, F4, G5, G4, H5, H4D13, C18, D16, D18, D15, B18, C14	These pins provide the reference shared ground for the digital and LVDS I/Os.
PLL0_DVSS	F16	This pin provides the reference ground for the system PLL0 digital logic.
PLL1_DVSS	F15	This pin provides the reference ground for the system PLL1 digital logic.
PLL0_VSSA	E16	This pin provides the reference ground for the system PLL0 analog circuitry.
PLL1_VSSA	E15	This pin provides the reference ground for the system PLL1 analog circuitry.
MSFE0_AVSS	U12, V12, W12, Y12, AA12, T13, V13, W13, Y13, AA13, U14, W14, Y14, AA14, T15, V15, Y15, U16, W16, T17, V17, AA17, W18, AA18, AA20, Y21, AB22	These pins provide the reference ground for MSFE0 analog circuitry.
MSFE1_AVSS	AB1, Y2, AA3, W5, AA5, T6, V6, AA6, U7, W7, T8, V8, Y8, U9, W9, Y9, AA9, T10, V10, W10, Y10, AA10, U11, V11, W11, Y11, AA11	These pins provide the reference ground for MSFE1 analog circuitry.
TSENSE_AVSS	G7	This pin provides the reference ground for the temperature sensor analog circuitry.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RWM6050 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 13. Absolute Maximum Ratings

Symbol ^[a]	Parameter	Minimum	Typical	Maximum	Units
Power Supplies					
VDD, PCIE_VP, PCIE_VPTX, PLLx_VDDA, MSFEx_AVDD, MSFEx_PLL_AVDD,	0.9V Nominal Rated Supplies	-0.4		1.1	V
VDDIO, LVDS_VDDIO, PCIE_VPH, PLLx_VDDH, MSFEx_AVDDH, MSFEx_OSC_AVDDH, MSFEx_PLL_AVDDH, TSENSE_AVDDH, FUSE_VDDQ,	1.8V Nominal Rated Supplies	-0.4		2.2	V
ESD					
VESD_HBM	Human Body Model Electrostatic discharge voltage JESD22-A114	2			kV
VESD_RCDM	Charge Discharge Model Electrostatic discharge voltage JESD22-C101	500			V
Thermal and Power					
T _{STG}	Storage temperature	-65		150	°C
T _{JUNCTION}	Operating temperature (junction)	-40		125	°C

[a] RC1x, PLLx and MSFEx represent RC10 / RC11, PLL0 / PLL1 and MSFE0 / MSFE1 respectively.

3.2 Recommended Operating Conditions

 Table 14. Recommended Operating Conditions^[a]

Symbol ^[b]	Parameter	Minimum	Typical	Maximum	Units
T _J	Junction temperature	-40		110	°C
VDD	Core 0.9V supply	0.8775	0.9	0.9225	V
VDDIO	Digital LVCMOS I/O 1.8V supply	1.755	1.8	1.845	V
LVDS_VDDIO	LVDS I/O 1.8V supply	1.755	1.8	1.845	V
RCI _x _REF	LVDS pads 1.2V reference voltage	1.188	1.2	1.212	V
AUX_VP1	Auxiliary 0.9V analog supply 1	0.8775	0.9	0.9225	V
AUX_VPH	Auxiliary 1.8V high voltage supply	1.71	1.8	1.89	V
AUX_VP2	Auxiliary 0.9V analog supply 2	0.8775	0.9	0.9225	V
PCIE_VP	PCIe 0.9V analog supply	0.8775	0.9	0.9225	V
PCIE_VPH	PCIe 1.8V high voltage supply	1.71	1.8	1.89	V
PCIE_VPTX	PCIe 0.9V PHY transmit supply	0.8775	0.9	0.9225	V
PLL _x _DVDD	PLL _x 0.9V digital voltage supply	0.8775	0.9	0.9225	V
PLL _x _VDDH	PLL _x 1.8V high voltage supply	1.71	1.8	1.89	V
PLL _x _VDDA	PLL _x 0.9V analog supply	0.8775	0.9	0.9225	V
MSFEx_AVDD	MSFEx ADC/DAC 0.9V analog supply	0.8775	0.9	0.9225	V
MSFEx_PLL_AVDD	MSFEx PLL 0.9V analog supply	0.8775	0.9	0.9225	V
MSFEx_AVDDH	MSFEx ADC/DAC 1.8V supply	1.71	1.8	1.89	V
MSFEx_OSC_AVDDH	MSFEx Oscillator 1.8V supply	1.71	1.8	1.89	V
MSFEx_PLL_AVDDH	MSFEx PLL 1.8V supply	1.71	1.8	1.89	V
TSENSE_AVDDH	Temperature sensor 1.8V analog supply	1.71	1.8	1.89	V

[a] Exposure to conditions outside the recommended operating conditions can affect the operation and/or reliability of the device.

[b] RCI_x, PLL_x and MSFEx represent RCI0 / RCI1, PLL0 / PLL1 and MSFE0 / MSFE1 respectively.

3.3 Supply Currents and Power

Table 15. Supply Currents and Power^[a]

Supply ^[b]	Description	Current (mA)		Voltage (V)		Power (mW)	
		Typical	Max.	Typical	Max.	Typical	Max.
Core Power							
VDD	Core supply	3000		0.9		2700.0	
VDDIO	Digital I/O supply	50		1.8		90.0	
LVDS_VDDIO	LVDS I/O supply	50		1.8		90.0	
RCI _x _REF	RCI _x LVDS pad reference	0		1.2		0	
PCIE_VP	PCIE analog supply	50		0.9		45.0	
PCIE_VPH	PCIE high-voltage supply	22		1.8		39.6	
PCIE_VPTX	PCIE PHY transmit supply	60		0.9		54.0	
AUX_VP1	Auxiliary analog supply 1	0.2		0.9		0.1	
AUX_VPH	Auxiliary high voltage supply	0		1.8		0	
AUX_VP2	Auxiliary analog supply 2	0		0.9		0	
MSFEx_AVDD	MSFEx ADC 0.9V analog supply	76		0.9		68.4	
MSFEx_PLL_AVDD	MSFEx PLL 0.9V analog supply	2.3		0.9		2.1	
MSFEx_AVDDH	MSFEx ADC 1.8V supply	62.5		1.8		112.5	
MSFEx_OSC_AVDDH	MSFEx OSC 1.8V supply	2.9		1.8		5.2	
MSFEx_PLL_AVDDH	MSFE PLL 1.8V supply	5.9		1.8		10.6	
PLL _x _VDDH	Analog PLL supply voltage	5.2		1.8		9.4	
PLL _x _VDDA	Analog PLL supply voltage	1.1		0.9		1.0	
TSENSE_AVDDH	Temperature sensor analog supply	0		1.8		0	
Total Power (W)						3.2	

[a] All power figures are estimated

[b] RCI_x, PLL_x and MSFEx represent RCI0 / RCI1, PLL0 / PLL1 and MSFE0 / MSFE1 respectively. Reported power of these domains is included twice in the total power.

3.4 Power Supply Sequencing

The voltages on any input or I/O pin cannot exceed its corresponding supply voltage during power supply ramp-up.

3.4.1 Ramp-up Time

All power supplies should ramp up with minimum rise time of 15 μ s to ensure the ESD structure remains off during power-up. The maximum time spread between the power-up times of all power supplies should not exceed 90ms.

3.4.2 Power-Up Sequencing

1. (Recommended) Power up VDDIO before VDD. All LVCMOS outputs are tri-stated when VDD is not powered up.
2. Power up LVDS_VDDIO then VDD.
3. Power up MSFEx_AVDDH, MSFEx_OSC_AVDDH, MSFEx_PLL_AVDDH first followed by VDD and then MSFEx_AVDD, MSFEx_PLL_AVDD.

4. Power up PCIE_VP, PCIE_VPTX, and PCIE_VPH in any order.
5. Power up PLLx_VDDH, PLLx_VDDA, and TSENSE_AVDDH in any order.

3.4.3 Power-Down Sequencing

1. (Recommended) Power down MSFEx_AVDD and MSFEx_PLL_AVDD first followed by VDD and then MSFEx_AVDDH, MSFEx_OSC_AVDDH, and MSFEx_PLL_AVDDH.
2. (Recommended) Power down VDD then VDDIO.
3. (Recommended) Power down VDD then LVDS_VDDIO.
4. Power down PCIE_VP, PCIE_VPTX, and PCIE_VPH in any order.
5. Power down PLLx_VDDH, PLLx_VDDA, and TSENSE_AVDDH in any order.

3.5 DC Electrical Characteristics

DC characteristics for LVCMOS and LVDS I/Os are displayed in [Table 16](#) and [Table 17](#).

3.5.1 LVCMOS I/Os

Table 16. 1.8V LVCMOS I/O DC Parameters

Parameter	Description	Minimum	Maximum	Units
V_{IL}	Input Low Voltage	-0.3	0.63	V
V_{IH}	Input High Voltage	1.17	1.98	V
V_{TLH}	Schmitt Trigger Low to High Threshold Point	0.95	1.11	V
V_{THL}	Schmitt Trigger High to Low Threshold Point	0.67	0.9	V
V_{TLHPU}	Schmitt Trigger Low to High Threshold with Pull-up Enabled	0.94	1.11	V
V_{THLPU}	Schmitt Trigger High to Low Threshold with Pull-up Enabled	0.67	0.89	V
V_{TLHPD}	Schmitt Trigger Low to High Threshold with Pull-down Enabled	0.95	1.12	V
V_{THLPD}	Schmitt Trigger High to Low Threshold with Pull-down Enabled	0.68	0.9	V
V_{OL}	Output Voltage Low At V_{OL} maximum and default drive strength: <ul style="list-style-type: none"> ▪ Nominal I_{OL} = 13 mA for SYSOSC_XO ▪ Nominal I_{OL} = 36 mA for all other LVCMOS output and bi-directional pins 		0.45	V
V_{OH}	Output Voltage High. At V_{OH} min and default drive strength: <ul style="list-style-type: none"> ▪ Nominal I_{OH} = -8.8 mA for SYSOSC_XO ▪ Nominal I_{OH} = -33 mA for all other LVCMOS output and bi-directional pins 	1.35		V
I_I	Input Leakage Current at input voltage 1.8V or 0V		± 10	μA
I_{OZ}	Tri-state Output Leakage Current at output voltage 1.8V or 0V		± 10	μA
R_{PU}	Pull-up Resistor	54k	120k	Ω
R_{PD}	Pull-down Resistor	55k	176k	Ω
C_{PIN}	Pin capacitance (typical value ~ 3pF)		10	pF

3.5.2 LVDS I/O

Table 17. LVDS I/O DC Parameters

Parameter	Description	Minimum	Typical	Maximum	Units
V_{LDVS_OH}	Output Voltage High (Rload = 100Ω)			1.475	V
V_{LDVS_OL}	Output Voltage Low (Rload = 100Ω)	0.925			V
V_{LDVS_OD}	Output Differential Voltage (Rload = 100Ω)	250		400	mV
V_{LDVS_OS}	Output Offset Voltage (Rload = 100Ω)	1.125		1.275	V
R_{LDVS_OI}	Output Impedance	40		140	Ω

3.6 LVCMOS and LVDS I/O AC Specifications

This section contains AC timing specifications and electrical characteristics for the LVCMOS and LVDS I/Os.

3.6.1 AC Timing Test Conditions

The following tables explain the test conditions for the AC timing specifications.

Table 18. LVCMOS AC Test Conditions for VDDIO = 1.8V

Parameter	
Input slew rate	2.4V/ns 10–90%
Input timing reference level	0.9V
Output reference levels	0.9V
Output load	
▪ I2C_SCL and I2C_SDA	$C_{LOAD} = 40$ pF
▪ RCI LVCMOS outputs	$C_{LOAD} = 25$ pF
▪ All other LVCMOS outputs	$C_{LOAD} = 20$ pF

Table 19. LVDS AC Test Conditions for LVDS_VDDIO = 1.8V

Parameter	
Output reference levels	1.2V
Output load	$C_{LOAD} = 25$ pF

3.6.2 Reference Clock Timing Specification

The RWM6050 contains two system PLLs that are used to generate system clocks. The reference of these two PLL can be sourced internally via an external 25MHz crystal oscillator, or via an external single-ended high quality reference clock with very low jitter.

3.6.2.1 External System Crystal Oscillator

The system external oscillator requires external components as shown in Figure 5. Exact component values in the figure depend on crystal choice and PCB layout. Reference values are provided in Table 20.

Figure 5. Circuit for the System XTAL

Keep Board Traces Short

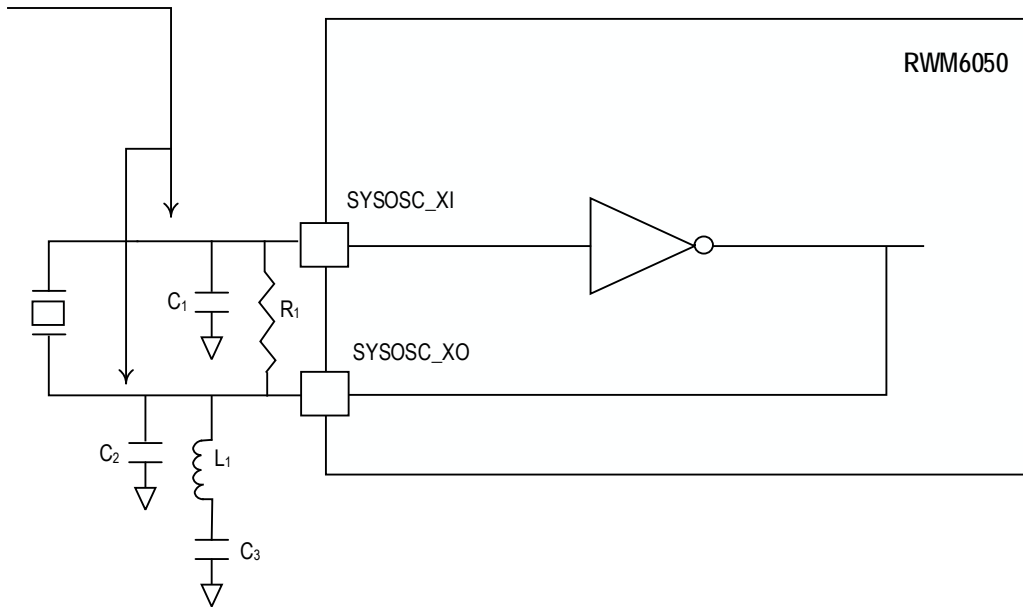


Table 20. Recommended Values for System XTAL Oscillator

XTAL ^[a]	C ₁ (pF)	C ₂ (pF)	C ₃ (pF)	L ₁ (nH)	R ₁ (Ω)
25MHz Fundamental	18pF	18pF	N/A	N/A	1M
25MHz 3rd Overtone	TBD	TBD	TBD	TBD	1M

[a] L₁ and C₃ are not required for the fundamental mode of operation.

3.6.2.2 External Single-ended System Reference Clock

A single-ended reference clock can be provided via the crystal input pin SYSOSC_XI, as displayed in Figure 6. Table 21 lists the reference clock signal timing specifications.

Figure 6. Single-ended System Reference Clock^[1]

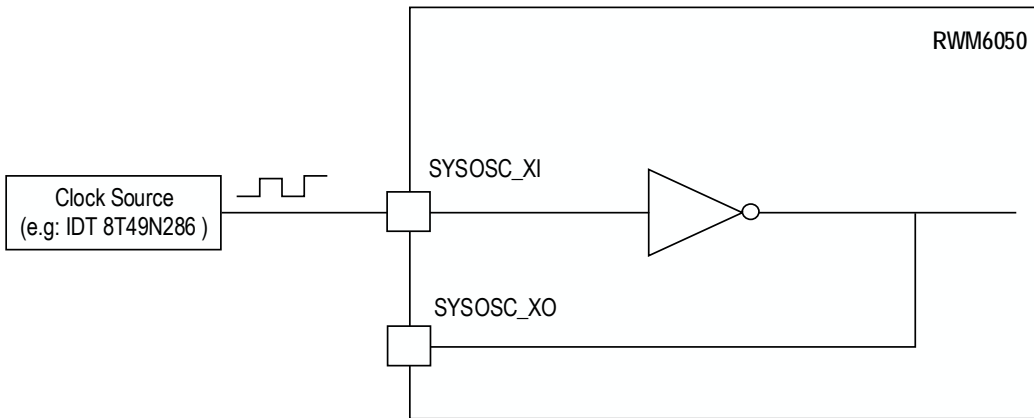


Table 21. Reference Clock Specification

Parameter	Description	Minimum	Typical	Maximum	Units
F _{SREF}	System reference frequency		25		MHz
T _{PRD}	System reference period		40		ns
T _{DUTY}	System reference duty cycle	30	50	70	%
T _J	System reference phase jitter		0.2		ps, rms
R _{Slew}	Slew Rate		0.2		V/ns

[1] Refer to the clock source device for the recommended interface to the SYSOSC_XI input.

3.6.3 Reset Signal Timing Specifications

The following table lists the reset signal, RESET_N, timing specifications.

Table 22. Reset Signal Timing Specifications^[a]

Symbol	Parameter	Minimum	Maximum	Units
T_{RST}	When asserted, RESET_N must remain asserted at least this long after power becomes valid and the clocks become stable and within the specified frequencies.	100		μs

[a] During device power-up, PCIE_PERSTN must be asserted while RESET_N is asserted.

3.6.4 JTAG Signal Timing Specifications

The following table lists the JTAG signal timing specifications.

Table 23. Debug JTAG Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
F_{DCK}	DEBUG_TCK frequency		25	MHz
T_{DCKH}	DEBUG_TCK high time	16		ns
T_{DCKL}	DEBUG_TCK low time	16		ns
T_{DCKR}	DEBUG_TCK rise time		4	ns
T_{DCKF}	DEBUG_TCK fall time		4	ns
T_{DS}	DEBUG_TMS, DEBUG_TDI set up to rising edge of JTAG_TCK	8		ns
T_{DH}	DEBUG_TMS, DEBUG_TDI hold to rising edge of JTAG_TCK	8		ns
T_{DOV}	DEBUG_TDO output valid delay from falling edge of JTAG_TCK		10	ns
T_{DOF}	DEBUG_TDO output float delay from falling edge of JTAG_TCK		10	ns
T_{DRST}	DEBUG_TRSTN minimum low time	16		ns
T_{DRSTR}	DEBUG_TRSTN ^[a] recovery time to rising edge of JTAG_TCK	8		ns

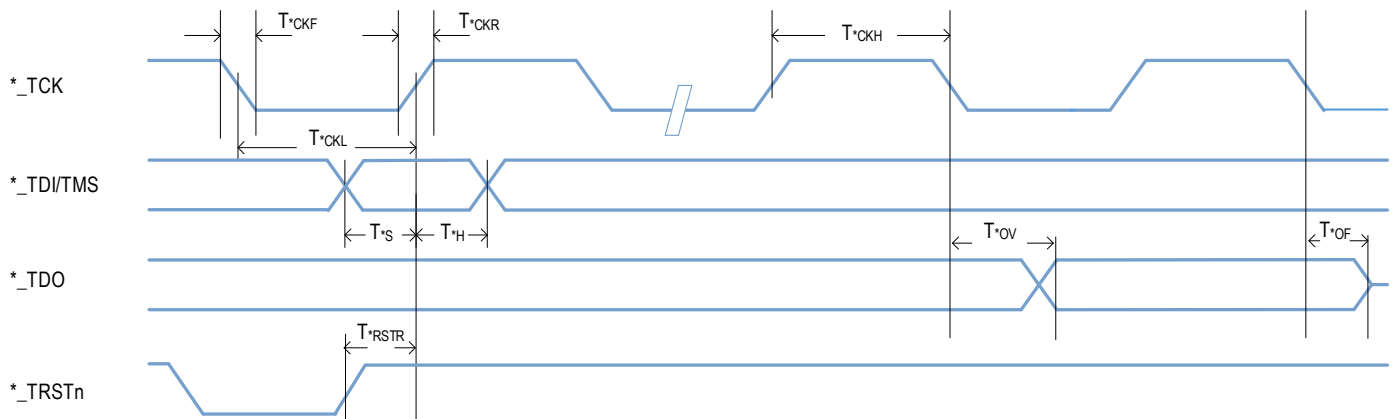
[a] DEBUG_TRSTN must be asserted while RESET_N is asserted during device power-up.

Table 24. Test JTAG Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
F_{JCK}	JTAG_TCK frequency		20	MHz
T_{JCKH}	JTAG_TCK high time	20		ns
T_{JCKL}	JTAG_TCK low time	20		ns
T_{JCKR}	JTAG_TCK rise time		5	ns
T_{JCKF}	JTAG_TCK fall time		5	ns
T_{JS}	JTAG_TMS, JTAG_TDI set up to rising edge of JTAG_TCK	10		ns
T_{JH}	JTAG_TMS, JTAG_TDI hold to rising edge of JTAG_TCK	10		ns
T_{JOV}	JTAG_TDO output valid delay from falling edge of JTAG_TCK		13	ns
T_{JOF}	JTAG_TDO output float delay from falling edge of JTAG_TCK		13	ns
T_{JRST}	JTAG_TRSTN minimum low time	16		ns
T_{JRSTR}	JTAG_TRSTN ^[a] recovery time to rising edge of JTAG_TCK	10		ns

[a] JTAG_TRSTN must be asserted while RESET_N is asserted during device power-up.

Figure 7. JTAG (Debug and Test) Signal Timings



3.6.5 Radio Control Interface Signal Timing Specifications

Table 25 and Figure 8 show the RCI LVC MOS signal timing specifications. The LVC MOS I/Os are used when the RWM6050 is configured to operate in QPSI/SPI mode.

Table 26 and Figure 9 show the RCI LVDS signal timing specifications. The LVDS I/Os are used when the RWM6050 is configured to operate in QPSI-Like mode.

Table 27/Table 28 and Figure 10/Figure 11 show the RCI LVC MOS GPIO signal timing specifications. The GPIO I/Os are used as general purpose and timed I/Os.

Table 25. RCI LVC MOS AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Units
F_{SCLK}	Clock frequency	31.42		73.33	MHz
T_{SCLK}	RCI clock period	13.64		31.83	ns
T_{CSECK}	Chip select setup time	1.5			ns
T_{CKCSD}	Chip select hold time	1.5			ns
T_{DOS}	Data out valid before clock edge	1.5			ns
T_{DOH}	Data out hold time	1.5			ns
T_{DIH}	Data in hold time	1.5			ns
T_{DIS}	Data in setup time	6.5			ns
T_{CSDES}	Chip select de-select time	9.1			ns

Figure 8. RCI LVC MOS AC Timing Diagram

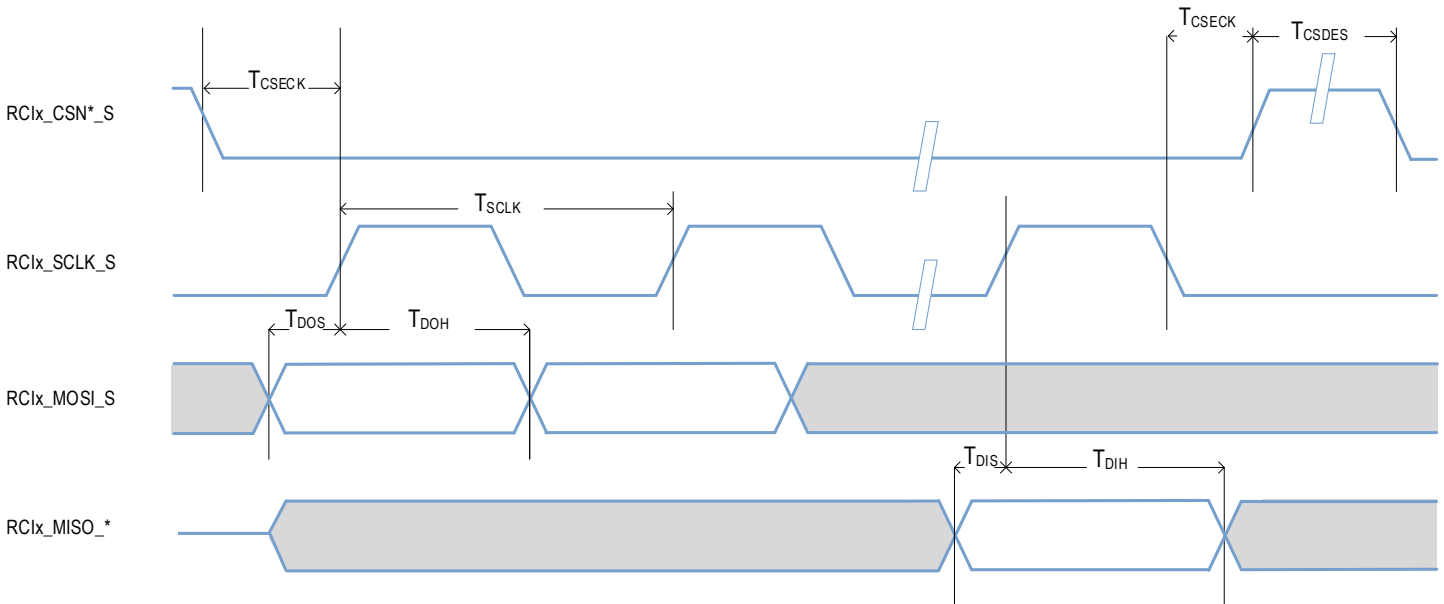


Table 26. RCI LVDS AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Units
F_{SCLK}	Clock frequency			220	MHz
T_{SCLK}	RCI clock period	4.54			ns
T_{CSV}	Chip select valid after clock edge			1.5	ns
T_{DOS}	Data out valid before clock edge	1.5			ns
T_{DOH}	Data out hold time	1.5			ns
T_{DIH}	Data in hold time	1.5			ns
T_{DIS}	Data in setup time	4.5			ns
T_{CSDES}	Chip select de-select time	4.5			ns

Figure 9. RCI LVDS AC Timing Diagram

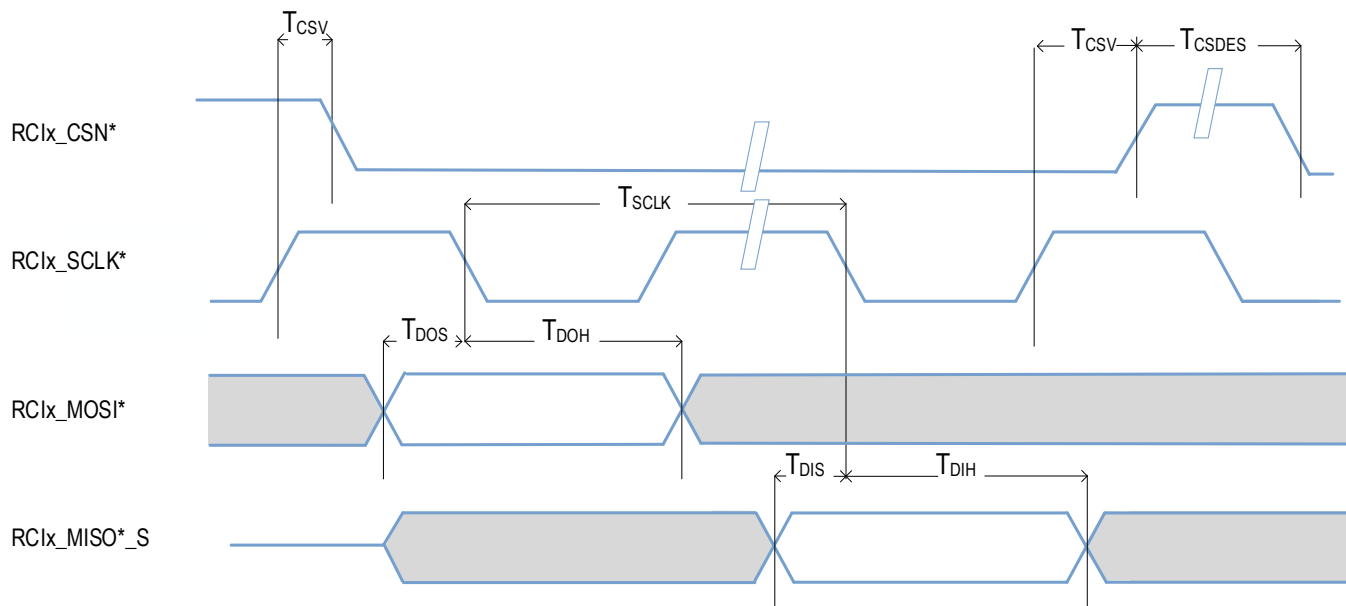


Table 27. RC1x_GPIO_n, n = 2:6, AC Timing Parameters - SDR Operation^[a]

Symbol	Description	Minimum	Typical	Maximum	Units
T _{SWID}	Strobe width	4.6			ns
T _{SR}	Strobe rise time			1.6	ns
T _{SF}	Strobe fall time			1.6	ns
T _{DVAS}	Command word valid time after strobe edge	3.5			ns
T _{DVBS}	Command word valid time before strobe edge	3.5			ns

[a] This interface is intended for Automatic Gain Control of the RF receiver.

Figure 10. RC1x_GPIO_n, n = 2:6, AC Timing Diagram - SDR Operation

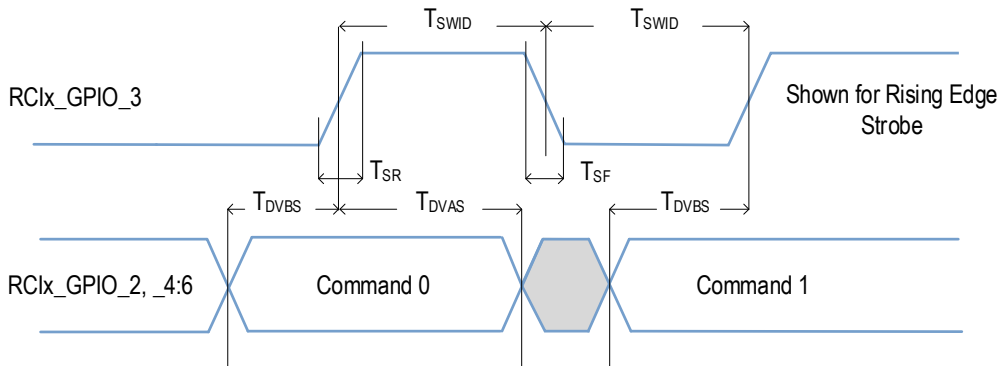
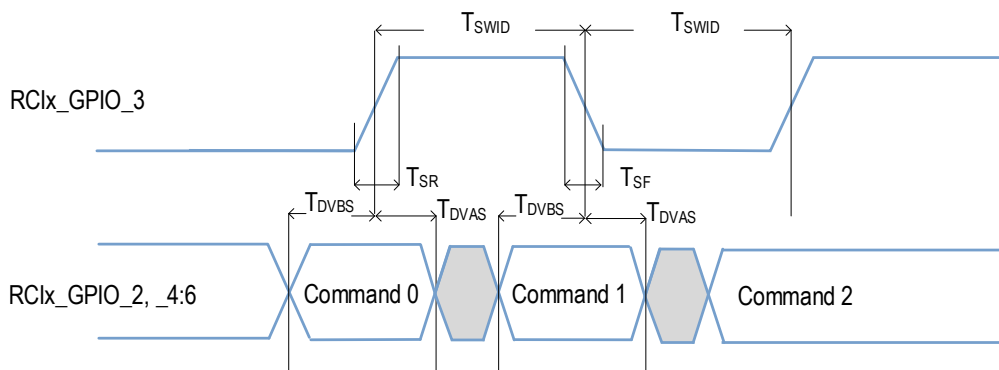


Table 28. RC1x_GPIO_n, n = 2:6, AC Timing Parameters - DDR Operation^[a]

Symbol	Description	Minimum	Typical	Maximum	Units
T _{SWID}	Strobe width	9.2			ns
T _{SR}	Strobe rise time			2	ns
T _{SF}	Strobe fall time			2	ns
T _{DVAS}	Command word valid time after strobe edge	3.5			ns
T _{DVBS}	Command word valid time before strobe edge	3.5			ns

[a] This interface is intended for Automatic Gain Control of the RF receiver.

Figure 11. RC1x_GPIO_n, n = 2:6, AC Timing Diagram - DDR Operation



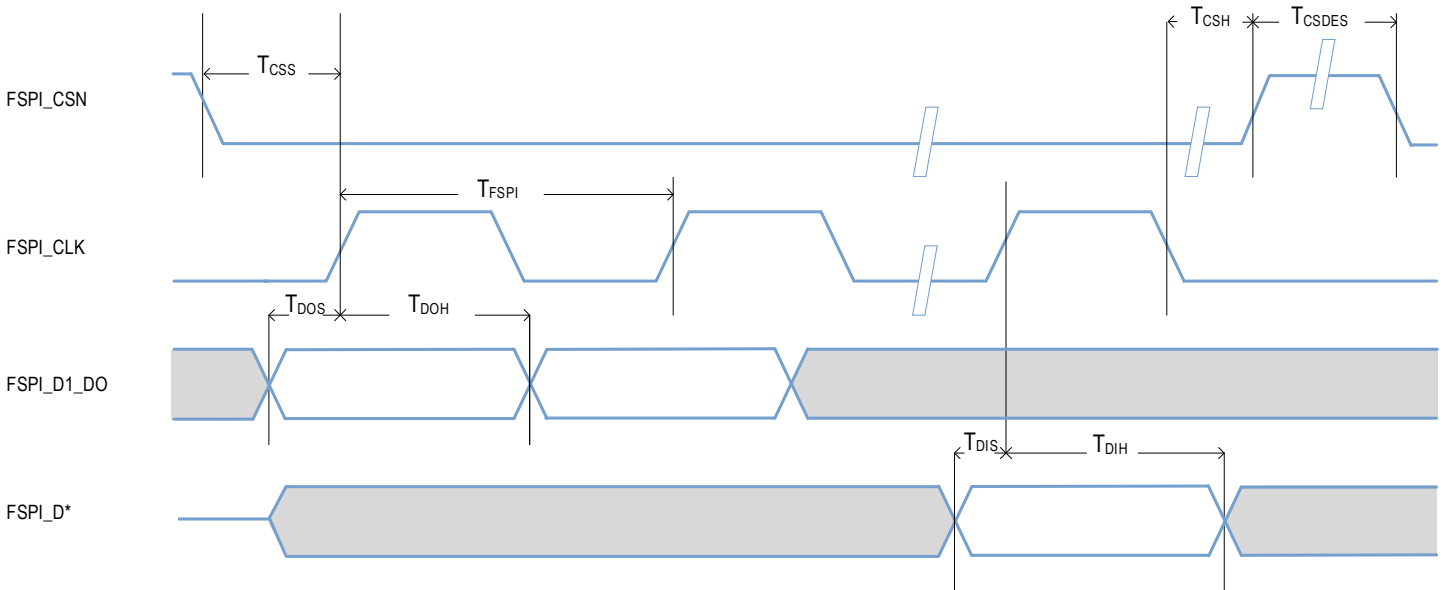
3.6.6 Flash SPI (FSPI) Boot Interface Signal Timing Specifications

The following table lists the Flash SPI Interface signal timing specifications as shown in [Figure 12](#).

Table 29. FSPI Interface AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Units
F_{FSPI}	FSPI_CLK Clock frequency			50	MHz
T_{FSPI}	FSPI_CLK clock period	20			ns
T_{CSS}	Chip select setup time	TBD			ns
T_{CSH}	Chip select hold time	TBD			ns
T_{CSDES}	Chip select de-select time	TBD			ns
T_{DOS}	Data out setup time	TBD			ns
T_{DOH}	Data out hold time	TBD			ns
T_{DIH}	Data in hold time	TBD			ns
T_{DIS}	Data in setup time	TBD			ns

Figure 12. FSPI AC Timing Diagram



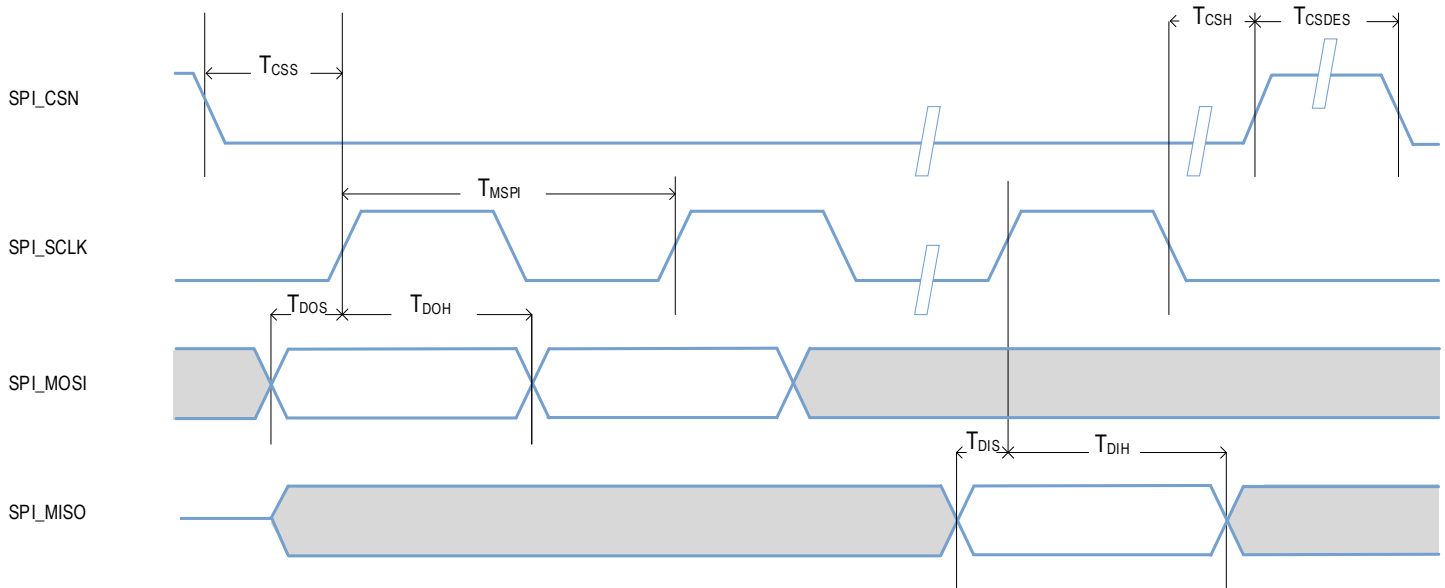
3.6.7 System SPI Interface Signal Timing Specifications

The following table lists the System SPI Interface signal timing specifications as shown in Figure 13.

Table 30. System SPI Interface AC Timing Parameters

Symbol	Description	Minimum	Typical	Maximum	Units
F_{MSPI}	SPI_SCLK Clock frequency			62.5	MHz
T_{MSPI}	SPI_SCLK clock period	16			ns
T_{CSS}	Chip select setup time	TBD			ns
T_{CSH}	Chip select hold time	TBD			ns
T_{CSDES}	Chip select de-select time	TBD			ns
T_{DOS}	Data out valid before clock edge	TBD			ns
T_{DOH}	Data out hold time	TBD			ns
T_{DIH}	Data in hold time	TBD			ns
T_{DIS}	Data in setup time	TBD			ns

Figure 13. System SPI AC Timing Diagram



3.6.8 I²C Interface Signal Timing Specifications

The following table lists the I²C Interface signal timing specifications as shown in [Figure 31](#).

Table 31. I²C Interface Signal Timing Specifications

Symbol	Description ^[a]	Standard Mode		Fast Mode		Units
		Minimum	Maximum	Minimum	Maximum	
F _{SCL}	I2C_SCL clock frequency	0	100		400	kHz
T _{LO}	I2C_SCL clock low time ^{[b],[c]}	4.7		1.3		μs
T _{HI}	I2C_SCL clock high time ^{[b],[c]}	4.0		0.6		μs
T _{HD}	I2C_SDA hold time ^[c]	[d]	3.45	[d]	0.9	μs
T _{SD}	I2C_SDA setup time ^[c]	250		100		ns
T _{SR}	Rise time of I2C_SCL and I2C_SDA ^[c] (30–70%)		1000	20 ^[e]	300 ^[d]	ns
T _{SF}	Fall time of I2C_SCL and I2C_SDA ^[c] (70–30%)		300	6.5 ^[f]	300	ns
T _{BF}	Bus free time between STOP and START condition ^[c]	4.7		1.3		μs
T _{HSTRT}	Hold time (repeated) START condition ^{[c],[g]}	4.0		0.6		μs
T _{SSSTRT}	Setup time for repeated START condition ^[c]	4.7		0.6		μs
T _{SSSTP}	Setup time for STOP condition ^[c]	4.0		0.6		μs
T _{SPK}	Pulse width of spikes that must be suppressed by the input filter			0	50	ns

[a] An external pull-up resistor is required for specification compliance. Input reference levels are set as 30% and 70% of VDDIO.

[b] Not tested.

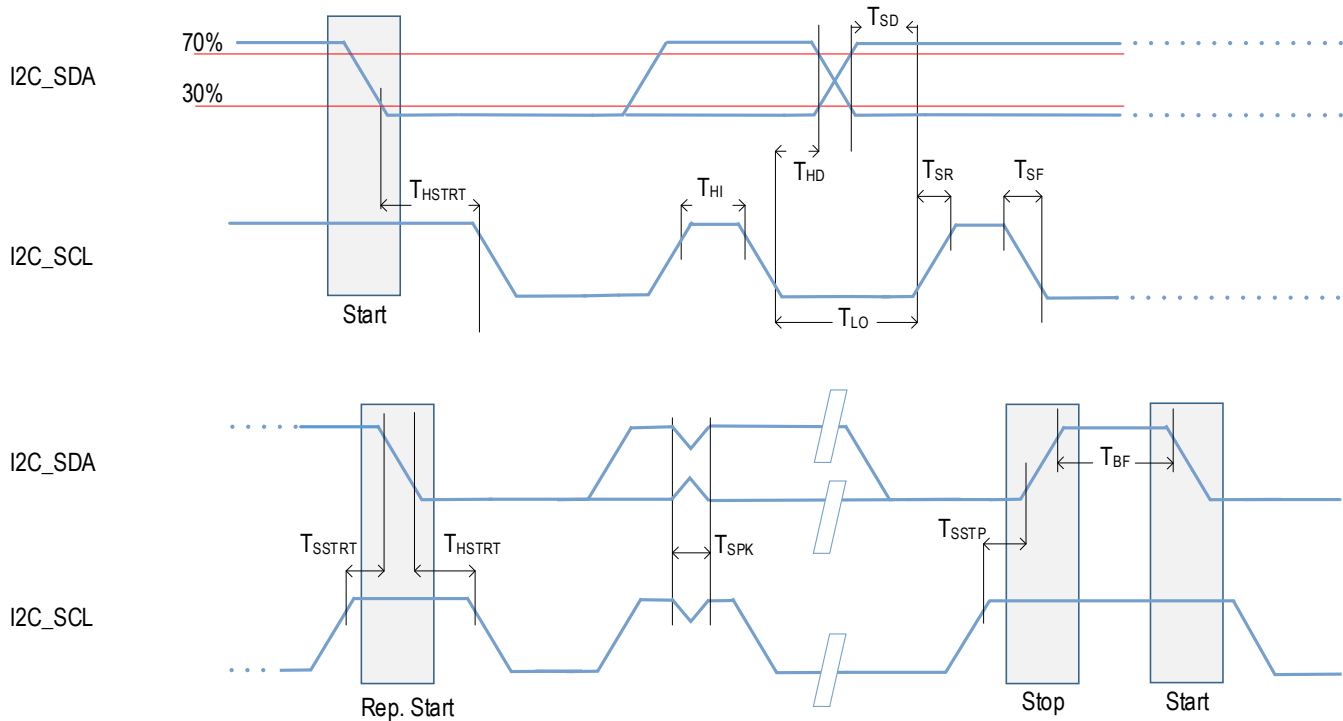
[c] See timing diagram in [Figure 14](#).

[d] When the RWM6050 drives I2C_SDA, it provides 300ns of hold time. When an external device drives I2C_SDA, it must provide a hold time of at least 300ns for I2C_SDA regarding V_{IH} min of the I2C_SCL.

[e] $20 \leq 0.85 \times R_{load}(k\Omega) \times C_{bus}(pF) \leq 300$.

[f] $C_{bus} \geq 40$ pF.

[g] After this period, the first clock pulse is generated.

Figure 14. I²C AC Timing Diagram


3.7 Mixed Signal Front End Interface Characteristics

The RWM6050 Mixed Signal Front End (MSFE) includes integrated ADC and DAC for signal conversion and an integrated PLL to provide the required sample clock. The reference clock for the PLL is provided either by the RF transceiver or a common external temperature compensated Crystal Oscillator (TCXO).

3.7.1 MSFE ADC Specifications

The ADC can be AC or DC coupled. The target configuration for the RWM6050 is to use DC coupling since this reduces the time constants associated with DC offset changes and AC coupling. In this configuration, the ADC provides a common mode output voltage as a reference.

The characteristic of the ADCs is given in [Table 32](#). The ADC input range can be configured as shown in [Table 33](#).

Table 32. ADC Characteristics

Parameter	Minimum	Typical	Maximum	Units
Number of bits		7		
Effective number of bits		6 ^[a]		
Sample rate			3.52	Gsps
Input full scale range (Typical)	290		690	Vppd
Full scale input at 0.575 Vppd typical	0.51	0.575	0.64	Vppd
Input common mode	0.4	0.6	0.7	V
Input capacitance to ground		0.3	0.4	pF
Differential input impedance	7	8	9	kΩ
Integral non linearity	-1.2		1.2	LSB

Table 32. ADC Characteristics (Cont.)

Parameter	Minimum	Typical	Maximum	Units
Differential non linearity	-1		1	LSB
SNR at 1.4GHz, -1dBfs	36	39		dBc
SINAD at 1.4GHz, -1dBfs	36	37		dBc
SFDR at 1.4GHz, -1dBfs	42	53		dBc
Aperture jitter		200	400	fs rms
IQ gain mismatch	-1.2		1.2	%
Aperture timing mismatch	-10		10	ps

[a] ENOB may be slightly under 6 bits under -20°C operating temperature.

Table 33. ADC Full-scale Input Configuration

Setting	Typical fsd	Units
1	290	mVppd
2	345	mVppd
3	499	mVppd
4	460	mVppd
5	515	mVppd
6	575	mVppd
7	630	mVppd
8	690	mVppd

3.7.2 MSFE DAC Specifications

The RWM6050 provides a 100 Ω on-chip output load to convert the current from the current-steering DAC to voltage. The DAC characteristics are listed in [Table 34](#).

Table 34. IQ DAC Characteristics

Parameter	Minimum	Typical	Maximum	Units
Number of bits		7		
Effective number of bits		6		
Sample rate		3.52		Gsps
Output full scale range (nominal)	1.84		5.0	mA
Full scale output at 5mA setting	4.75	5	5.25	mA
Gain adjustment resolution (per step)	48	50	52	μ A
On-chip Output load (single ended to ground)		100		Ω
Output compliance			0.25	V
Integral non linearity	-1		1	LSB
Differential non linearity	-1		1	LSB
SNR at 800 MHz, -1dBfs	37	38		dBc
SINAD at 800 MHz, -1dBfs	35	36		dBc
SFDR at 800 MHz, -1dBfs	36	39		dBc
Aperture jitter			700	fs rms
IQ gain mismatch	-2		2	%
Aperture timing mismatch	-6		6	ps

3.7.3 MSFE Reference Clock

The integrated PLL is used to generate the 3.52GHz ADC and DAC sample clocks. The reference clock for the MSFE PLL can be sourced via an external CML differential reference input, via a CMOS external single-ended reference input, or via an external crystal oscillator. The two MSFE instances have independent clocking options. The specifications of the MSFE reference clock are listed in [Table 35](#).

Table 35. MSFE Reference Clock Specifications

Parameter	Minimum	Typical	Maximum	Units
MSFEx_REFCLKN/MSFEx_REFCLKP Differential CML Reference Clock				
Reference clock frequency ^[a]		54		MHz
Reference clock duty cycle	40		60	%
CML Ref Clock Common Mode	0.3		0.7	V
CML Ref Clock Input Amplitude	0.6		2	V p-p diff
Differential Reference Load Resistance ^[b]		100		Ω
MSFEx_XI Single-ended Reference				
Voltage Swing Level ^[c]		0.9	0.99	V
Reference clock frequency ^[a]		54		MHz

[a] Required to meet jitter specifications.

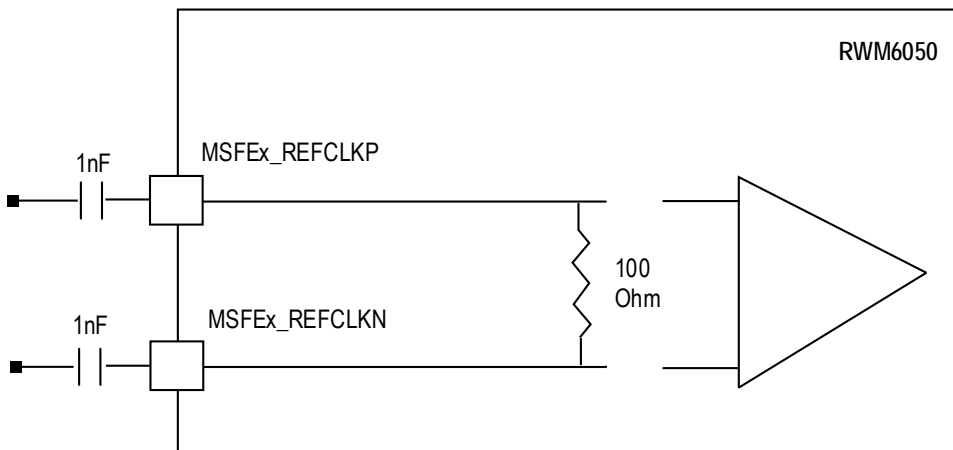
[b] Between MSFEx_REFCLKN and MSFEx_REFCLKP.

[c] Refer to [Table 36](#).

3.7.3.1 MSFE Differential Reference Clock

AC coupling capacitors should be used with an external differential reference, as displayed in [Figure 15](#).

Figure 15. Differential MSFE Reference Clock with AC Coupling - An Example



3.7.3.2 Single-ended MSFE Reference Clock

The MSFE single-ended reference clock requires external components as shown in Figure 16. Exact component values in Figure 16 depend on PCB layout. Reference values are given in Table 36.

Figure 16. Single-ended MSFE Reference Clock Coupling

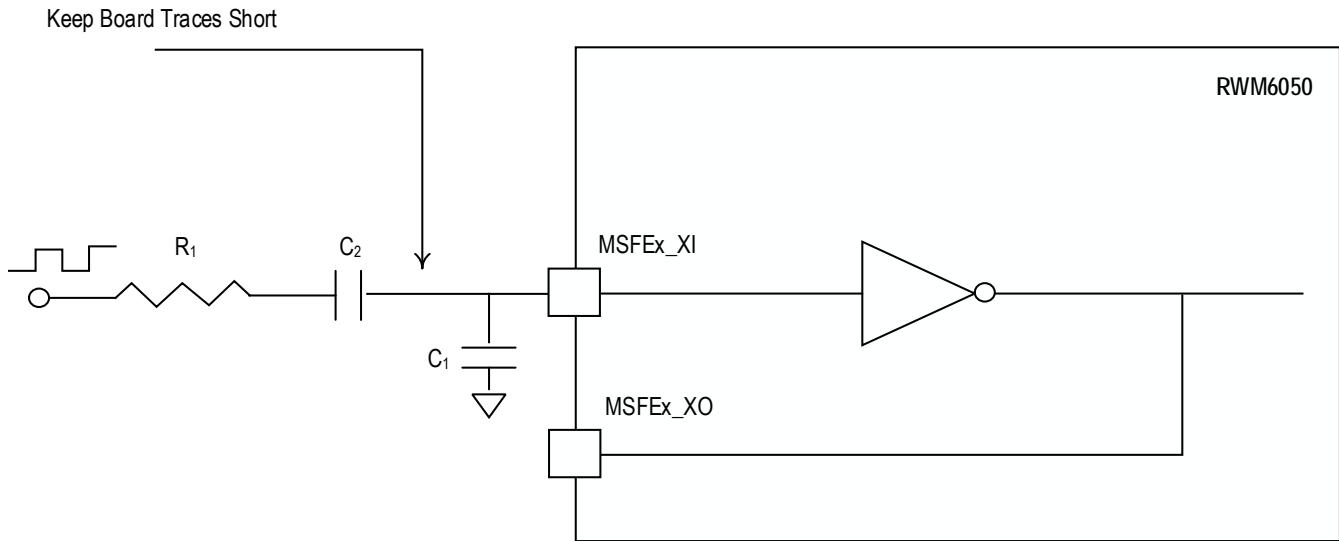


Table 36. Recommended Values for Single-ended MSFE Reference Clock Coupling

Vpk-pk Square (V)	C1 (pF)	C2 (pF)
0.9 ±10%	13	5.1
1.8 ±10%	27	5.1
2.5 ±10%	36	5.1

3.7.3.3 MSFE Crystal Oscillator

The MSFE external oscillator requires external components as shown in Figure 17. Exact component values in Figure 17 depend on crystal choice and PCB layout. Reference values are given in Table 37.

Figure 17. Circuit for the MSFE XTAL

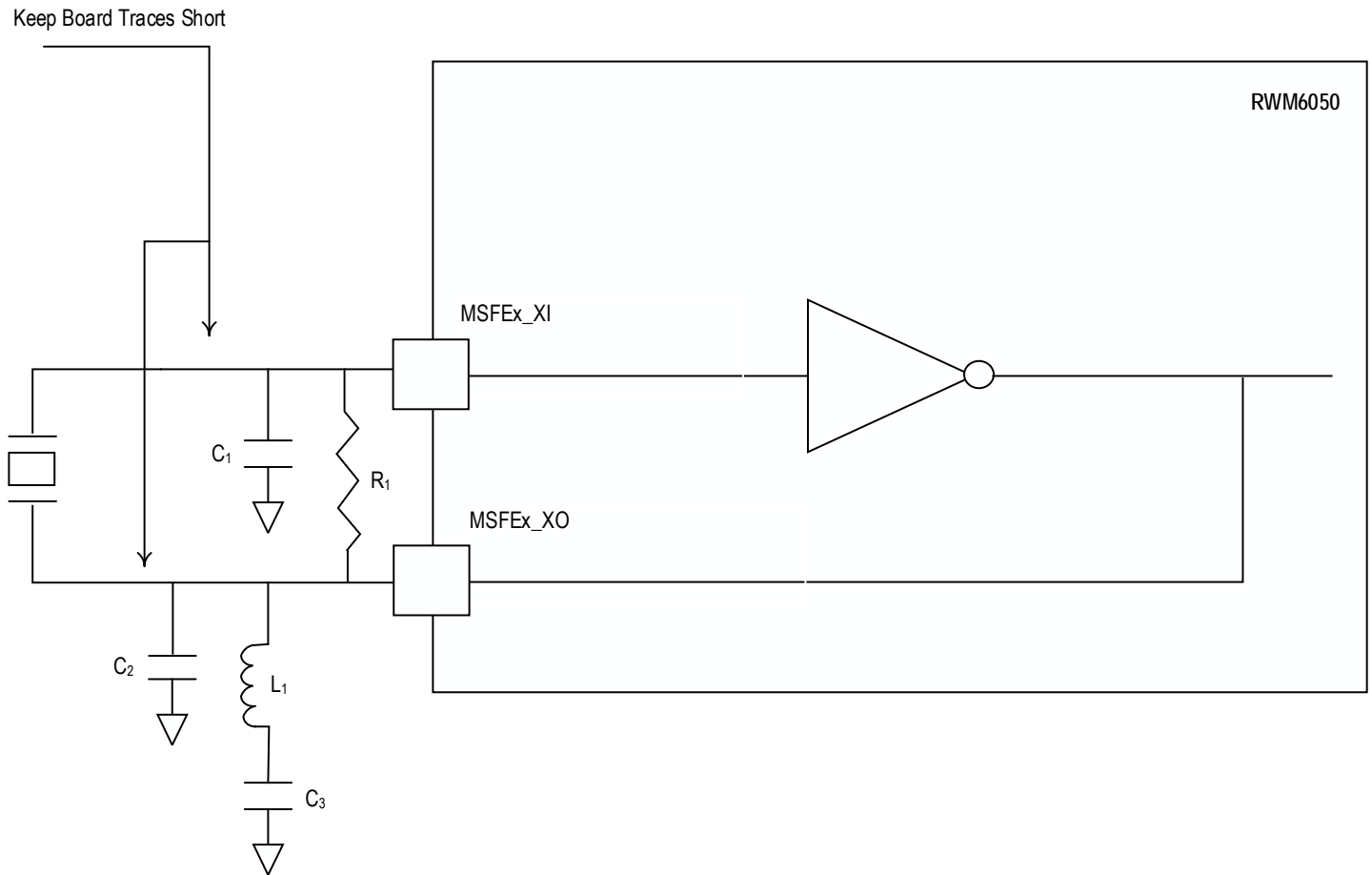


Table 37. Recommended Values for MSFE XTAL Oscillator

XTAL ^[a]	C ₁ (pF) ^[b]	C ₂ (pF)	C ₃ (pF) ^[c]	L ₁ (nH) ^[d]	R ₁ (Ω)
54MHz Fundamental ^[e]	13pF	25pF	N/A	N/A	1M
54MHz 3rd Overtone	18pF	39pF	1000	680	1M

[a] Start-up time is 10ms worst case.

[b] C₁ and C₂ should be ceramic NP0 or similar.

[c] C₃ can be a lower grade such as X7R with relaxed tolerance.

[d] L₁ needs to provide the appropriate resonance to maintain the oscillation and typically a tolerance better than ±5% is required.

[e] L₁ and C₁ are not required for the fundamental mode of operation.

3.7.4 MSFE External Matching Recommendations

The common mode voltage, AC peak-to-peak differential swing voltage, and impedance must be satisfied at both ends of a differential interconnect. High-frequency behavior of the interconnect can also be affected by the following interconnect defects:

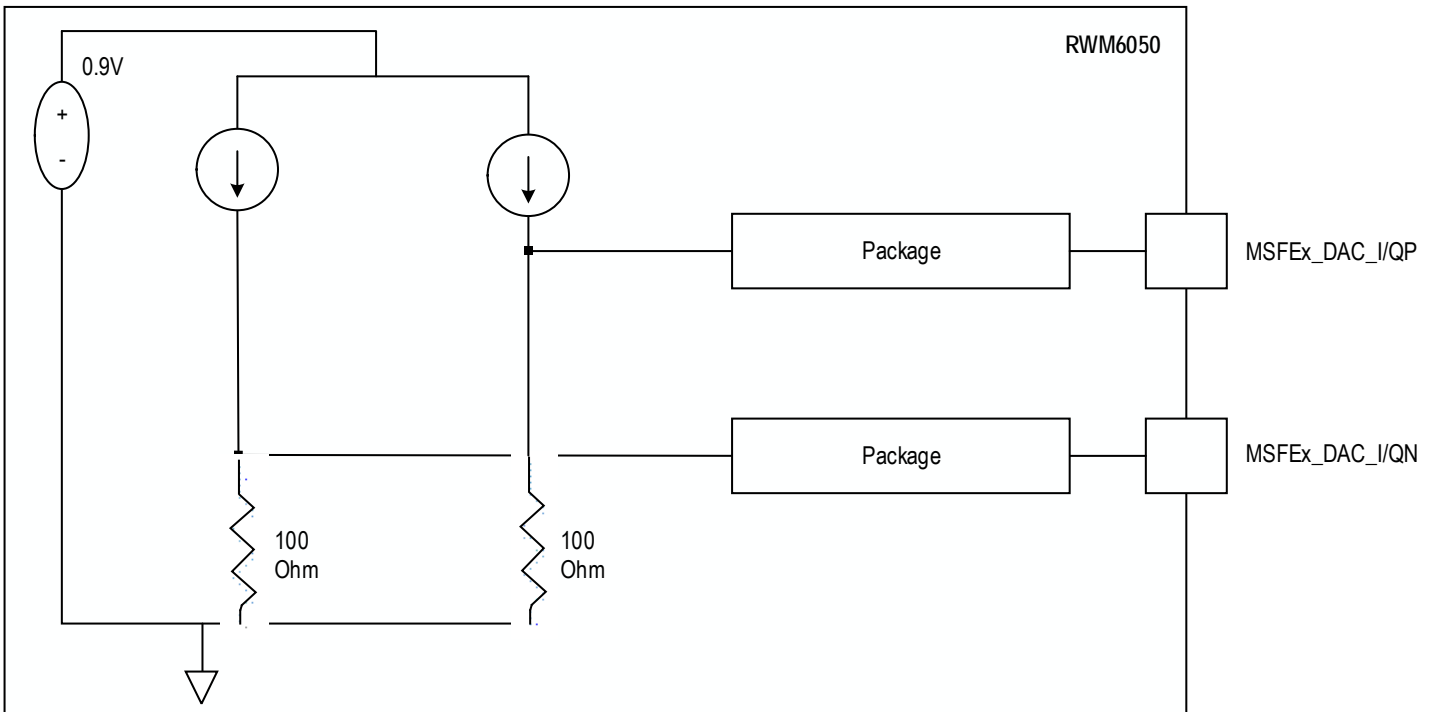
- Source and load impedance mismatch to transmission lines (tolerances in chip resistor components and PCB trace geometry)
- Stubs in the line
- Mismatch in line length within a differential pair or between I and Q pairs
- Impedance discontinuities caused by chip packages, discrete components, connectors, and test points

3.7.4.1 DAC Considerations

Each DAC current output is internally connected to ground through a load inside the RWM6050, as well as through any external termination loads. The maximum voltage developed by the output current through these load resistances must be maintained within the DAC output compliance voltage for DAC specifications to be met. The maximum DAC output currents are programmable.

The equivalent circuit for the MSFE DAC outputs is displayed in [Figure 18](#).

Figure 18. Equivalent Circuit for MSFE DAC Outputs^[1]



[1] IDT will provide a model that includes package parameters.

3.7.4.2 ADC Considerations

The ADC nominal full-scale swing can be reduced using the programmable reference voltage. There is an internal 100Ohm termination. In addition, there is internal DC biasing available for use when the ADC inputs are AC coupled.

In DC coupled mode of operation, the common-mode input voltage is critical, and an external buffer may be required to adjust the common-mode voltage reference output from the RF device. LTC6409 and ADL5565 are examples of usable buffer/amplifier devices.

The equivalent circuit for the MSFE ADC inputs in DC and AC coupled operations is displayed in [Figure 19](#) and [Figure 20](#).

Figure 19. Equivalent Circuit for MSFE ADC Inputs – DC Coupled^[1]

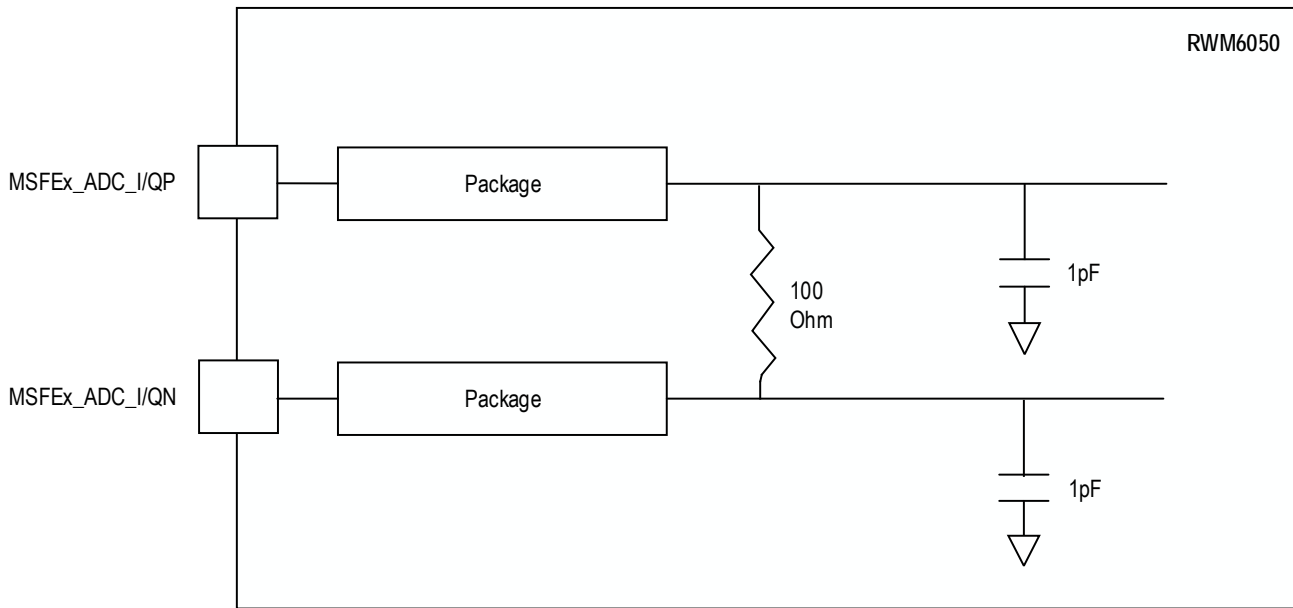
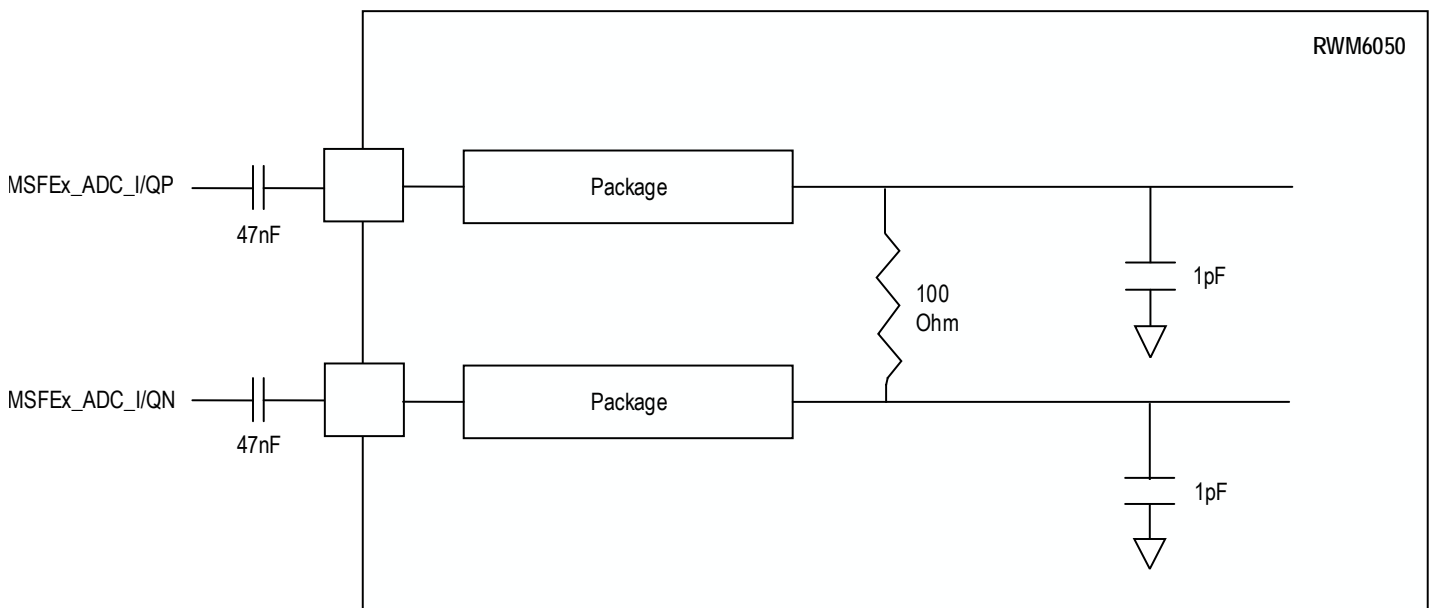


Figure 20. Equivalent Circuit for MSFE ADC Inputs – AC Coupled



3.8 PCIe Interface Characteristics

3.8.1 PCIe Reference Clock

The PCIe PHY supports a 100MHz input clock. The PCIe reference clock can be spread. If the reference clock provided to the PHY is spread for EMI purposes, both ends of the link must be spread synchronously.

When routing the reference clock from an off-chip source, terminated and unterminated clocks can both be used. With terminated clocks, a 50Ω termination resistor should be soldered on the board close to the RWM6050, preventing clock reflections. If the board clocks are unterminated, the clock's signal level doubles as it hits the high-impedance input of the RWM6050 reference clock inputs. This effect can be used to provide a clean clock to the PHY, but care should be taken to ensure that the signal swing of the reference clock is not too high after doubling the amplitude.

The reference clock inputs, PCIE_CLKP/PCIE_CLKN, are differential. If the reference clock requirements are met with a single-ended input clock, tie the unused reference input low or high. [Table 38](#) lists the PCIe PHY reference clock requirements.

Table 38. PCIe PCIE_CLKP/PCIE_CLKN Requirements

Description	Minimum	Typical	Maximum	Units
Reference clock frequency		100		MHz
Reference clock frequency offset	-300		300	ppm
Reference clock cycle-to-cycle jitter ^[a]			150	ps
Reference clock duty cycle	40		60	%
Common mode input level - Differential inputs	0		PCIE_VP	V
Differential input swing ^[b]	0.3			V p-p
Single ended input logic low	-0.3		0.3	V
Single-ended input logic high	PCIE_VP - 0.3		PCIE_VP + 0.3	V
Input edge rate	0.6			V/ns
Reference clock skew			200	ps

[a] Deterministic Jitter across all frequencies.

[b] Total input swing should be between -0.3V and PCIE_VP + 0.3V.

3.8.2 PCIe Differential Receiver and Transmitter Specifications

The RWM6050's SerDes logic fully complies to the *PCI Express Base Specification (Rev. 2.1)*. This section provides those specifications for reference purposes only. For complete requirements, see the specification.

3.8.2.1 PCIe Differential Receiver Specifications

Table 39 lists the main electrical characteristics for the PCIe differential receivers in the RWM6050. Parameters are defined separately for 2.5 and 5.0Gbps. For more information, see Section 4.3.3.4/Table 4-12 in the *PCI Express Base Specification (Rev. 2.1)*.

Table 39. PCIe Differential Receiver Specifications

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
UI	Unit interval	399.88	400.12	199.94	200.06	ps
$V_{RX-DIFF-PP-CC}$	Differential Rx peak-peak voltage					
	▪ Common reference clock Rx architecture	0.175	1.2	0.120	1.2	V
	▪ Data clocked Rx architecture	0.175	1.2	0.100	1.2	V
T_{RX-EYE}	Receiver eye time opening	0.40	-	N/A	-	UI
$T_{RX-TJ-CC}$	Maximum Rx inherent timing error					
	▪ Common reference clock Rx architecture	N/A	-	-	0.40	UI
	▪ Data clocked Rx architecture	N/A	-	-	0.34	UI
$T_{RX-DJ-DD-CC}$	Maximum Rx inherent deterministic timing error					
	▪ Common reference clock Rx architecture	N/A	-	-	0.30	UI
	▪ Data clocked Rx architecture	N/A	-	-	0.24	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time delta between median and deviation from median	-	0.3	Not specified		UI
$T_{RX-MIN-PULSE}$	Minimum width pulse at Rx	Not specified		0.6	-	UI
$V_{RX-MAX-MIN-RATIO}$	Minimum/Maximum pulse voltage on consecutive UI	Not specified		-	5	--
$RL_{RX-DIFF}$	Rx package + Si differential return loss					
	▪ 0.05–1.25 GHz	10	-	10	-	dB
	▪ 1.25–2.5 GHz	10	-	8	-	
RL_{RX-CM}	Common mode Rx return loss	6	-	6	-	dB
Z_{RX-DC}	Receiver DC common mode impedance	40	60	40	60	W
$Z_{RX-DIFF-DC}$	DC differential impedance	80	120	Not specified		W
$V_{RX-CM-AC-P}$	Rx AC common mode voltage	-	150	-	150	mV
$Z_{RX-HIGH-IMP-DC-POS}$	DC input common mode input impedance for positive voltage during reset or power down	50k	-	50k	-	W

Table 39. PCIe Differential Receiver Specifications (Cont.)

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
$Z_{RX-HIGH-IMP-DC-NEG}$	DC input common mode input impedance for negative voltage during reset or power down	1.0k	-	1.0k	-	W
$V_{RX-IDLE-DET-DIFF-p}$	Electrical idle detect threshold	65	175	65	175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical Idle enter detect threshold integration time	-	10	-	10	ms
$L_{RX-SKEW}$	Lane-to-lane skew	-	20	-	8	ns

3.8.2.2 PCIe Differential Transmitter Specifications

Table 40 lists the main electrical characteristics for the PCIe differential transmitters in the RWM6050. Parameters are defined separately for 2.5 and 5.0Gbps. For more information, see Section 4.3.3.5/Table 4-9 in *PCI Express Base Specification (Rev. 2.1)*.

Table 40. PCIe Differential Transmitter Specifications

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
UI	Unit interval	399.88	400.12	199.94	200.06	ps
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8	1.2	0.8	1.2	V
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	0.4	1.2	0.4	1.2	V
$V_{TX-DE-RATIO-3.5DB}$	Tx de-emphasis level ratio	3.0	4.0	3.0	4.0	dB
$V_{TX-DE-RATIO-6DB}$	Tx de-emphasis level ratio	N/A	N/A	5.5	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width	Not specified		0.9	-	UI
T_{TX-EYE}	Transmitter eye including all jitter sources	0.75	-	0.75	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	0.125	Not specified		UI
$T_{TX-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz	Not specified		-	0.15	UI
$T_{TX-LF-RMS}$	TX RMS jitter < 1.5 MHz	Not specified		3.0	-	ps, rms
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	0.125	-	0.15	-	UI
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	Not specified		-	0.1	UI
$RL_{TX-DIFF}$	Tx package + Si differential return loss					
	<ul style="list-style-type: none"> ▪ 0.05–1.25GHz ▪ 1.25–2.5GHz 	10	-	10	-	dB
RL_{TX-CM}	Tx package + Si common mode return loss	6	-	6	-	dB
$Z_{TX-DIFF-DC}$	DC differential Tx impedance	80	120	-	120	W

Table 40. PCIe Differential Transmitter Specifications (Cont.)

Symbol	Parameter	2.5 Gbps		5.0 Gbps		Unit
		Min.	Max.	Min.	Max.	
$V_{TX-CM-AC-PP}$	Tx AC common mode voltage					
	▪ 5.0Gbps	Not specified		-	100	mV
	▪ 2.5Gbps	20	-	Not specified		mV
$I_{TX-SHORT}$	Transmitter short-circuit current limit	-	90	-	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0	3.6	0	3.6	V
$V_{TX-CM-DC-ATIVE-IDLE-DELTA}$	Absolute delta of DC common-mode voltage during L0 and Electrical Idle	0	100	0	100	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between the differential outputs	0	25	0	25	mV
$V_{TX-IDLE-DIFF_AC-p}$	Electrical idle differential peak output voltage	0	20	0	20	mV
$V_{TX-IDLE-DIFF_DC}$	DC electrical idle differential output voltage	Not specified		0	5	mV
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	-	600	-	600	mV
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	20	-	20	-	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an EIOS	-	8	-	8	ns
$T_{TX-IDLE-SET-TO-DIFF-DATA}$	Maximum time to transition to valid differential signaling after leaving electrical idle	-	8	-	8	ns
$T_{CROSSLINK}$	Cross-link random timeout	-	1	-	1	ms
$L_{TX-SKEW}$	Lane-to-lane output skew	-	500 ps + 2 UI	-	500 ps + 2 UI	ps
C_{TX}	AC coupling capacitor	75	200	75	200	nF

4. System Clocking

4.1 System Oscillator

The RWM6050 contains a single 25MHz system XTAL oscillator which provides the reference clock to the two system PLLs.

- When using a resonant crystal, it is connected to SYSOSC_XI and SYSOSC_XO.
- When using a crystal oscillator, it is connected to SYSOSC_XI, and SYSOSC_XO is left unconnected.

4.2 System PLLs

The RWM6050 contains two system PLLs, used to generate all clocks for the system with the exception of the MSFE and PCIe interfaces. The PLL supplies should be separated from the other, noisier, supplies in the board. These supplies should be decoupled close to the respective IC power pins.

4.3 PHY Clocks

The PHY allows considerable flexibility for the RF reference clocks. There must be a single common frequency reference for both the RF device and the RWM6050 PHY. The PHY contains a high-Q crystal oscillator that can generate a frequency reference with low jitter from either a fundamental or third overtone crystal. Alternatively, the PHY may use a frequency reference from an external source or the RF device itself. An external source would be required if fine frequency control is required. The following diagrams show some possible examples.

Figure 21. PHY Clocks – RWM6050 Master, RF Slave

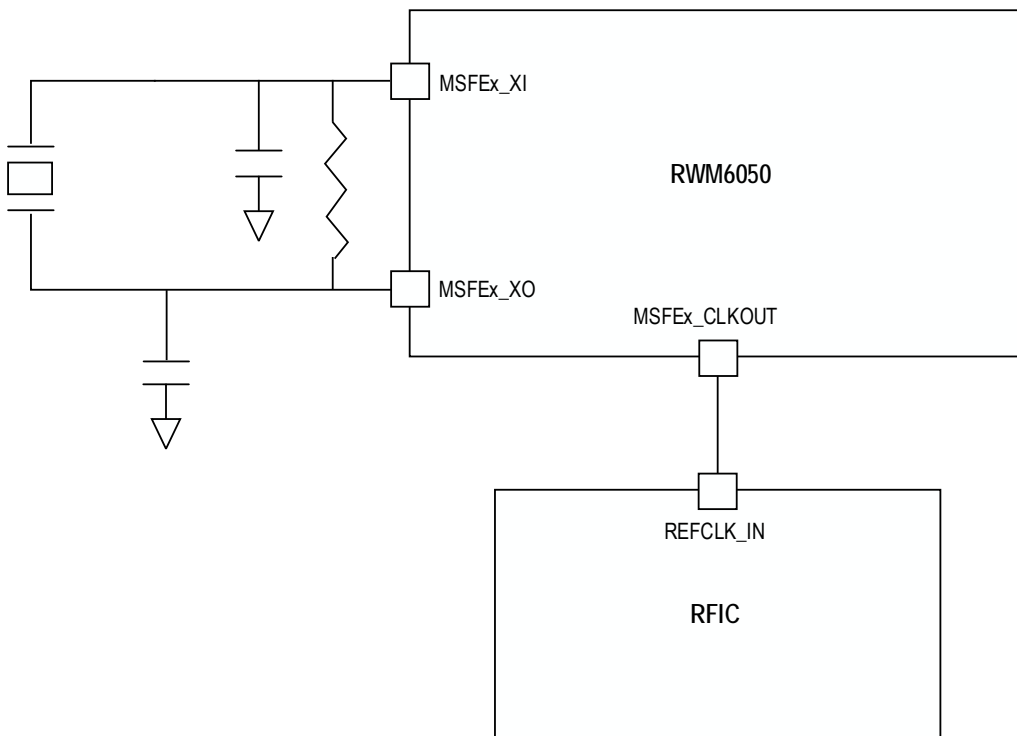


Figure 22. PHY Clocks - RF Master, RWM6050 Slave

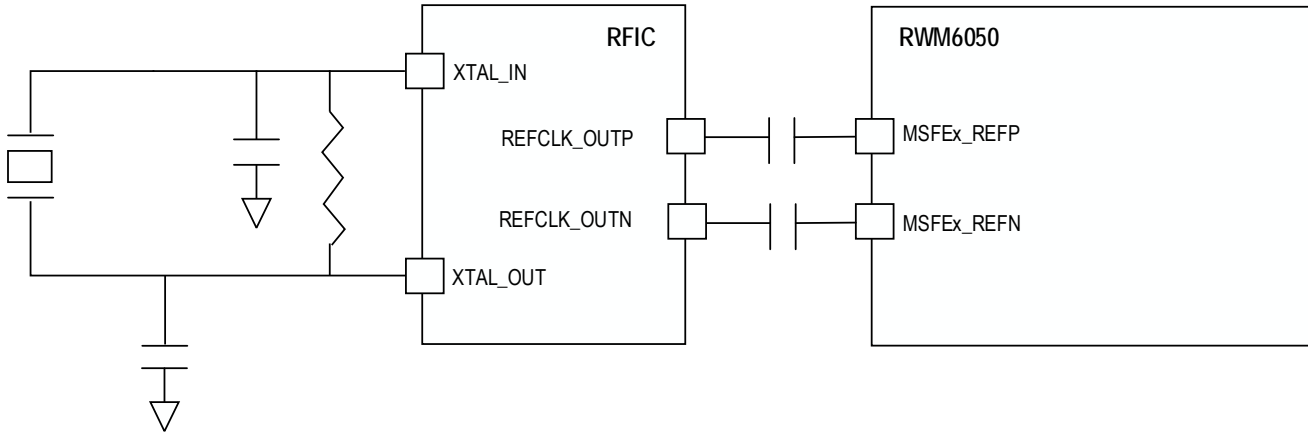
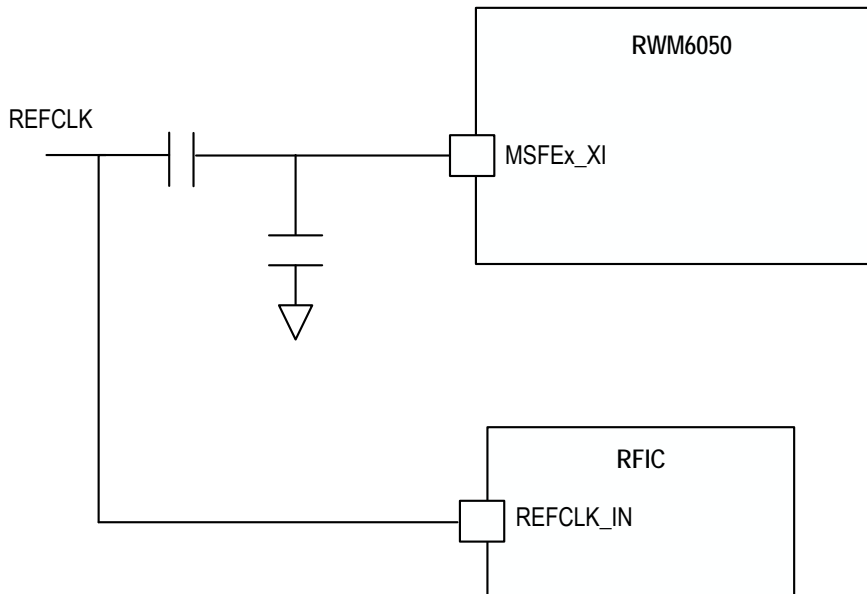


Figure 23. PHY Clocks - RWM6050 and RF Slave



5. Package Specifications

5.1 Package Information

Package information for the RWM6050 is summarized in the following table.

Table 41. Package Information

Specification	Description
Package Code	ALG484
Pb (Lead) Free	Yes - e1 SnAgCu
Package type	FlipChip BGA (FCBGA)
Package Length × Width	19 × 19 mm
Package Thickness - Nominal	2.47mm
Ball pitch	0.8mm
Ball diameter	0.5mm
Ball count	484

5.2 Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

5.3 Thermal Characteristics

Heat generated by the packaged silicon must be removed from the package to ensure the silicon is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive, the silicon temperature may exceed the temperature limits. A consequence of this is that the silicon may fail to meet the performance specifications and the reliability objectives may be affected.

Failure mechanisms and failure rate of a device has an exponential dependence on the silicon operating temperatures. Therefore, the control of the package, and by extension the junction temperature, is essential to ensure product reliability. The device is specified safe for operation when the junction temperature is within the recommended limits as displayed in [Table 14](#). [Table 42](#) shows the simulated junction to board and case thermal characteristics (Theta JB and Theta JC).

Table 42. Junction to Board/Case Thermal Characteristics (Theta JB/JC)

Interface	Results (°C/Watt)
Theta JB (Junction to Board)	2.74
Theta JC (Junction to Case)	0.466

Table 43 shows the simulated junction to ambient characteristics (Theta JA) of the FCBGA package. The thermal resistance Theta JA characteristics of a package depends on multiple variables other than just the package. In a typical application, designers must consider various system-level and environmental characteristics, such as:

- Package mounting (vertical/horizontal)
- System airflow conditions (laminar/turbulent)
- Heat sink design and thermal characteristics
- Heat sink attachment method
- PWB size, layer count, and conductor thickness
- Influence of the heat dissipating components assembled on the PWB (neighboring effects)

Table 43. Junction to Ambient Thermal Characteristics (Theta JA)

Package	Theta JA Results at Specified Airflow (°C/Watt)		
	0 m/s	1 m/s	2 m/s
FCBGA – No heat sink	13.8	10.34	8.89
FCBGA – With heat sink ^[a]	9.72	6.7	5.82

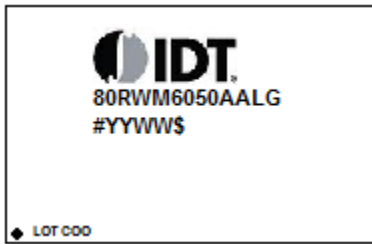
[a] Heat sink dimensions: See Table 44.

The simulated results in Table 44 are based on a JEDEC Thermal Test Board configuration (JESD51-9), and do not factor in the system-level characteristics described above. As such, these values are for reference only.

Table 44. With External Heat Sink

Characteristic	Value
Heat sink dimensions	19 × 19 mm
heat sink base thickness	1mm
Fin height	10mm
Thermal grease with conductivity of	25W/m-K

6. Marking Diagram



1. Line 1 is the part number.
2. Line 2:
 - “#” denotes stepping.
 - “YY” is the last two digits of the year, and “WW” is a work week number that the part was assembled.
 - “\$” denotes the mark code.

7. Ordering Information

Orderable Part Number	Description and Package	Shipping Packaging	Temperature
80RWM6050BALG	19 × 19 mm, 484-FCBGA	Tray	-40°C to 85°C
80RWM6050BALGI	19 × 19 mm, 484-FCBGA	Tray	0°C to 70°C

Revision History

Revision Date	Description of Change
January 22, 2018	<ul style="list-style-type: none"> ▪ Added a 01b setting for MODE1 in Table 2 ▪ Updated the description of the Flash SPI Boot signals in Table 6 ▪ Added a note to JTAG_SELECT in Table 9 ▪ Updated the minimum and maximum specifications in Table 24 ▪ Added Figure 20 ▪ Updated the Thermal Characteristics ▪ Updated the Ordering Information ▪ Completed other minor changes
December 19, 2017	<ul style="list-style-type: none"> ▪ Moved several topics from the <i>RWM6050 User Manual</i> into this document ▪ Updated the Pin Descriptions ▪ Updated the Electrical Specifications ▪ Updated System Clocking ▪ Provided estimates for typical power numbers ▪ Changed the ambient temperature specification to industrial grade in Ordering Information ▪ Updated the package outline drawings; however, no technical changes ▪ Completed other minor updates across the document
June 19, 2017	<ul style="list-style-type: none"> ▪ Completed numerous changes throughout the document ▪ Moved several topics to the currently unreleased <i>RWM6050 User Manual</i>
February 7, 2017	<ul style="list-style-type: none"> ▪ Updated the Pin Descriptions and relevant signal descriptions ▪ Completed other minor changes throughout the document
September 9, 2016	Changed the branding of the device. No technical changes were made.
July 15, 2016	Completed numerous minor changes throughout the document.
May 30, 2016	First release.



Corporate Headquarters
 6024 Silver Creek Valley Road
 San Jose, CA 95138 USA
www.IDT.com

Sales
 1-800-345-7015 or 408-284-8200
 Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its affiliated companies (herein referred to as "IDT") reserve the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners. For datasheet type definitions and a glossary of common terms, visit www.idt.com/go/glossary. Integrated Device Technology, Inc.. All rights reserved.