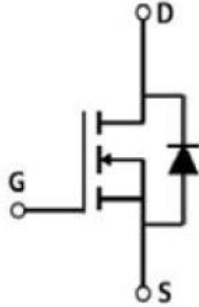


N-Channel Enhancement Mode Field Effect Transistor



TO-220

Product Summary

- V_{DS} 150V
- I_D 25A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 75 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 88 mohm

General Description

- Split Gate Trench MOSFET technology
- High Speed Power Switching, logic level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested

Applications

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- Motor Control

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

| Parameter | | Symbol | Maximum | Unit |
|---|-------------------|-----------------|----------|--------------|
| Drain-source Voltage | | V_{DS} | 150 | V |
| Gate-source Voltage | | V_{GS} | ± 20 | V |
| Drain Current | $T_C=25^\circ C$ | I_D | 25 | A |
| | $T_C=100^\circ C$ | | 16 | |
| Pulsed Drain Current ^A | | I_{DM} | 90 | A |
| Avalanche Energy, Single Pulse ^B | | E_{AS} | 3.75 | mJ |
| Total Power Dissipation @ $T_C=25^\circ C$ | | P_D | 52 | W |
| Thermal Resistance Junction-to-Case | | $R_{\theta JC}$ | 2.4 | $^\circ C/W$ |
| Junction and Storage Temperature Range | | T_J, T_{STG} | -55~+150 | $^\circ C$ |

■ Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|-----------|----------------------|-------------------------|----------------------------|---------------|
| YJP25N15B | B1 | YJP25N15B | 50 | / | 5000 | Tube |



YJP25N15B

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------------|-----------------------|--|-----------------------|------|------|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} = 0V, I _D =250μA | 150 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =150V, V _{GS} =0V | T _J =25°C | | 1 | μA |
| | | | T _J =100°C | | 100 | |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} = ±20V, V _{DS} =0V | | | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D =250μA | 1.0 | 2.0 | 3.0 | V |
| Static Drain-Source On-Resistance | R _{DS(on)} | V _{GS} =10V, I _D =15A | | 69 | 75 | mΩ |
| | | V _{GS} =4.5V, I _D =7.0A | | 70 | 88 | |
| Trans conductance | g _{fs} | V _{DS} =5V, I _D =15A | | 18 | | S |
| Gate Resistance | R _G | V _{GS} =0V, V _{DS} Open, f=1MHz | | 5.0 | | Ω |
| Diode Forward Voltage | V _{SD} | I _S =15.0A, V _{GS} =0V | | 0.9 | 1.2 | V |
| Maximum Body-Diode Continuous Current | I _S | | | | 25.0 | A |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} =75V, V _{GS} =0V, f=1MHZ | | 625 | | pF |
| Output Capacitance | C _{oss} | | | 37 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 13 | | |
| Switching Parameters | | | | | | |
| Total Gate Charge (10V) | Q _g (10V) | V _{GS} =10V, V _{DD} =75V, I _D =5A | | 11.6 | | nC |
| Total Gate Charge (4.5V) | Q _g (4.5V) | | | 6.5 | | |
| Gate Source Charge | Q _{gs} | | | 1.2 | | |
| Gate Drain Charge | Q _{gd} | | | 4 | | |
| Turn-on Delay Time | t _{d(on)} | V _{GS} =10V, V _{DD} =75V, I _D =5A, R _{GEN} =10Ω | | 10 | | ns |
| Turn-on Rise Time | t _r | | | 7 | | |
| Turn-off Delay Time | t _{d(off)} | | | 14 | | |
| Turn-off Fall Time | t _f | | | 3 | | |
| Reverse Recovery Time | t _{rr} | V _R =75V, I _F =5A, dI _F /dt=100A/μs | | 50 | | ns |
| Reverse Recovery Charge | Q _{rr} | | | 70 | | nC |

A. Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%.

B. L=0.3mH, T_A =25°C.



■ Typical Performance Characteristics

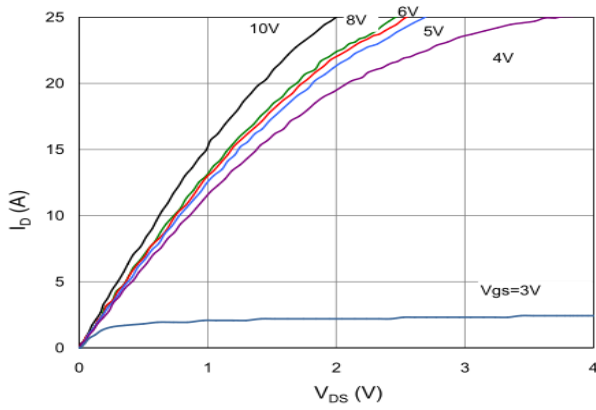


Figure1. Output Characteristics

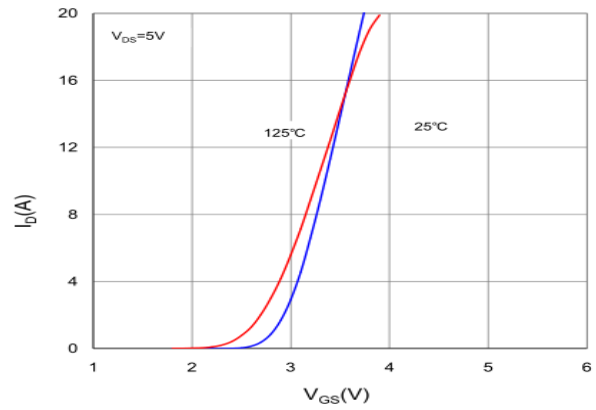


Figure2. Transfer Characteristics

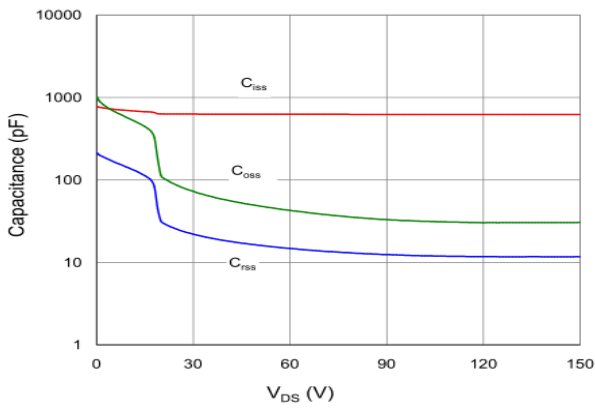


Figure3. Capacitance Characteristics

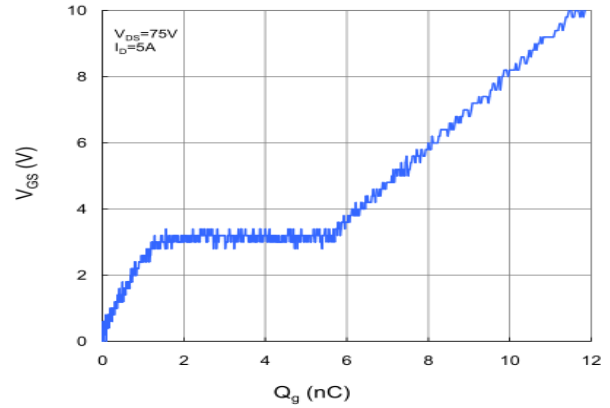


Figure4. Gate Charge

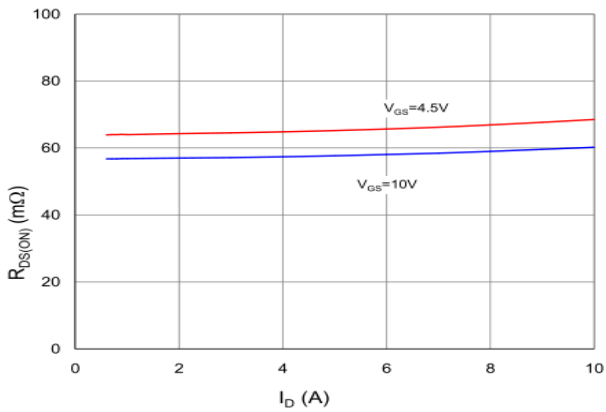


Figure5. Drain-Source on Resistance

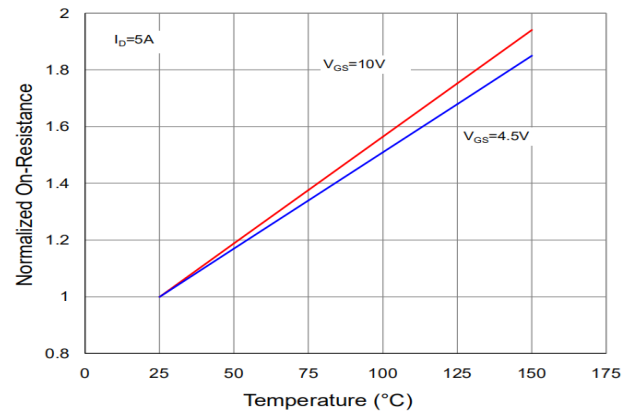


Figure6. Normalized On-Resistance vs. Junction Temperature



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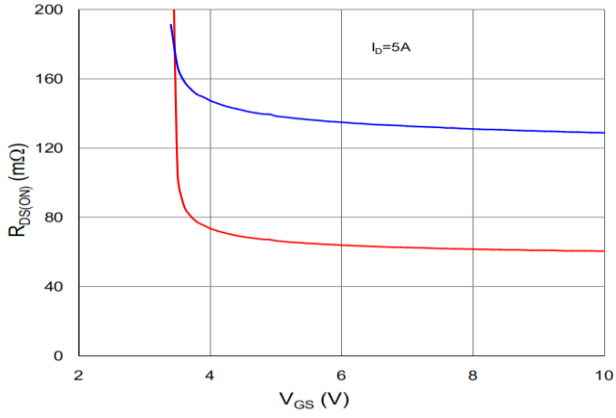


Figure7. On-Resistance vs. Gate-Source Voltage

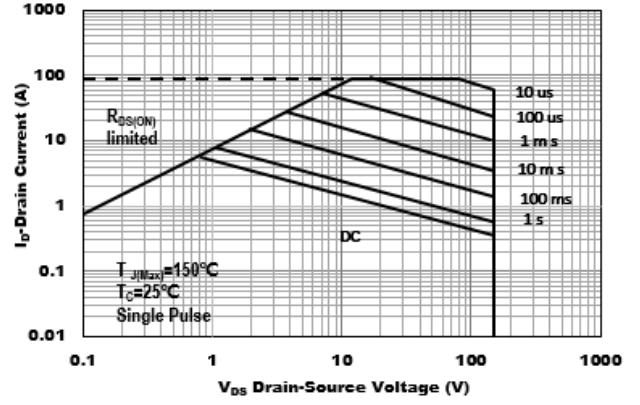


Figure8. Safe Operation Area

Figure A: Gate Charge Test Circuit & Waveforms

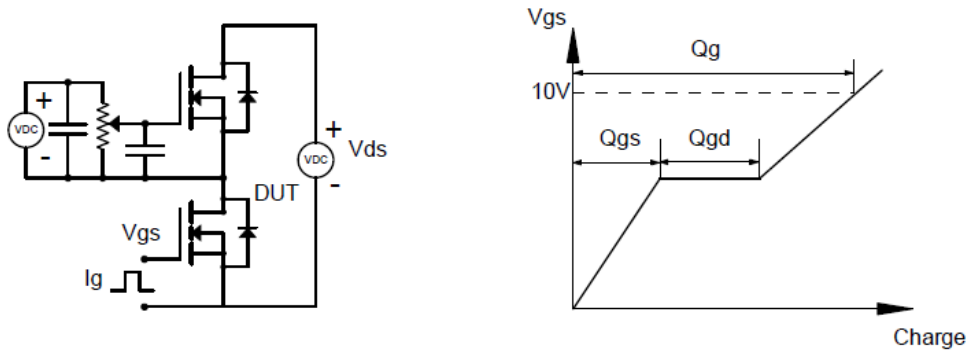


Figure B: Resistive Switching Test Circuit & Waveforms

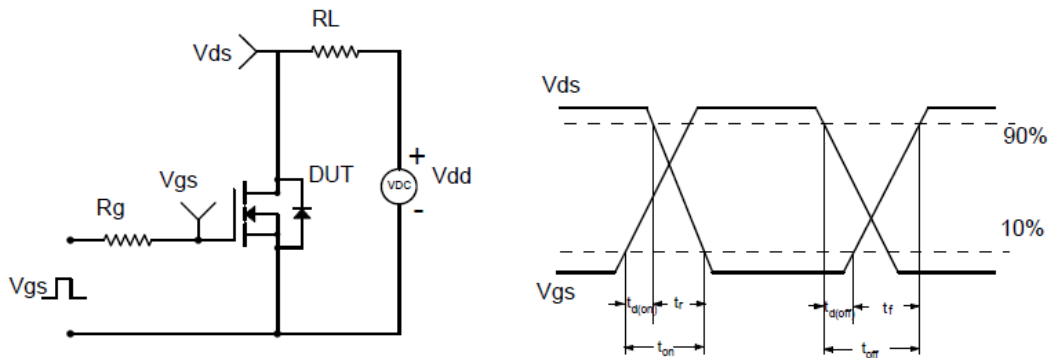


Figure C: Unclamped Inductive Switching (UIS) Test

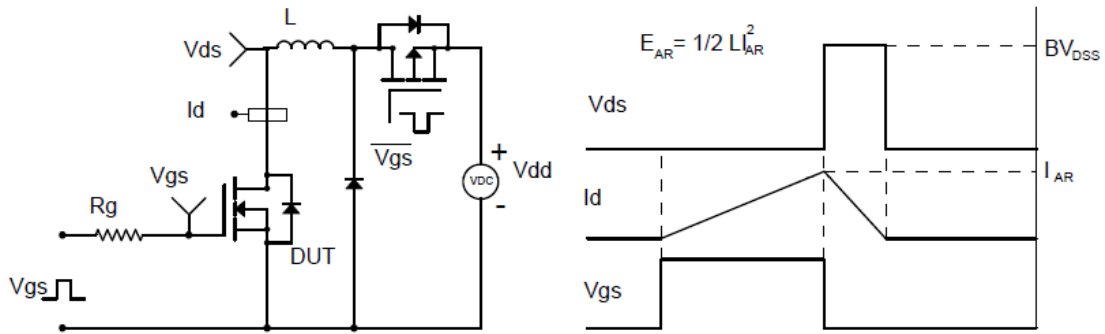
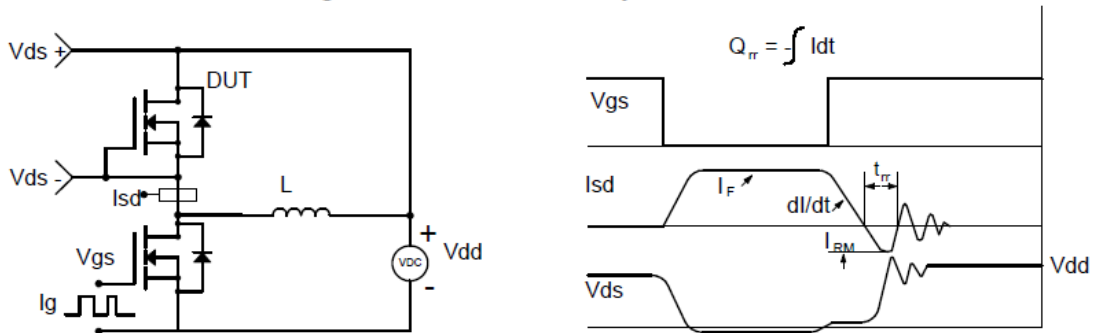


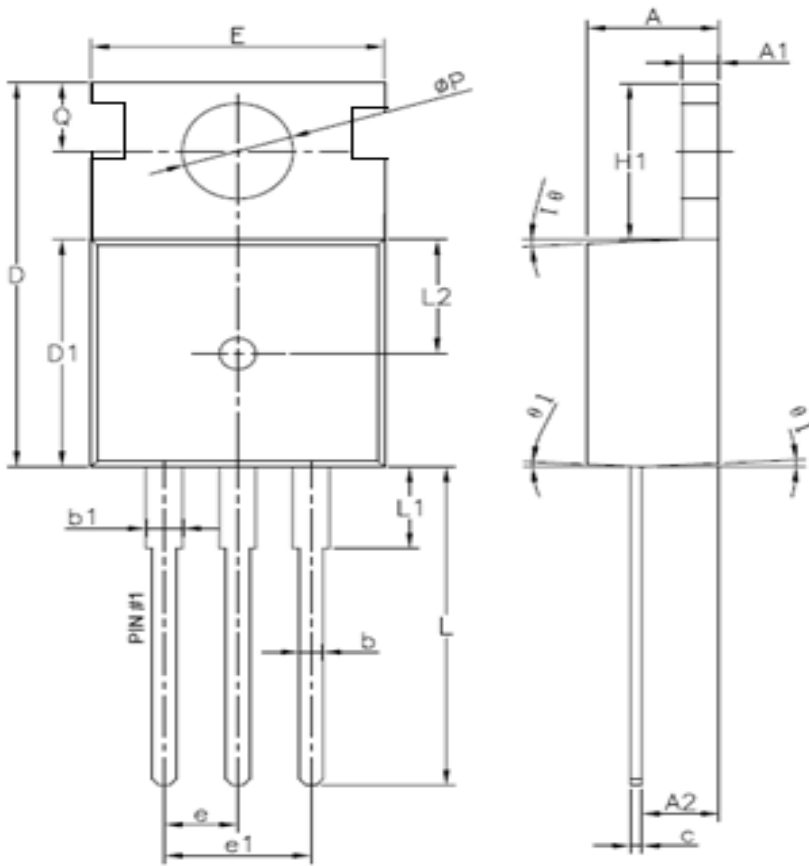
Figure D: Diode Recovery Test Circuit & Waveforms





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■TO-220 Package information



Unit: mm

| Symbol | Min | Normal | Max | Symbol | Min | Normal | Max |
|--------|------|--------|------|--------------|------|--------|------|
| A | 4.4 | 4.5 | 4.6 | e | | 2.54 | |
| A1 | 1.27 | 1.3 | 1.33 | e1 | | 5.08 | |
| A2 | 2.3 | 2.4 | 2.5 | H1 | 6.3 | 6.5 | 6.7 |
| b | 0.7 | / | 0.9 | L | 13.0 | 13.38 | 13.5 |
| b1 | 1.25 | / | 1.42 | L1 | / | / | 3.5 |
| c | 0.45 | 0.5 | 0.6 | L2 | | 4.6 | |
| D | 15.3 | 15.7 | 16.1 | ΦP | 3.55 | 3.6 | 3.65 |
| D1 | 9.1 | 9.2 | 9.3 | Q | 2.73 | / | 2.87 |
| E | 9.7 | 9.9 | 10.2 | θ (°) | 1 | 3 | 5 |



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