Platform Flash In-System Programmable Configuration XA PROMS

DS316-1 (v1.0) October 18, 2004

Advance Product Specification

Features

- AEC-Q100 device qualification and full PPAP support available in both extended temperature Q-grade and I-grade.
- In-System Programmable PROMs for Configuration of Xilinx FPGAs
- Low-Power Advanced CMOS FLASH Process
- Endurance of 20,000 Program/Erase Cycles
- Operation over Full Automotive Temperature Range (–40°C to +125°C)
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) Support for Programming, Prototyping, and Testing
- JTAG Command Initiation of Standard FPGA Configuration
- Cascadable for Storing Longer or Multiple Bitstreams
- Dedicated Boundary-Scan (JTAG) I/O Power Supply (V_{CCJ})
- I/O Pins Compatible with Voltage Levels Ranging From 1.8V to 3.3V
- Design Support Using the Xilinx Alliance ISE and Foundation ISE Series Software Packages
- XAF01S/XAF02S/XAF04S
  - 3.3V supply voltage
  - Serial FPGA configuration interface (up to 33 MHz)
  - Available in small-footprint VOG20 packages.
- Additionally, Xilinx and all of our production partners are qualified to QS-9000, moving to TS16949 in 2005.

Table 1: **Platform Flash PROM Features**

	Density	V_{CCINT}	V_{CCO} / V_{CCJ} Range	Packages	JTAG ISP Programming	Serial Configuration
XAF01S	1 Mbit	3.3V	1.8V - 3.3V	VOG20	√	√
XAF02S	2 Mbit	3.3V	1.8V - 3.3V	VOG20	√	√
XAF04S	4 Mbit	3.3V	1.8V - 3.3V	VOG20	√	√

Description

Xilinx introduces the Platform Flash series of in-system programmable configuration PROMs. Available in 1 to 4 Megabit (Mbit) densities, these PROMs provide an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bitstreams. The Platform Flash PROM series comprises the 3.3V XAFxxS PROM. The XAFxxS version includes 4-Mbit, 2-Mbit, and 1-Mbit PROMs that support Master Serial and Slave Serial FPGA configuration modes (Figure 1). A summary of the Platform Flash PROM family members and supported features is shown in Table 1.

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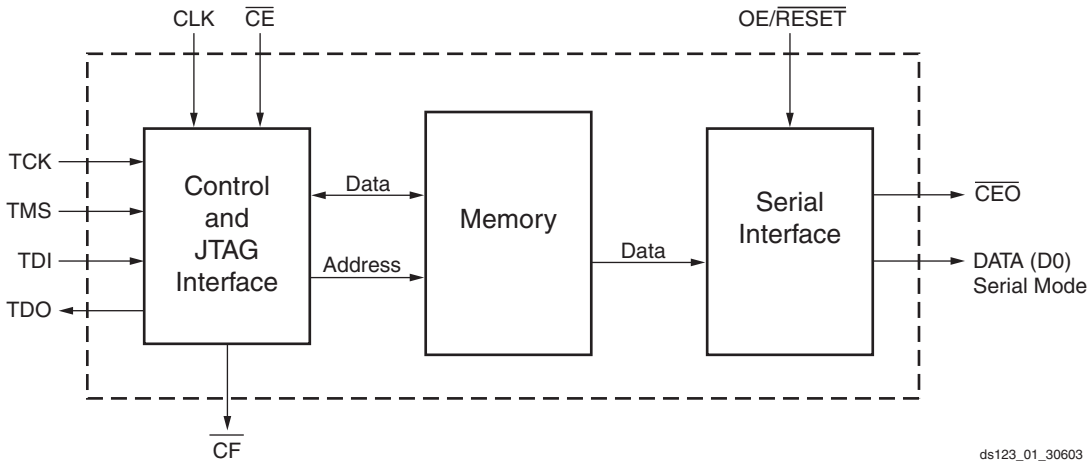


Figure 1: **XAFxxS Platform Flash PROM Block Diagram**

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. With $\overline{CF}$ High, a short access time after $\overline{CE}$ and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration.

When the FPGA is in Slave Serial mode, the PROM and the FPGA are both clocked by an external clock source.

The Platform Flash PROMs are compatible with all of the existing FPGA device families. A reference list of Xilinx FPGAs and the respective compatible Platform Flash PROMs is given in Table 2. A list of Platform Flash PROMs and their capacities is given in Table 3.

Table 2: **Xilinx FPGAs and Compatible Platform Flash PROMs**

FPGA	Configuration Bitstream	Platform Flash PROM
Spartan-3		
XA3S50	439,264	XCF01S
XA3S200	1,047,616	XCF01S
XA3S400	1,699,136	XCF02S
XA3S1000	3,223,488	XCF04S
Spartan-IIE		
XA2S50E	630,048	XCF01S
XA2S100E	863,840	XCF01S
XA2S150E	1,134,496	XCF02S
XA2S200E	1,442,016	XCF02S
XA2S300E	1,875,648	XCF02S

Table 3: **Platform Flash PROM Capacity**

Platform Flash PROM	Configuration Bits
XAF01S	1,048,576
XAF02S	2,097,152
XAF04S	4,194,304

Programming

In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 2. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. During in-system programming, the $\overline{CEO}$ output is driven High. All other outputs are held in a high-impedance state or held at clamp levels during in-system programming. In-system programming is fully supported across the recommended operating voltage and temperature ranges.

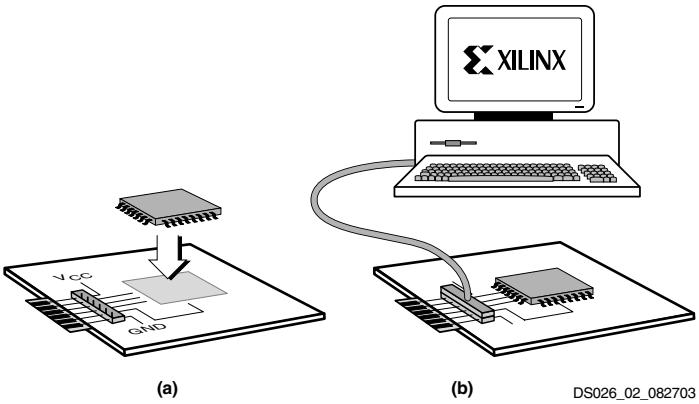


Figure 2: **JTAG In-System Programming Operation**
(a) Solder Device to PCB
(b) Program Using Download Cable

OE/$\overline{RESET}$

The 1/2/4 Mbit XAFxxS Platform Flash PROMs in-system programming algorithm requires issuance of a reset that causes OE/$\overline{RESET}$ to pulse Low.

External Programming

Xilinx reprogrammable PROMs can also be programmed by the Xilinx MultiPRO Desktop Tool or a third-party device programmer. This provides the added flexibility of using pre-programmed devices with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable Platform Flash PROM devices incorporate advanced data security features to fully protect the FPGA programming data against unauthorized reading via JTAG. Table 4 shows the security settings available for the XAFxxS PROM.

Read Protection

The read protect security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. Read protection does not prevent write operations. For the XAFxxS PROM, the read protect security bit is set for the entire device, and resetting the read protect security bit requires erasing the entire device.

Table 4: **XAFxxS Device Data Security Options**

Read Protect	Read/Verify Inhibited	Program Inhibited	Erase Inhibited
Reset (default)			
Set	√		

IEEE 1149.1 Boundary-Scan (JTAG)

The Platform Flash PROM family is IEEE Standard 1532 in-system programming compatible, and is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG, which is a subset of IEEE Std. 1532 Boundary-Scan. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the Platform Flash PROM device. Table 5 lists the required and optional boundary-scan instructions supported in the Platform Flash PROMs. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Instruction Register

The Instruction Register (IR) for the Platform Flash PROM is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

XAFxxS Instruction Register (8 bits wide)

The Instruction Register (IR) for the XAFxxS PROM is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Figure 3.

The instruction capture pattern shifted out of the XAFxxS device includes IR[7:0]. IR[7:5] are reserved bits and are set to a logic "0". The ISC Status field, IR[4], contains logic "1" if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic "0". The Security field, IR[3], contains logic "1" if the device has been programmed with the security option turned on; otherwise, it contains logic "0". IR[2] is unused, and is set to '0'. The remaining bits IR[1:0] are set to '01' as defined by IEEE Std. 1149.1.

Table 5: **Platform Flash PROM Boundary Scan Instructions**

Boundary-Scan Command	XAFxxS IR[7:0] (hex)	Instruction Description
Required Instructions		
BYPASS	FF	Enables BYPASS
SAMPLE/PRELOAD	01	Enables boundary-scan SAMPLE/PRELOAD operation
EXTEST	00	Enables boundary-scan EXTEST operation
Optional Instructions		
CLAMP	FA	Enables boundary-scan CLAMP operation
HIGHZ	FC	Places all outputs in high-impedance state simultaneously
IDCODE	FE	Enables shifting out 32-bit IDCODE
USERCODE	FD	Enables shifting out 32-bit USERCODE
Platform Flash PROM Specific Instructions		
CONFIG	EE	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low once. (For the XCFxxP this command also resets the selected design revision based on either the external REV_SEL[1:0] pins or on the internal design revision selection bits.)(1)

Notes:
1. For more information see Initiating FPGA Configuration.

TDI →	IR[7:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	→ TDO
	Reserved	ISC Status	Security	0	0 1	

Figure 3: **XAFxxS Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the Platform Flash PROM has two register stages which contribute to the boundary-scan register, while each input pin has only one register stage. The bidirectional pins have a total of three register stages which contribute to the boundary-scan register. For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the output pin. For each input pin, a single register stage controls and observes the input state of the pin. The bidirectional pin combines the three bits, the input stage bit is first, followed by the output stage bit and finally the output enable stage bit. The output enable stage bit is closest to TDO.

See the XAFxxS Pin Names and Descriptions Table in the **Pinouts and Pin Descriptions** section for the boundary-scan bit order for all connected device pins, or see the appropriate BSDL file for the complete boundary-scan bit order description under the "attribute BOUNDARY_REGISTER" section in the BSDL file. The bit assigned to boundary-scan cell "0" is the LSB in the boundary-scan register, and is the register bit closest to TDO.

Identification Registers

IDCODE Register

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG. Table 6 lists the IDCODE register values for the Platform Flash PROMs.

The IDCODE register has the following binary format:

```
vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1
```

where

v = the die version number
f = the PROM family code
a = the specific Platform Flash PROM product ID
c = the Xilinx manufacture's ID

The LSB of the IDCODE register is always read as logic "1" as defined by IEEE Std. 1149.1.

Table 6: **IDCODES A ssigned to Platform Flash PROMs**

Device	IDCODE(1) (hex)
XAF01S	05044093
XAF02S	05045093
XAF04S	05046093

Notes:
1. The first four bits indicate the die version number, and may vary.

USERCODE Register

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the Platform Flash PROM. If the device is blank or was not loaded during programming, the USERCODE register contains FFFFFFFFh.

Platform Flash PROM TAP Characteristics

The Platform Flash PROM family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the Platform Flash PROM TAP are described as follows.

TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

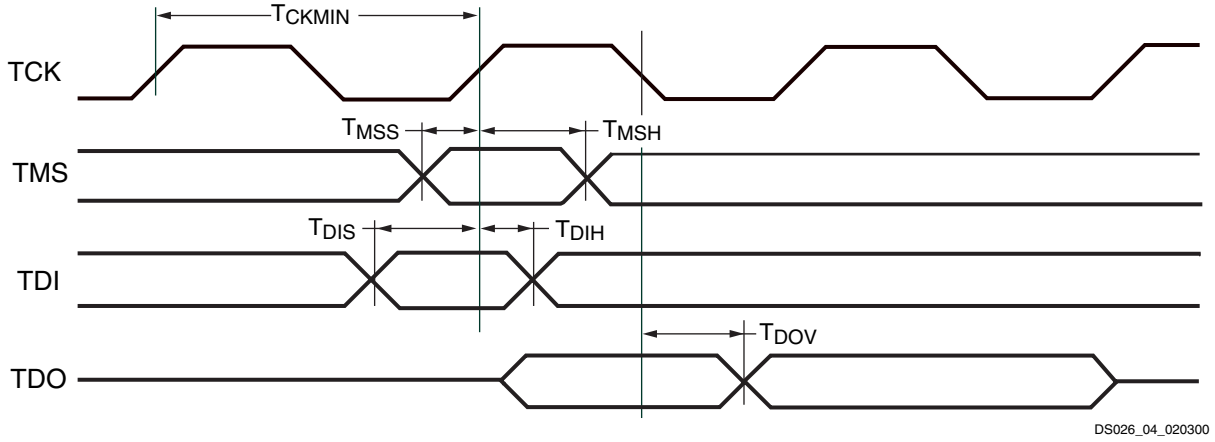


Figure 4: **Test Access Port Timing**

TAP AC Parameters

Table 7 shows the timing parameters for the TAP waveforms shown in Figure 4.

Table 7: **Test Access Port Timing Parameters**

Symbol	Parameter	Min	Max	Units
T_{CKMIN1}	TCK minimum clock period when V_{CCJ} = 2.5V or 3.3V	100	-	ns
T_{CKMIN2}	TCK minimum clock period, Bypass Mode, when V_{CCJ} = 2.5V or 3.3V	50	-	ns
T_{MSS}	TMS setup time when V_{CCJ} = 2.5V or 3.3V	10	-	ns
T_{MSH}	TMS hold time when V_{CCJ} = 2.5V or 3.3V	25	-	ns
T_{DIS}	TDI setup time when V_{CCJ} = 2.5V or 3.3V	10	-	ns
T_{DIH}	TDI hold time when V_{CCJ} = 2.5V or 3.3V	25	-	ns
T_{DOV}	TDO valid delay when V_{CCJ} = 2.5V or 3.3V	-	30	ns

PROM to FPGA Configuration Mode and Connections Summary

The FPGA's I/O, logical functions, and internal interconnections are established by the configuration data contained in the FPGA's bitstream. The bitstream is loaded into the FPGA either automatically upon power up, or on command, depending on the state of the FPGA's mode pins. Xilinx Platform Flash PROMs are designed to download directly to the FPGA configuration interface. FPGA configuration modes which are supported by the XAFxxS Platform Flash PROMs include: Master Serial and Slave Serial. See the respective FPGA data sheet for device configuration details, including which configuration modes are supported by the targeted FPGA device.

FPGA Master Serial Mode

In Master Serial mode, the FPGA automatically loads the configuration bitstream in bit-serial form from external memory synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master Serial configuration mode. Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be set up at the FPGA's DIN input pin a short time before each rising edge of the FPGA's internally generated CCLK signal.

Typically, a wide range of frequencies can be selected for the FPGA's internally generated CCLK which always starts at a slow default frequency. The FPGA's bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master Serial configuration sequence. The desired CCLK frequency is selected during bitstream generation.

Connecting the FPGA device to the configuration PROM for Master Serial Configuration Mode (Figure 5):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s)
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary I_{CC} active supply current (**DC Characteristics Over Operating Conditions**).
- The PROM $\overline{CF}$ pin is typically connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input. For the XCFxxP only, the $\overline{CF}$ pin is a bidirectional pin. If the XCFxxP $\overline{CF}$ pin is not connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input, then the pin should be tied High.

FPGA Slave Serial Mode

In Slave Serial mode, the FPGA loads the configuration bitstream in bit-serial form from external memory synchronized by an externally supplied clock. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Slave Serial configuration mode. Slave Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be set up at the FPGA's DIN input pin a short time before each rising edge of the externally provided CCLK.

Connecting the FPGA device to the configuration PROM for Slave Serial Configuration Mode (Figure 6):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- An external clock source drives the FPGA's CCLK input.
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the INIT_B (or INIT) pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary I_{CC} active supply current (**DC Characteristics Over Operating Conditions**).
- The PROM $\overline{CF}$ pin is typically connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input.

Serial Daisy Chain

Multiple FPGAs can be daisy-chained for serial configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the FPGA's DOUT pin. Typically the data on the DOUT pin changes on the falling edge of CCLK, although for some devices the DOUT pin changes on the rising edge of CCLK. Consult the respective device data sheets for detailed information on a particular FPGA device. For clocking the daisy-chained configuration, either the first FPGA in the chain can be set to Master Serial, generating the CCLK, with the remaining devices set to Slave Serial (Figure 7), or all the FPGA devices can be set to Slave Serial and an externally generated clock can be used to drive the FPGA's configuration interface.

FPGA Master SelectMAP (Parallel) Mode

In Master SelectMAP mode, byte-wide data is written into the FPGA, typically with a BUSY flag controlling the flow of data, synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master SelectMAP configuration mode. The configuration interface typically requires a parallel data bus, a clock line, and two control lines (INIT and DONE). In addition, the FPGA's Chip Select, Write, and BUSY pins must be correctly controlled to enable SelectMAP configuration. The configuration data is read from the PROM byte by byte on pins [D0..D7], accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The bitstream data must be set up at the FPGA's [D0..D7] input pins a short time before each rising edge of the FPGA's internally generated CCLK signal. If BUSY is asserted (High) by the FPGA, the configuration data must be held until BUSY goes Low. An external data source or external pull-down resistors must be used to enable the FPGA's active Low Chip Select ($\overline{CS}$ or CS_B) and Write ($\overline{WRITE}$ or RDWR_B) signals to enable the FPGA's SelectMAP configuration process.

The Master SelectMAP configuration interface is clocked by the FPGA's internal oscillator. Typically, a wide range of frequencies can be selected for the internally generated CCLK which always starts at a slow default frequency. The FPGA's bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master SelectMAP configuration sequence. The desired CCLK frequency is selected during bitstream generation.

Connecting the FPGA device to the configuration PROM for Master SelectMAP (Parallel) Configuration Mode:

- The DATA outputs of the PROM(s) drive the [D0..D7] input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s)
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary I_{CC} active supply current (**DC Characteristics Over Operating Conditions**).
- For high-frequency parallel configuration, the BUSY pins of all PROMs are connected to the FPGA's BUSY output. This connection assures that the next data

transition for the PROM is delayed until the FPGA is ready for the next configuration data byte.

- The PROM $\overline{CF}$ pin is typically connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input.

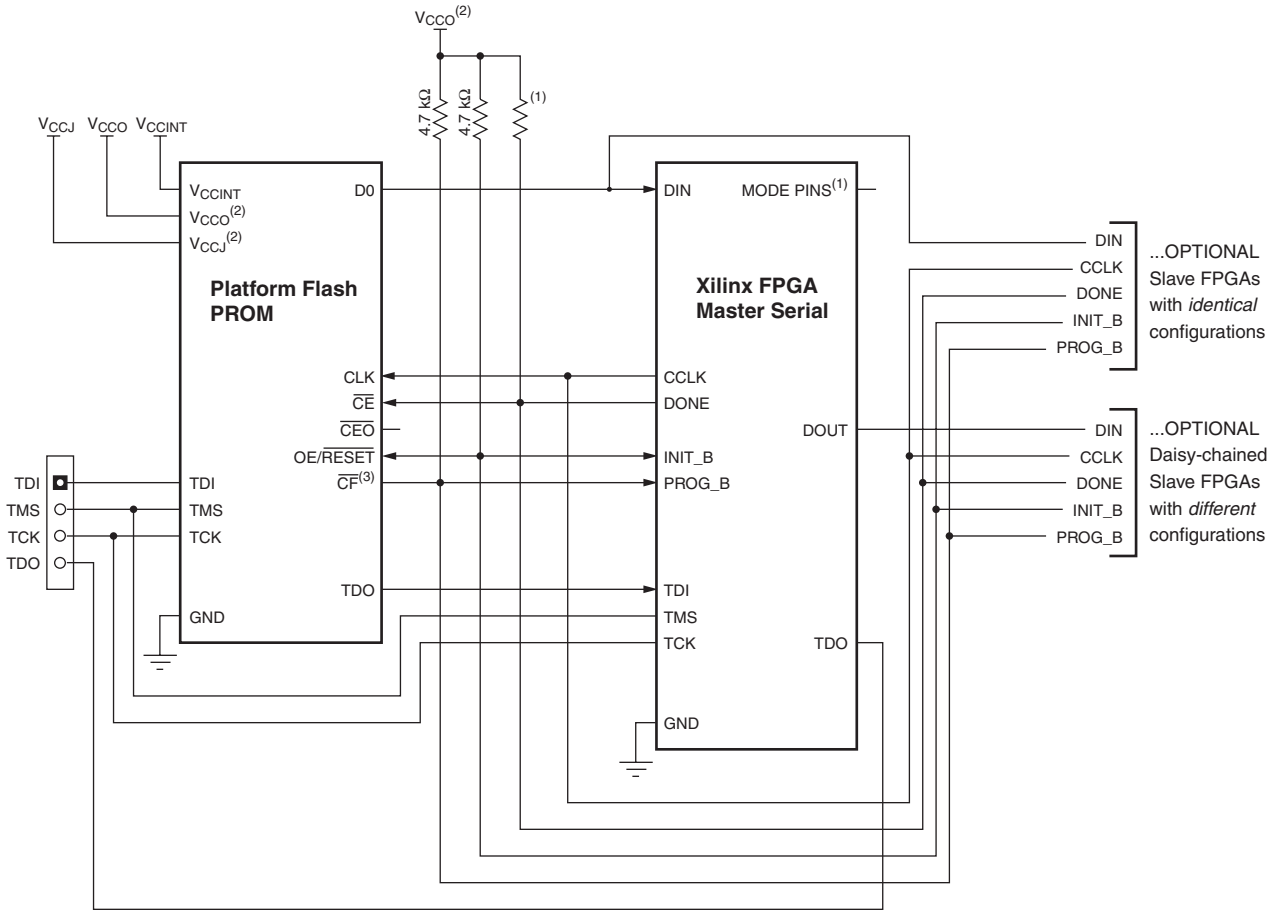
Initiating FPGA Configuration

The options for initiating FPGA configuration via the Platform Flash PROM include:

1. Automatic configuration on power up
2. Applying an external PROG_B (or $\overline{PROGRAM}$) pulse
3. Applying the JTAG CONFIG instruction

Following the FPGA's power-on sequence or the assertion of the PROG_B (or $\overline{PROGRAM}$) pin the FPGA's configuration memory is cleared, the configuration mode is selected, and the FPGA is ready to accept a new configuration bitstream. The FPGA's PROG_B pin can be controlled by an external source, or alternatively, the Platform Flash PROMs incorporate a $\overline{CF}$ pin that can be tied to the FPGA's PROG_B pin. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ output Low once for 300-500 ns, resetting the FPGA and initiating configuration. The iMPACT software can issue the JTAG CONFIG command to initiate FPGA configuration by setting the "Load FPGA" option.

Configuration PROM to FPGA Device Interface Connection Diagrams



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 For the XAFxxS the CF pin is an output pin.

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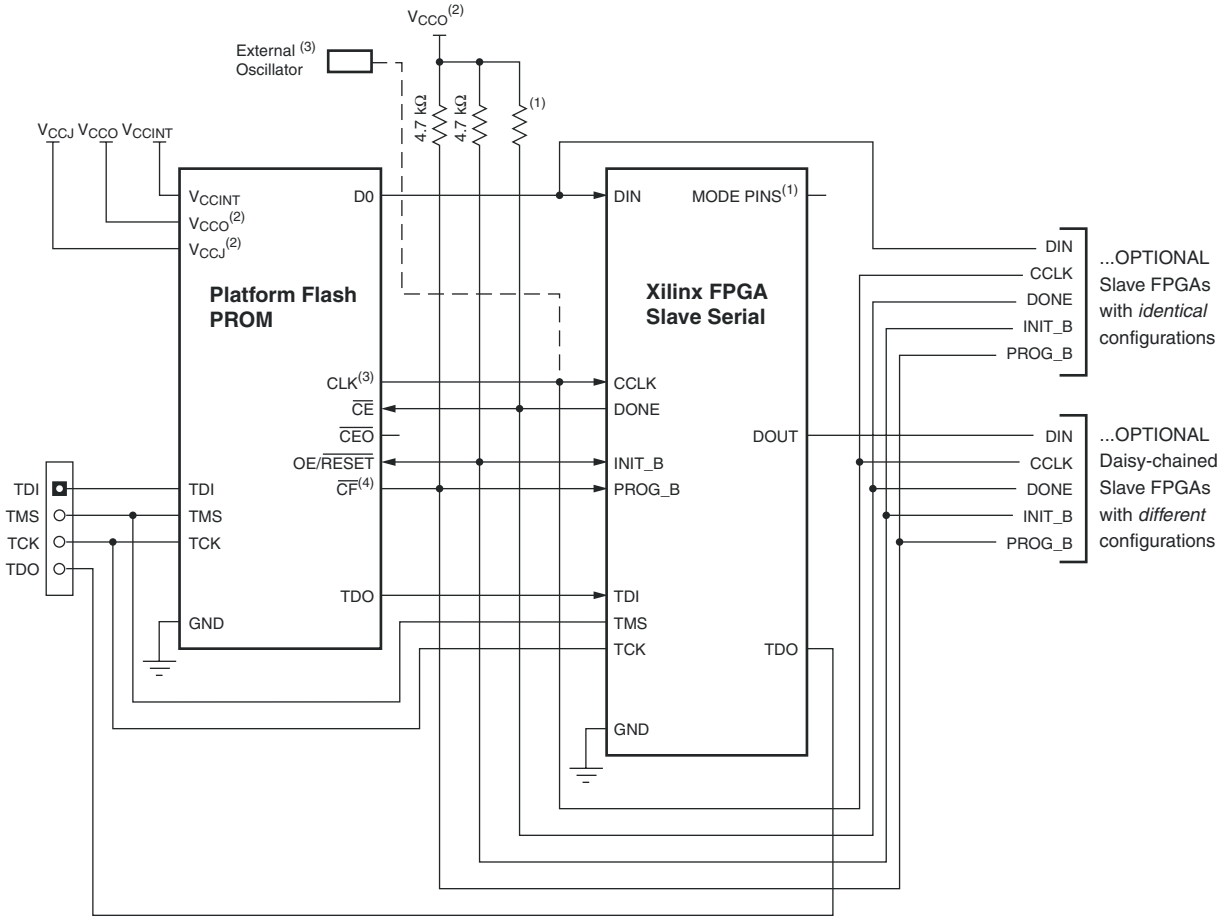
Figure 5: **Configuring in Master Serial Mode**



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 In Slave Serial mode, the configuration interface can be clocked by an external oscillator, or optionally—for the XCFxxP Platform Flash PROM only—the CLKOUT signal can be used to drive the FPGA's configuration clock (CCLK). If the XCFxxP PROM's CLKOUT signal is used, then it must be tied to a 4.7KΩ resistor pulled up to V_{CCO}.
4 For the XAFxxS the CF pin is an output pin.

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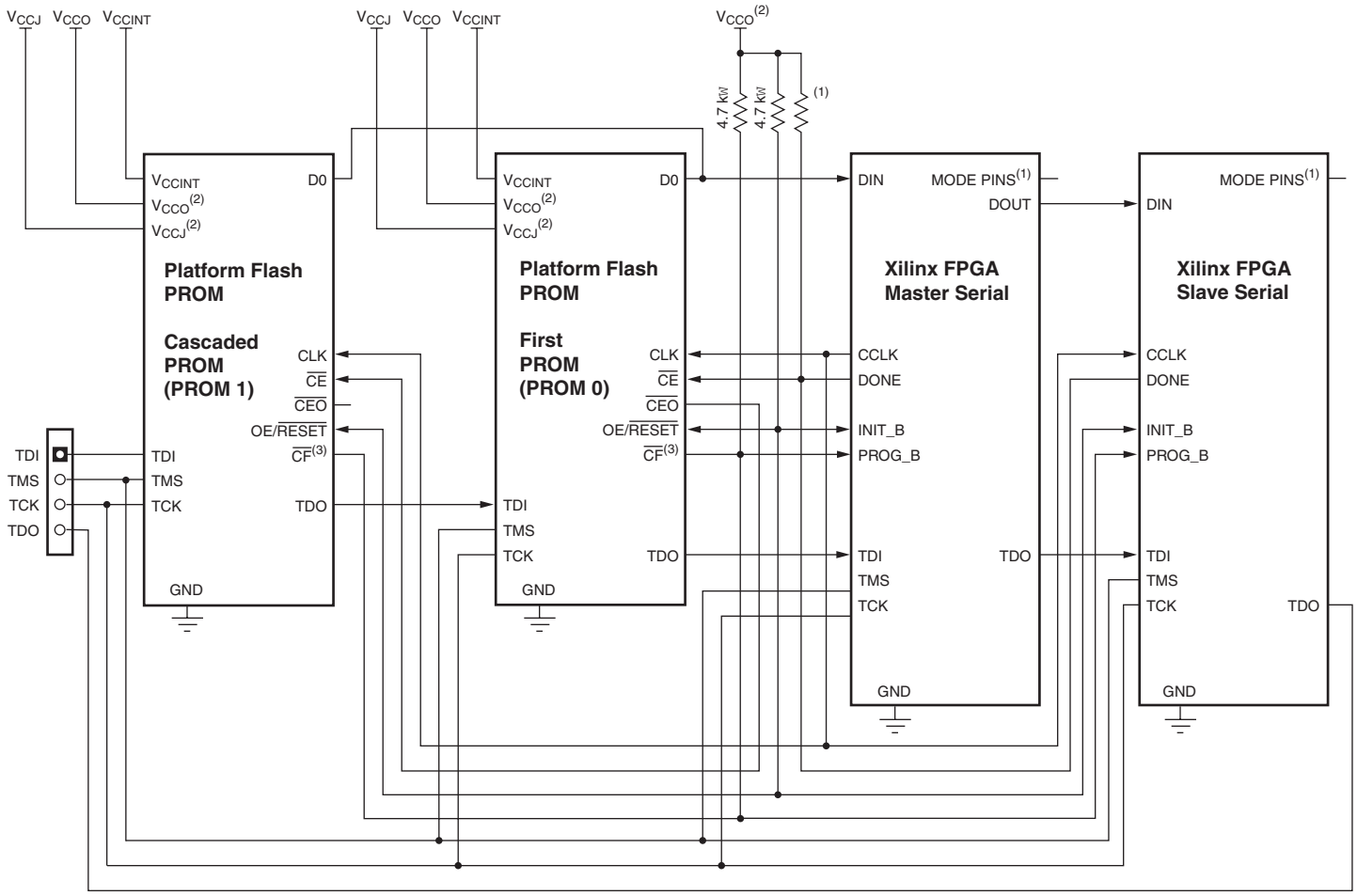
Figure 6: **Configuring in Slave Serial Mode**



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 For the XAFxxS the CF pin is an output pin.

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Figure 7: **Configuring Multiple Devices Master/Slave Serial Mode**

Reset and Power-On Reset Activation

At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified V_{CCINT} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on reset properly. During the power-up sequence, OE/$\overline{RESET}$ is held Low by the PROM. Once the required supplies have reached their respective POR (Power On Reset) thresholds, the OE/$\overline{RESET}$ release is delayed (T_{OER} minimum) to allow more margin for the power supplies to stabilize before initiating configuration. The OE/$\overline{RESET}$ pin is connected to an external 4.7kΩ pull-up resistor and also to the target FPGA's INIT pin. For systems utilizing slow-rising power supplies, an additional power monitoring circuit can be used to delay the target configuration until the system power reaches minimum operating voltages by holding the OE/$\overline{RESET}$ pin Low. When OE/$\overline{RESET}$ is released, the FPGA's INIT pin is pulled High allowing the FPGA's configuration sequence to begin. If the power drops below the power-down threshold (V_{CCPD}), the PROM resets and OE/$\overline{RESET}$ is again held Low until the after the POR threshold is reached. OE/$\overline{RESET}$ polarity is not programmable. These power-up requirements are shown graphically in Figure 8.

For a fully powered Platform Flash PROM, a reset occurs whenever OE/$\overline{RESET}$ is asserted (Low) or $\overline{CE}$ is deasserted (High). The address counter is reset, $\overline{CEO}$ is driven High, and the remaining outputs are placed in a high-impedance state.

Notes:

1. The XAFxxS PROM only requires V_{CCINT} to rise above its POR threshold before releasing OE/$\overline{RESET}$.

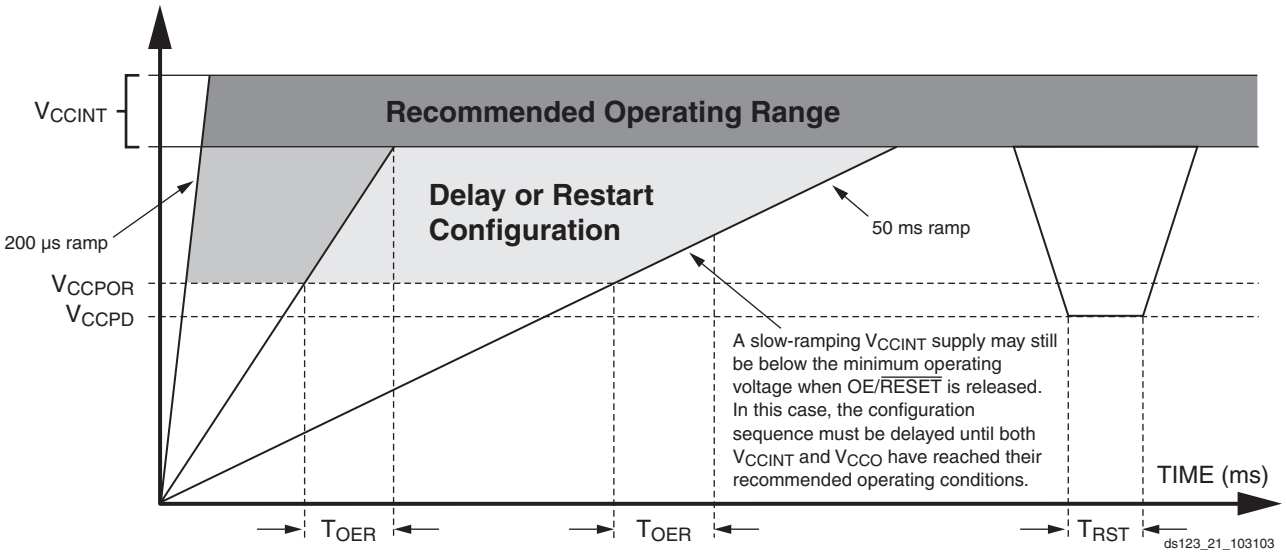


Figure 8: **Platform Flash PROM Power-Up Requirements**

I/O Input Voltage Tolerance and Power Sequencing

The I/Os on each re-programmable Platform Flash PROM are fully 3.3V-tolerant. This allows 3V CMOS signals to connect directly to the inputs without damage. The core power supply (V_{CCINT}), JTAG pin power supply (V_{CCJ}), output power supply (V_{CCO}), and external 3V CMOS I/O signals can be applied in any order.

Additionally, for the XAFxxS PROM only, when V_{CCO} is supplied at 2.5V or 3.3V and V_{CCINT} is supplied at 3.3V, the I/Os are 5V-tolerant. This allows 5V CMOS signals to connect directly to the inputs on a powered XAFxxS PROM without damage. Failure to power the PROM correctly while supplying a 5V input signal may result in damage to the XAFxxS device.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is deasserted (High). In standby mode, the address counter is reset, $\overline{CEO}$ is driven High, and the remaining outputs are placed in a high-impedance state regardless of the state of the OE/$\overline{RESET}$ input. For the device to remain in the low-power standby mode, the JTAG pins TMS, TDI, and TDO must not be pulled Low, and TCK must be stopped (High or Low).

When using the FPGA DONE signal to drive the PROM $\overline{CE}$ pin High to reduce standby power after configuration, an external pull-up resistor should be used. Typically a 330Ω pull-up resistor is used, but refer to the appropriate FPGA data sheet for the recommended DONE pin pull-up value. If the DONE circuit is connected to an LED to indicate FPGA configuration is complete, and is also connected to the PROM $\overline{CE}$ pin to enable low-power standby mode, then an

external buffer should be used to drive the LED circuit to ensure valid transitions on the PROM's $\overline{CE}$ pin. If low-power standby mode is not required for the PROM, then the $\overline{CE}$ pin should be connected to ground.

Table 8: **Truth Table for XAFxxS PROM Control Inputs**

Control Inputs		Internal Address	Outputs		
OE/$\overline{RESET}$	**$\overline{CE}$**		**DATA**	**$\overline{CEO}$**	**ICC**
High	Low	If address < TC(2) : increment	Active	High	Active
		If address = TC(2) : don't change	High-Z	Low	Reduced
Low	Low	Held reset	High-Z	High	Active
X(1)	High	Held reset	High-Z	High	Standby

Notes:
1. X = don't care.
2. TC = Terminal Count = highest address value. TC + 1 = address 0.

DC Electrical Characteristics

AC Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description		XAF01S, XAF02S, XAF04S	Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5 to +4.0	V
V_{CCO}	I/O supply voltage relative to GND		–0.5 to +4.0	V
V_{CCJ}	JTAG I/O supply voltage relative to GND		–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	$V_{CCO} < 2.5V$	–0.5 to +3.6	V
		$V_{CCO} \geq 2.5V$	–0.5 to +5.5	V
V_{TS}	Voltage applied to High-Z output	$V_{CCO} < 2.5V$	–0.5 to +3.6	V
		$V_{CCO} \geq 2.5V$	–0.5 to +5.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_A	Ambient temperature		+125	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
3. For soldering guidelines, see the information on "Packaging and Thermal Characteristics" at www.xilinx.com.

Supply Voltage Requirements for Power-On Reset and Power-Down

Symbol	Description	XAF01S, XAF02S, XAF04S		Units
		Min	Max	
T_{VCC}	V_{CCINT} rise time from 0V to nominal voltage(2)	0.2	50	ms
V_{CCPOR}	POR threshold for the V_{CCINT} supply	1	-	V
T_{OER}	OE/$\overline{\text{RESET}}$ release delay following POR(3)	0	1	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	-	1	V
T_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10	-	ms

Notes:
1. V_{CCINT}, V_{CCO}, and V_{CCJ} supplies may be applied in any order.
2. At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 8, page 12.
3. If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM will not be available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

Recommended Operating Conditions

Symbol	Description		XAF01S, XAF02S, XAF04S			Units
			Min	Typ	Max	
V_{CCINT}	Internal voltage supply		3.0	3.3	3.6	V
V_{CCO}/V_{CCJ}	Supply voltage for output drivers	3.3V Operation	3.0	3.3	3.6	V
		2.5V Operation	2.3	2.5	2.7	V
		1.8V Operation	1.7	1.8	2.0	V
		1.5V Operation	-	-	-	V
V_{IL}	Low-level input voltage	3.3V Operation	0	-	0.8	V
		2.5V Operation	0	-	0.8	V
		1.8V Operation	-	-	20% V_{CCO}	V
		1.5V Operation	-	-	-	V
V_{IH}	High-level input voltage	3.3V Operation	2.0	-	5.5	V
		2.5V Operation	1.7	-	5.5	V
		1.8V Operation	70% V_{CCO}	-	3.6	V
		1.5V Operation	-	-	-	V
T_{IN}	Input signal transition time(1)		-	-	500	ns
V_O	Output voltage		0	-	V_{CCO}	V
T_A	Operating ambient temperature		–40	-	85	°C

Notes:
1. Input signal transition time measured between 10% V_{CCO} and 90% V_{CCO}.

Quality and Reliability Characteristics

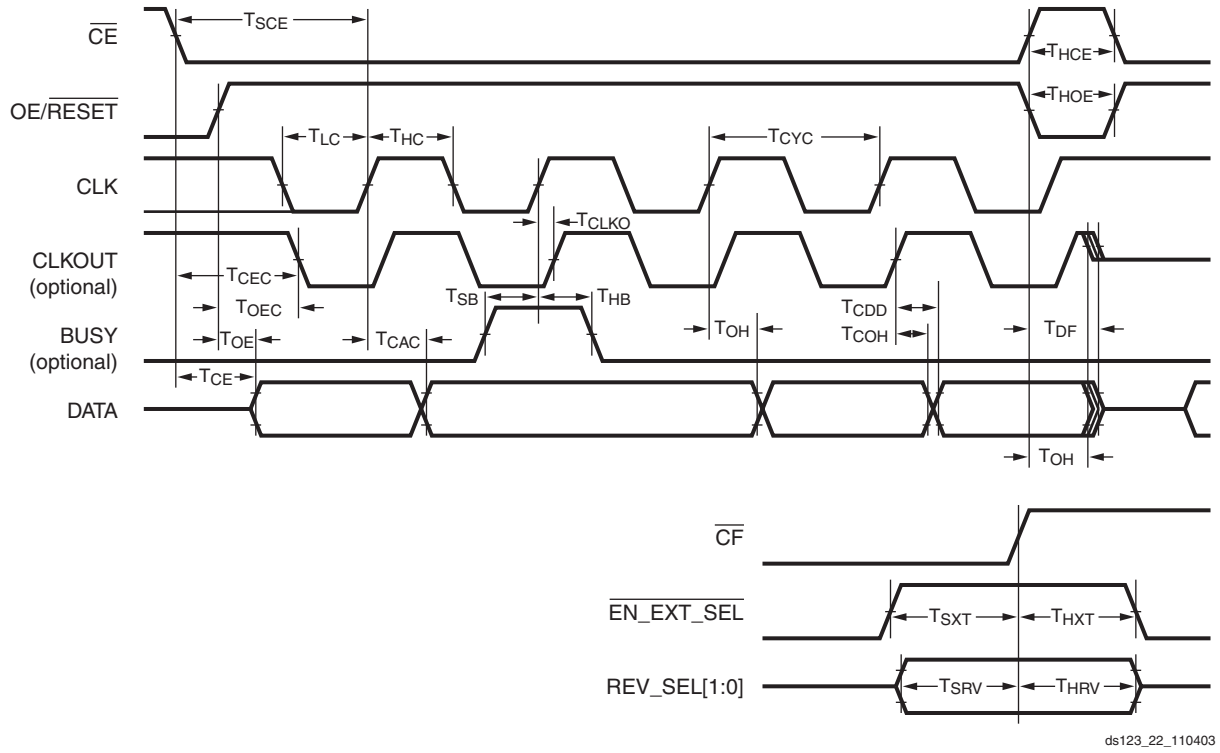
Symbol	Description	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance)	20,000	-	Cycles
V_{ESD}	Electrostatic discharge (ESD)	2,000	-	Volts

DC Characteristics Over Operating Conditions

Symbol	Description	XAF01S, XAF02S, XAF04S			Units
		Test Conditions	Min	Max	
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4	-	V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	V_{CCO} – 0.4	-	V
	High-level output voltage for 1.8V outputs	I_{OH} = –50 µA	V_{CCO} – 0.4	-	V
	High-level output voltage for 1.5V outputs	-	-	-	V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
	Low-level output voltage for 1.8V outputs	I_{OL} = 50 µA	-	0.4	V
	Low-level output voltage for 1.5V outputs	-	-	-	V
I_{CCINT}	Internal voltage supply current, active mode	33 MHz	-	10	mA
I_{CCO}	Output driver supply current, active serial mode	33 MHz	-	5	mA
	Output driver supply current, active parallel mode	-	-	-	mA
I_{CCJ}	JTAG supply current, active mode	Note (1)	-	5	mA
I_{CCINTS}	Internal voltage supply current, standby mode	Note (2)	-	1	mA
I_{CCOS}	Output driver supply current, standby mode	Note (2)	-	1	mA
I_{CCJS}	JTAG supply current, standby mode	Note (2)	-	1	mA
I_{ILJ}	JTAG pins TMS, TDI, and TDO pull-up current	V_{CCJ} = max V_{IN} = GND	-	100	µA
I_{IL}	Input leakage current	V_{CCINT} = max V_{IN} = GND or V_{CCINT}	–10	10	µA
I_{IH}	Input and output High-Z leakage current	V_{CCINT} = max V_{IN} = GND or V_{CCINT}	–10	10	µA
C_{IN}	Input capacitance	V_{IN} = GND f = 1.0 MHz	-	8	pF
C_{OUT}	Output capacitance	V_{IN} = GND f = 1.0 MHz	-	14	pF

Notes:
1. TDI/TMS/TCK non-static (active).
2. $\overline{CE}$ High, OE Low, and TMS/TDI/TCK static.

AC Characteristics Over Operating Conditions



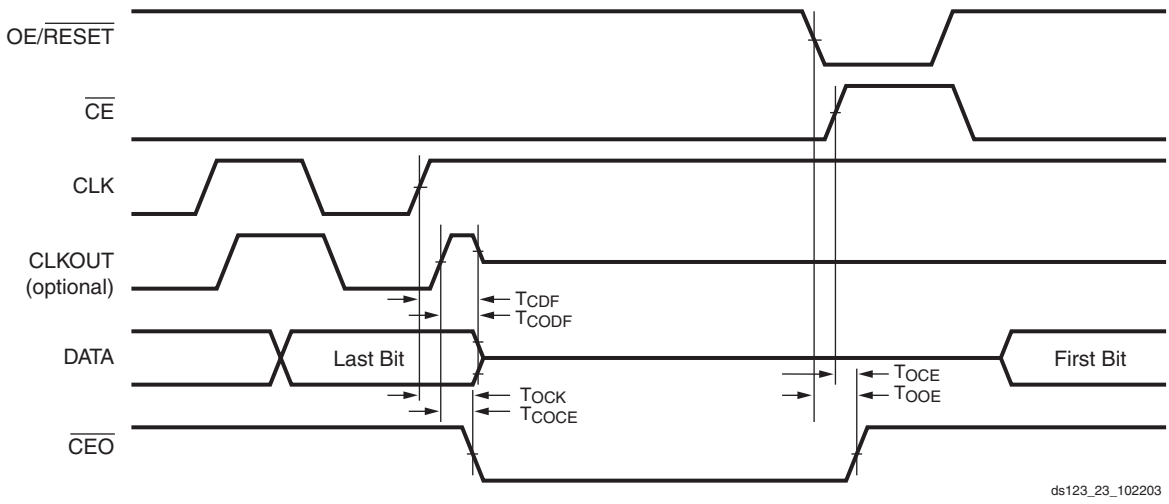
Symbol	Description	XAF01S, XAF02S, XAF04S		Units
		Min	Max	
T_{OE}	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 3.3V or 2.5V	-	10	ns
	OE/$\overline{RESET}$ to data delay(6) when V_{CCO} = 1.8V	-	30	ns
T_{CE}	$\overline{CE}$ to data delay(5) when V_{CCO} = 3.3V or 2.5V	-	15	ns
	$\overline{CE}$ to data delay(5) when V_{CCO} = 1.8V	-	30	ns
T_{CAC}	CLK to data delay when V_{CCO} = 3.3V or 2.5V	-	15	ns
	CLK to data delay when V_{CCO} = 1.8V	-	30	ns
T_{OH}	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or CLK when V_{CCO} = 3.3V or 2.5V	0	-	ns
	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or CLK when V_{CCO} = 1.8V	0	-	ns
T_{DF}	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 3.3V or 2.5V	-	25	ns
	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay(2) when V_{CCO} = 1.8V	-	30	ns
T_{CYC}	Clock period(7) when V_{CCO} = 3.3V or 2.5V	30	-	ns
	Clock period(7) when V_{CCO} = 1.8V	67	-	ns
T_{LC}	CLK Low time(3) when V_{CCO} = 3.3V or 2.5V	10	-	ns
	CLK Low time(3) when V_{CCO} = 1.8V	15	-	ns

Symbol	Description	XAF01S, XAF02S, XAF04S		Units
		Min	Max	
T_{HC}	CLK High time(3) when V_{CCO} = 3.3V or 2.5V	10	-	ns
	CLK High time(3) when V_{CCO} = 1.8V	15	-	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 3.3V or 2.5V	20	-	ns
	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 1.8V	30		ns
T_{HCE}	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	250	-	ns
	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	250	-	ns
T_{HOE}	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 3.3V or 2.5V	250	-	ns
	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 1.8V	250	-	ns
T_{SB}	BUSY setup time to CLK when V_{CCO} = 3.3V or 2.5V	-	-	ns
	BUSY setup time to CLK when V_{CCO} = 1.8V	-	-	ns
T_{HB}	BUSY hold time to CLK when V_{CCO} = 3.3V or 2.5V	-	-	ns
	BUSY hold time to CLK when V_{CCO} = 1.8V	-	-	ns
T_{CLKO}	CLK input to CLKOUT output delay when V_{CCO} = 3.3V or 2.5V	-	-	ns
	CLK input to CLKOUT output delay when V_{CCO} = 1.8V	-	-	ns
T_{CEC}	$\overline{CE}$ to CLKOUT delay when V_{CCO} = 3.3V or 2.5V	-	-	ns
	$\overline{CE}$ to CLKOUT delay when V_{CCO} = 1.8V	-	-	ns
T_{OEC}	OE/$\overline{RESET}$ to CLKOUT delay when V_{CCO} = 3.3V or 2.5V	-	-	ns
	OE/$\overline{RESET}$ to CLKOUT delay when V_{CCO} = 1.8V	-	-	ns
T_{CDD}	CLKOUT to data delay when V_{CCO} = 3.3V or 2.5V	-	-	ns
	CLKOUT to data delay when V_{CCO} = 1.8V	-	-	ns
T_{COH}	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V	-	-	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V	-	-	ns
T_{SXT}	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	ns
	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	ns
T_{HXT}	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	ns
	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	ns
T_{SRV}	REV_SEL setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	ns
	REV_SEL setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	ns

Symbol	Description	XAF01S, XAF02S, XAF04S		Units
		Min	Max	
T_{HRV}	REV_SEL hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	ns
	REV_SEL hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	ns
T_{FF}	CLKOUT default (fast) frequency	-	-	ns
	CLKOUT default (fast) frequency with compression	-	-	ns
T_{SF}	CLKOUT alternate (slower) frequency	-	-	ns
	CLKOUT alternate (slower) frequency with compression	-	-	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
7. Minimum possible T_{CYC}. Actual $T_{CYC} = T_{CAC}$ + FPGA data setup time. With V_{CCO} = 3.3V, if FPGA data setup time = 15 ns, actual T_{CYC} = 15 ns + 15 ns = 30 ns.

AC Characteristics Over Operating Conditions When Cascading



Symbol	Description	XAF01S, XAF02S, XAF04S		Units
		Min	Max	
T_{CDF}	CLK to output float delay(2,3) when V_{CCO} = 2.5V or 3.3V	-	25	ns
	CLK to output float delay(2,3) when V_{CCO} = 1.8V	-	35	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 2.5V or 3.3V	-	20	ns
	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 1.8V	-	35	ns
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	-	20	ns
	$\overline{CE}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	-	35	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	-	20	ns
	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	-	35	ns
T_{COCE}	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 2.5V or 3.3V	-	-	ns
	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 1.8V	-	-	ns
T_{CODF}	CLKOUT to output float delay when V_{CCO} = 2.5V or 3.3V	-	-	ns
	CLKOUT to output float delay when V_{CCO} = 1.8V	-	-	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascaded PROMs:
   - T_{CYC} min = T_{OCK} + T_{CE} + FPGA data setup time
   - T_{CAC} min = T_{OCK} + T_{CE}

Pinouts and Pin Descriptions

The XAFxxS Platform Flash PROM is available in the VOG20 packages.

- Table 9, **XAFxxS Pin Names and Descriptions**, page 21
- Figure 9,**VOG20 Pinout Diagram (Top View) with Pin Names**, page 22

- Notes:

1. VOG20 denotes a 20-pin (TSSOP) Plastic Thin Shrink Small Outline Package

XAFxxS Pinouts and Pin Descriptions

Table 9 provides a list of the pin names and descriptions for the XAFxxS 20-pin VOG20 package XAFxxS Pinout diagrams.

Table 9: **XAFxxS Pin Names and Descriptions**

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	20-pin TSSOP (VOG20)
D0	4	Data Out	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped).	1
	3	Output Enable		
CLK	0	Data In	Configuration Clock Input. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High.	3
OE/$\overline{RESET}$	20	Data In	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is not programmable.	8
	19	Data Out		
	18	Output Enable		
$\overline{CE}$	15	Data In	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.	10
$\overline{CF}$	22	Data Out	Configuration Pulse (Open-Drain Output). Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.	7
	21	Output Enable		
$\overline{CEO}$	12	Data Out	Chip Enable Output. Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	13
	11	Output Enable		
TMS		Mode Select	JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the device if the pin is not driven.	5
TCK		Clock	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	6
TDI		Data In	JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the device if the pin is not driven.	4
TDO		Data Out	JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the system if the pin is not driven.	17

Table 9: **XAFxxS Pin Names and Descriptions *(Continued)***

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	20-pin TSSOP (VOG20)
VCCINT			+3.3V Supply. Positive 3.3V supply voltage for internal logic.	18
VCCO			+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.	19
VCCJ			+3.3V, 2.5V, or 1.8V JTAG I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.	20
GND			Ground	11
DNC			Do not connect. (These pins must be left unconnected.)	2, 9, 12, 14, 15, 16

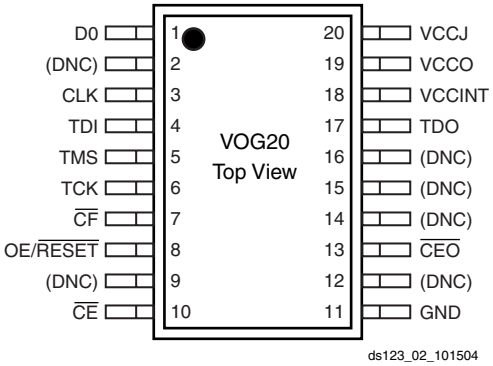


Figure 9: **VOG20 Pinout Diagram (Top View) with Pin Names**

Ordering Information

XAF04S VOG20 Q

Device Number

XAF01S
XAF02S
XAF04S

Package Type

VOG20 = 20-pin TSSOP Package, Pb-free

Operating Range/Processing

Q= (T_A = –40° C to +125° C)

Valid Ordering Combinations

XAF01SVOG20 Q
XAF02SVOG20 Q
XAF04SVOG20 Q

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/18/04	1.0	Xilinx Initial Release.