MA8112

DIGITAL SWITCH MODULE (DSM)

The MA8112 is a CMOS device providing digital switching for up to 256 8-bit channels as used in PCM or data systems 8-bit words are received and transmitted at 2 048 Mb/s on each of eight input and eight output lines respectively either in a parallel format whh 256 consecutive channels or in serial format with 32 channels multiplexed on to each of the eight lines.

The device operates unidirectionally and allows 8-bit words from any incoming channel to be switched to any outgoing channel, under the control of an on-chip connection memory, which may be updated or interrogated via an external control interface The control interface and addressing facilities are designed to allow easy expansion to provide greater switching capacity

Applications include PCM switching systems in which up to 32 x 64Kb/s speech/data channels are time division multiplexed onto a single line in accordance with CCITT Recommendation G732 2 048Mb/s format

Alternatively, the device can be used as a high speed data switch at data rates up to 2 048 Mb/s and can be used to convert 8-bit channels from serial to parallel format or vice versa

The MA8112 is pin-compatible with the MS2002

FEATURES

- Single 5V Supply
- Low Power CMOS Design
- Inputs and Outputs TTL Compatible
- Compatible with CCITT 32-Channel 2.048 Mb/s Format (Rec. G732)
- 256 Input/256 Output Channels
- Inputs and Outputs can be Serial or Parallel
- Variable Input/Output Frame Delay
- Designed to allow Easy Expansion into Larger Switches Matrices

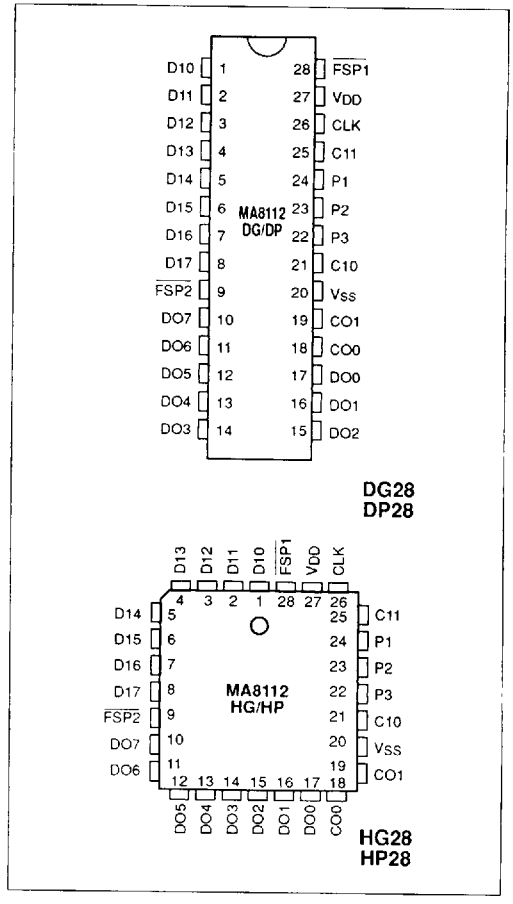

Figure 1 Pin connections - top view

FUNCTIONAL DESCRIPTION

The MA8112 Digital Switch Module is designed to provide switching for 256 x 8-bit PCM encoded speech or data channels operating at rates upto 2.048 Mb/s. The input and output data is handled in frames containing 256 8-bit channels in either serial or parallel format and repeating at a rate of up to 8 kHz. The format of these frames is shown in Fig.3. When operating at 2.048 Mb/s in serial input/output mode, 32 channels each operating at a rate of 64 kb/s are multiplexed on to each line according to CCITT specifications for PCM transmission (Recommmendatbn G732).

The input frame to output frame delay is variable (up to one frame perbd) with the input channel data stored on chip until being sent to the appropriate output channel. The switching of any input channel is independent of any other channel and once set up, the connection between an input channel and an output channel is maintained until a new connection is specified via the control interface.

Switching is achieved as follows:

The MA8112 contains two read/write memories- the SPEECH (i.e. PCM) memory and the CONNECTION memory.

In the speech memory, there is one 8-bit location dedicated to each of the 256 8-bit PCM (speech) input channels. In each frame of incoming data, each 8-bit PCM word will be written to a location in the speech memory according to its input channel. This operation is repeated in successive frames.

In the connection memory, there is one location dedicated to each of the 256 PCM output channels. Each of these locations contains an 8-bitt word which is used to address one of the 256 locations in the speech memory (and hence one of the 256 input channels). The PCM word contained in this location is then sent to the output channel concerned. Thus switching of an 8-bit word between an input channel and an output channel is achieved.

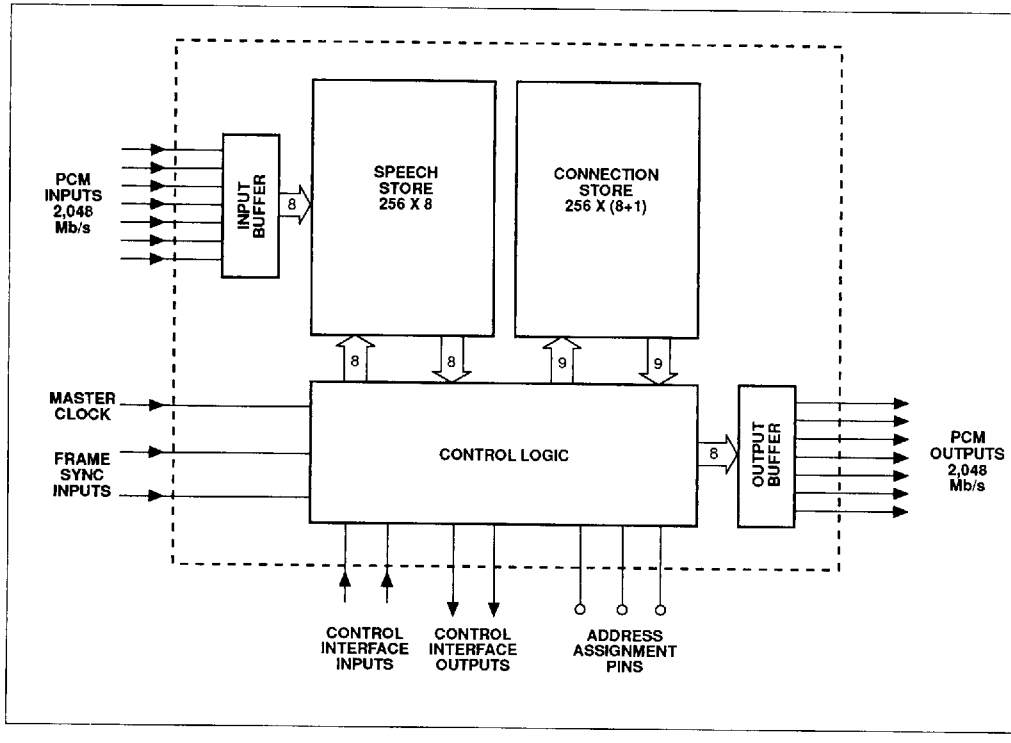

Figure 2 MA8112 block diagram

PIN DESCRIPTION

No.	Name	Function and Description
1 - 8	DI0- DI7	SPEECH DATA INPUTS. These inputs carry the 256 8-bit channels (containing PCM encoded speech or datal in either serial or parallel format for switching. All eight input lines must be bit and timeslot synchronous. The start and format (i.e. serial or parallel) of an input frame is determined by the input frame synchronisation pulse on Pin 28($\overline{FSP1}$). Input and output channels are formatted and numbered as shown in Fig. 3 and the input channel timing is shown in Fig. 4.
10 - 17	DO7 - DO0	SPEECH DATA OUTPUTS. These outputs carry the 256 8-bit channels containing PCM encoded speech or data) in either serial or parallel format after switching. All eight output lines are bit and timeslot synchronous. The timing of the output frame relative to the input frame is determined by the input to Pin 9 (FSP2). These outputs are open-drain type and should be tied externally to V_{DD} using 1Kohm resistors.
9 28	$\overline{FSP2}$ $\overline{FSP1}$	FRAME SYNC PULSE INPUTS. A frame sync pulse input on $\overline{FSP1}$ provides a frame datum for the incoming data (on both the speech and control inputs) and indicates the active edges of the system clock. In addition the duration of the sync pulse low period determines the speech data input and output formats (i.e. serial or parallel) as shown in Table 1. The $\overline{FSP2}$ input is used to define the start of the output frame. If no frame sync pulse is provided on FSP2, the output frame will automatically start 21 bits after $\overline{FSP1}$ (mode 1), and will be timed by the negative clock edges alternate to those used for clocking the input frame.
22 - 24	P3 - P1	ADDRESS ASSIGNMENT PINS. These pins are each hardwired to V_{DD} Or V_{SS} in order to assign a unique address for up to eight DSMs in a matrix. This allows several DSMs to share the same control interface lines (CI0, CI1 and CO0, CO1).
21, 25	CI0, CI1	CONTROL INTERFACE INPUTS. These are serial control inputs into which all instructions and data regarding the addressing of the DSM, routing of the PCM inputs and outputs and channel insertion and extraction are entered. CI1 is the control instruction input. 8-bit words entered on CI1 correspond to, and control the 8-bit words entered synchronously on CI0, the control data input.
18, 19	CO0, CO1	CONTROL INTERFACE OUTPUTS. These are serial outputs which respond to the words received on the control interface inputs There is a fixed response time of 21 bit periods between a control interface input word and the corresponding control interface output word. The control instruction output CO1 carries 8-bit words which refer to the words carried on the control data output CI0. These outputs are used to extract data from either the speech or connection memories. CO0 and C01 are open drain outputs and should be tied high externally using 1Kohm resistors.
26	CLK	MASTER CLOCK INPUT. This input requires a 4.096 MHz TTL level clock. All input signals are strobed on alternate falling clock edges (the active edge is assigned by the position of the input frame sync pulse FSP1). All output data is clocked out on the opposite alternate negative edges of the clock
20	V_{SS}	NEGATIVE POWER SUPPLY PIN. Connect to 0v.
27	V_{DD}	POSITIVE POWER SUPPLY PIN Connect to + 5v.

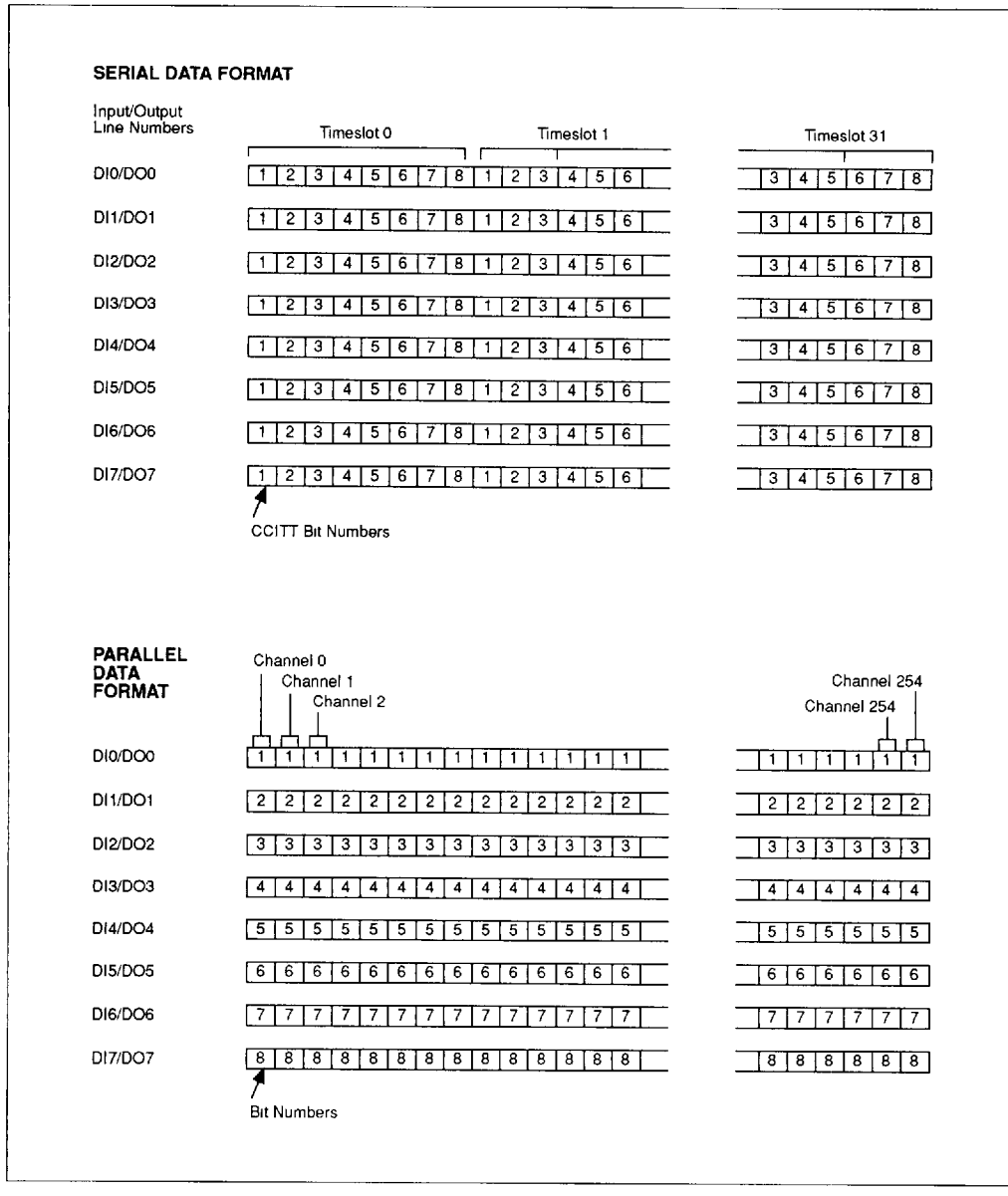

Figure 3 Input and output data formats

INTERFACE DESCRIPTION

TIMING INTERFACE

The following timing information signals must be provided to the MA8112:

(a) A 4.096 MHz master clock on CLK (Pin 26).

(b) An input frame synchronisation pulse on $\overline{FSP1}$ (Pin 28). This pulse must repeat every 125µs (i.e. every 512 master clock periods).

(c) (Optional).An output frame synchronisation pulse on FSP2 (Pin 9) which repeats every 125µs (512 master clock periods). If this is not provided, the MA8112 will default to assuming a start time for the output frame 21 bit periods after $\overline{FSP1}$.

The master clock is used to strobe all data into and out of the DSM. Data is clocked in on the speech data inputs (DI0-7) and the control interface inputs (CI0, CI1) on alternate falling edges of the master clock. The first active edge of the master clock in each frame is assigned by the timing of the input frame sync pulse $\overline{FSP1}$, as shown in Fig. 4.

$\overline{FSP1}$ also indicates a frame datum for the speech data inputs and control interface inputs, thereby allowing an input channel to be identified by its input line and/or input timeslot (Fig.4). The length of the frame sync pulse low period is used to determine the format of the data on the speech data inputs and outputs.

The input and output formats are explained in the Data Interface description.

The input frame sync pulse must repeat every 512 master clock periods to denote the start of each input frame.

The output frame sync allows the start of each output frame to be denoted in the same way as the input frames. If no pulse is provided on $\overline{FSP2}$, then the output frame starts 21 bits after the $\overline{FSP1}$ automatically. As $\overline{FSP2}$ is internally tied high by a resistor, it may be left open circuit.

Zero frame delay is achieved by tying $\overline{FSP2}$ to $\overline{FSP1}$.

The length of the pulse on $\overline{FSP2}$ has no relevance to the operation of the MA8112.

Length of FSP1 low period (clock periods)	Format
1	Serial In, Serial Out (SISO)
2	Serial In, Parallel Out (SIPO)
3	Parallel In, Serial Out (PISO)
4	Parallel In, Parallel Out (PIPO)

Table 1

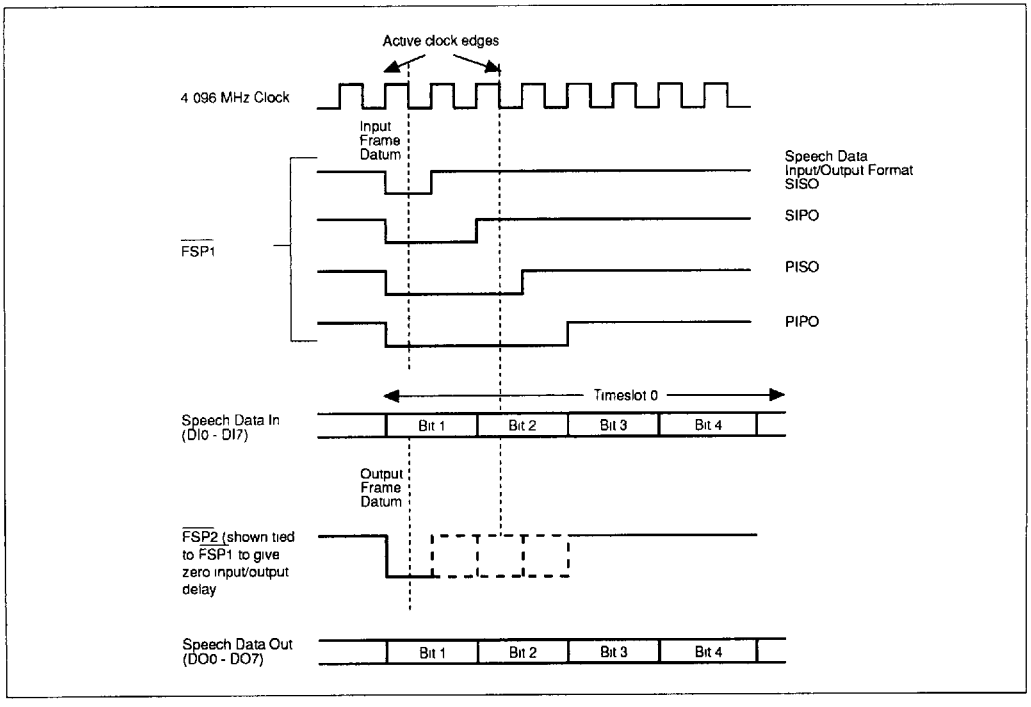

Figure 4(a): DSM timing diagram

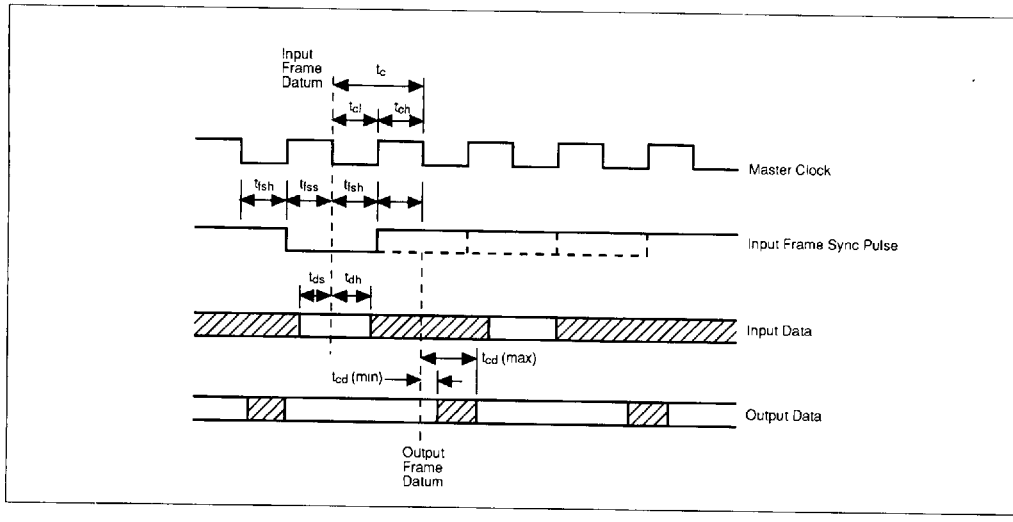

Figure 4b Timing diagram

DATA INTERFACE

The data interface consists of eight input lines DI0-7 and eight output lines DO0-7 Input and output lines carry data at a rate of 2.048Mb/s. This allows 256 8-bit PCM or data channels repeating at a rate of 8 kHz to be switched from the input lines to the output lines.

The data on both the input and output lines is in frames arranged either as 32 serial 8bit channels on each of the eight input or output lines or, as 256 consecutive 8-bit parallel words on the eight input or output lines These formats and the numbering scheme for the channels are shown in Fig.3. Any combination of parallel or serial input or output formats is possible and may be selected by the length of the input frame sync pulse on $\overline{FSP1}$ as explained in the timing interface description.

The input frames are clocked in by alternate negative edges of the master clock All input lines must be both bit and channel synchronous with each other The output frames are clocked on the other alternate negative edges to the input frames.

Outputs are open drain type and should be connected via a 1kohm resistor to V_{DD}. This allows several DSMs to be wire-ORed on to the same PCM lines in a matrix configuration

CONTROL INTERFACE

The control interface consists of two input lines (CI0 and CI1) and two output lines (CO0 and CO1) The operation of the control interface is summarised in Table 2

Control Interface Inputs

The two input lines receive data in the form of serial 8-bit words at the same rate, and synchronised with the data input lines DI0-DI7. Thus, 32 8bit words are received per frame

Each 8-bit control instruction word received on CI1 corresponds to and controls the processing of the 8-bit control data word received in the same timeslot on CI0.

(a) Control Instruction word

The control instruction word format is shown in Fig. 5-

Each control instruction word refers to a specific connection memory location (and hence, also to a specific output channel) The connection memory location is addressed by a combination of the timeslot number in which the word is received and the three bits A0, A1, A2 within the control instruction word.

Bits S3, S2 and S1 are used to identify a particular DSM in an array These bits are compared to the hardwired address assignment pins, P3, P2 and P1 If they match, the control instruction word is intended for this particular DSM and the DSM will respond accordingly (this is the normal mode in an application using only one DSM).

However, if P3 and S3 match, but either or both S2 and S1 do not match P2 and P1, the DSM will recognise that the message is intended for another DSM which shares the same control interface and speech data lines within a matrix (see Application note) This does not mean that the message is completely ignored If the message specifies a write operation to a location in another DSM's connection memory, then this DSM will fill its corresponding location with all 1s(including B_{INT}) in order that its speech data output will go open drain on the same output line and timeslot as that of the addressed DSM This facility allows a DSM matrix to operate particularly efficiently, as several DSMs can be wire-ORed onto the same control lines and when a new connection on to an output channel is made, previous connections from other DSMs are automatically removed

In the case of a mismatch between S3 and P3, the control instruction word and the control data word are completely ignored as it is assumed that the message is for a DSM with outputs connected to other lines

The R/$\overline{W}$bit is the read/write bit. H R/$\overline{W}$ = 0 the operation is a write operation then (subject to an address match on S3, S2 and S1) new data will be written to the appropriate connection memory location. This new data will consist of the 8-bit control data word loaded synchronously on CI0 and the external busy bit, B_{EXT} from the control instruction word. B_{EXT} then becomes the internal busy bit B_{INT}, a ninth bit attached to the eight data bits in each connection memory location. If B_{INT} = 0, then an input channel to output channel connection is made, the location of the word in the connection memory indicating the output channel and the 8 bits at that location (loaded on CI0) indicating the input channel to be switched to the output channel. H B_{INT} = 1, the 8 bits in the connection memory are switched directly to the output channel. This facility allows an idle code to be inserted via the control interface when an output channel is unused.

(b) Control data word

Fig.5 shows the three possible formats for the control data word loaded synchronously with the control instruction word. If R/$\overline{W}$ = 0 and B_{EXT}= 0 in the CIW, one of the first two formats should be used (depending upon whether the speech data format is serial or parallel). If B_{EXT} = 1, the third format should be used as this is data to be sent to an output channel.

H R/W = 1 in the corresponding control instruction word, then the operation is a read and the data on CO0 is irrelevant.

Control Interface Outputs

The two control interface output lines, C01 and CO0 (Pins 19 and 18) transmit data in the form of serial 8-bit words in response to messages received on the control instruction input CI1. The outputs operate at the same data rate as the inputs(i.e.328-bit words per frame) and are synchronous with each other, each control instruction output word transmitted on C01 corresponding to the accompanying control data output word on CO0.

The delay time from input messages on CI0 and CI1 to the response messages on CO0 and C01 is 21 bit periods (the outputs are clocked on the other alternate falling edges of the master clock to the inputs). This is a fixed delay and does not vary with the input/output frame delay.

(a) Control Instruction output word

The format of the control instruction output word is shown in Fig.6. The information carried on C01 relates to the data on CO0. As explained earlier, each pair of control interface words on CI0 and CI1 refer to as pecific connection memory location, therefore, the control interface output words which form a response will also refer to the same connection memory location.

If the S3 bit in the control instruction word input on CI1 does not match P3, then the input message is ignored and the control interface outputs, C01 and CO0 will go open - drain (i.e. all 1 s) during the response timeslot.

When S3 = P3 on CI1, then the response word on C01 will always contain a reflection of the connection memory addressing bits A0, A1 and A2 and the R/$\overline{W}$ (read/write) bit on CI1. This information, together with the timeslot during which the output words are transmitted, provides the information on whether the input message was a read or write operation and which connection memory location (and, therefore, output channel) is being referred to. The remaining bits of the control instruction output word and the data contained in the corresponding word on COO will depend upon the operation being performed and the contents of the connection memory.

When R/$\overline{W}$ = 0 on CI1 (i.e. a write operation), then the corresponding control data output word on CO0 will reflect the new connection memory contents at the specified location and B_{INT} will, similarly, be reflected on C01. If the new contents of the connection memory location is all 1s, including B_{INT} (because either the input message was addressed to another DSM in a matrix or because all 1 s were specifically written to this location in this DSM) this will be reflected by the control data output CO0 going open - drain during the relevant timeslot. Also the S1, S2 and S3 bits on C01 will be set to one. If the word on CI1 was specifically addressed to this DSM and the connection memory location contents is not all 1 s, then S1, S2 and S3 will reflect the address of this DSM (i.e. P1, P2 and P3). As only one DSM in a matrix can have anything other than all 1 s in corresponding connection memory locations (because only one device can be active in a PCM output channel at a time) this arrangement ensures that only this DSM responds with the address in the relevant timeslot.

When R/$\overline{W}$ = 1 on the control instruction word on CI1 (i e. a read operation) the data input on CIO is irrelevant. It is not necessary to specify which DSM is to be read from by matching S1 and S2 to P1 and P2 because when used on a matrix, only one of the DSMs with output lines wired together will contain any data other than all 1s in the connection memory location which is to be read. Therefore, only one DSM will respond to the read instruction by transmitting data on CO0 and a reflection of its address on C01 - other DSMs will go open-drain at the appropriate time. The status of the B_{EXT} bit in the control instruction input word determines whether the read operation refers to reading the word in the connection memory location or reading the PCM output channel associated with this location. If B_{EXT} = 0, the connection memory is read. If B_{EXT} = 1, the output channel word is read - this may be the word from the speech memory addressed by the contents of the connection memory or the word from the connection memory itself, depending upon the status of B_{INT} appended to this location

(b) Control data output word

The four possible control data output word formats are shown in Fig. 6. Which format is applicable is determined by the information requested, and the format in which this data is stored on chip

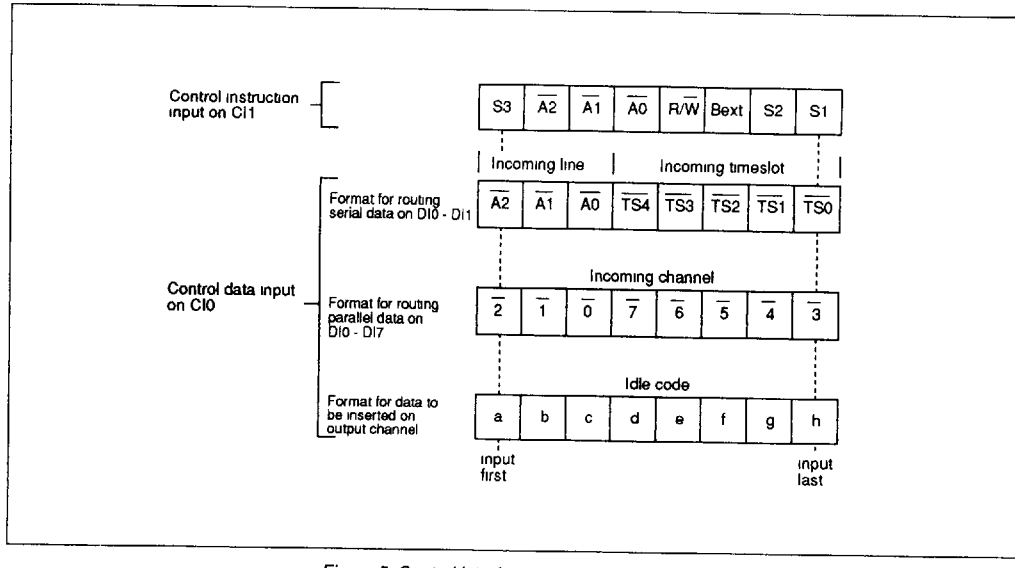

Figure 5: Control interface input message formats

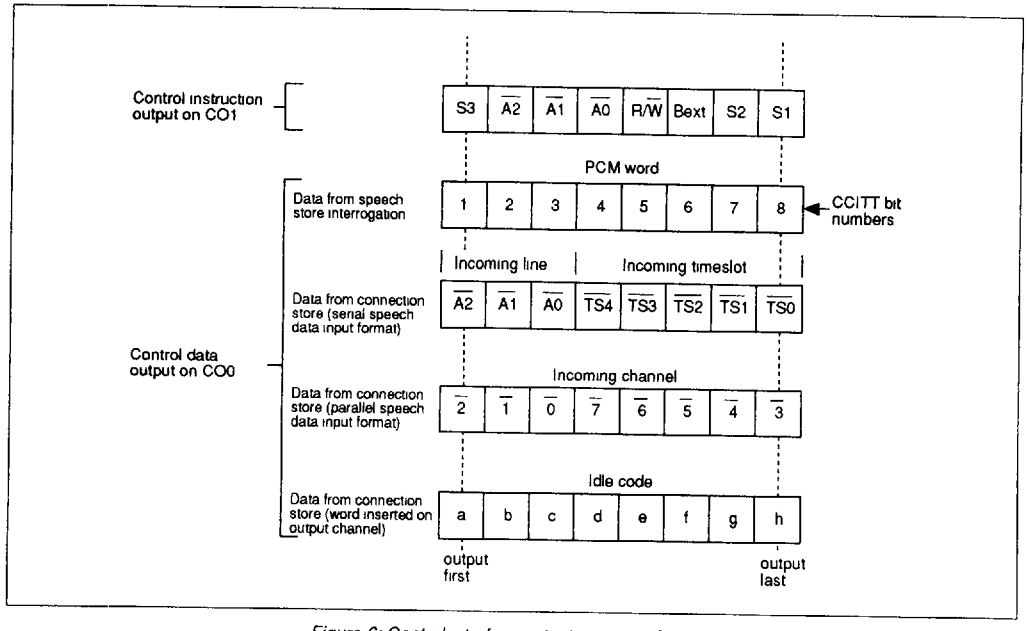

Figure 6: Control interface output message formats

Table 2: Control interface operation

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ADDITIONAL NOTES

CHANNEL NUMBERING

When the DSM is operated in a mixed input/output format mode, i.e. Serial In, Parallel Out, or Parallel In, Serial Out, it is necessary to be able to equate channel numbers.

MSB							LSB
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

In serial mode, a channel number is identified by taking the line number and timeslot number and assembling them as follows:

MSB							LSB
TS4	TS3	TS2	TS1	TSO	A2	A0	A1

DSM INTERNAL DELAYS

There is a fixed minimum internal delay through the DSM for PCM words which is that produced by format conversion and the memory read/write cycle within the DSM. This delay is 21 bit periods (i.e. 42 master clock periods) and is the shortest period in which an input word can be sent to an output channel.

If the $\overline{FSP2}$ input is left open circuit, then the fixed delay will be 21 bit periods, but if an output frame sync pulse is provided, the fixed delay will be up to 255 bit periods longer, dependent upon the timing of the $\overline{FSP2}$ relative to $\overline{FSP1}$.

The total delay tor any particular channel is equal to this fixed delay plus a variable delay determined by the time spent in the speech memory waiting for the relevant output timeslot.

The overall delay is given by the following relation:

$$\left.\begin{aligned} D &= F + (N - M) \text{ for } N \geq M \\ D &= F + 256 + (N - M) \text{ for } N < M \end{aligned}\right\} \text{ PIPO format}$$

$$\left.\begin{aligned} D &= F + \left(\text{INT}\frac{N}{8} - \text{INT}\frac{M}{8}\right) \times 8 \text{ for } N \geq M \\ D &= F + 256 + \left(\text{INT}\frac{N}{8} - \text{INT}\frac{M}{8}\right) \times 8 \text{ for } N < M \end{aligned}\right\} \text{ SISO format}$$

where

D = total delay in bit periods (488ns)
F = fixed delay in bit periods (21 bits or specified by FSP2)
M = Incoming channel number
N = Outgoing channel number

APPLICATIONS INFORMATION

Fig.7 shows how a 1024-channel DSM matrix can be constructed, providing four times the switching capacity of a single DSM. Note that the control interface allows DSMs connected to the same PCM output lines to be wire-ORed to common interface lines without additional logic.

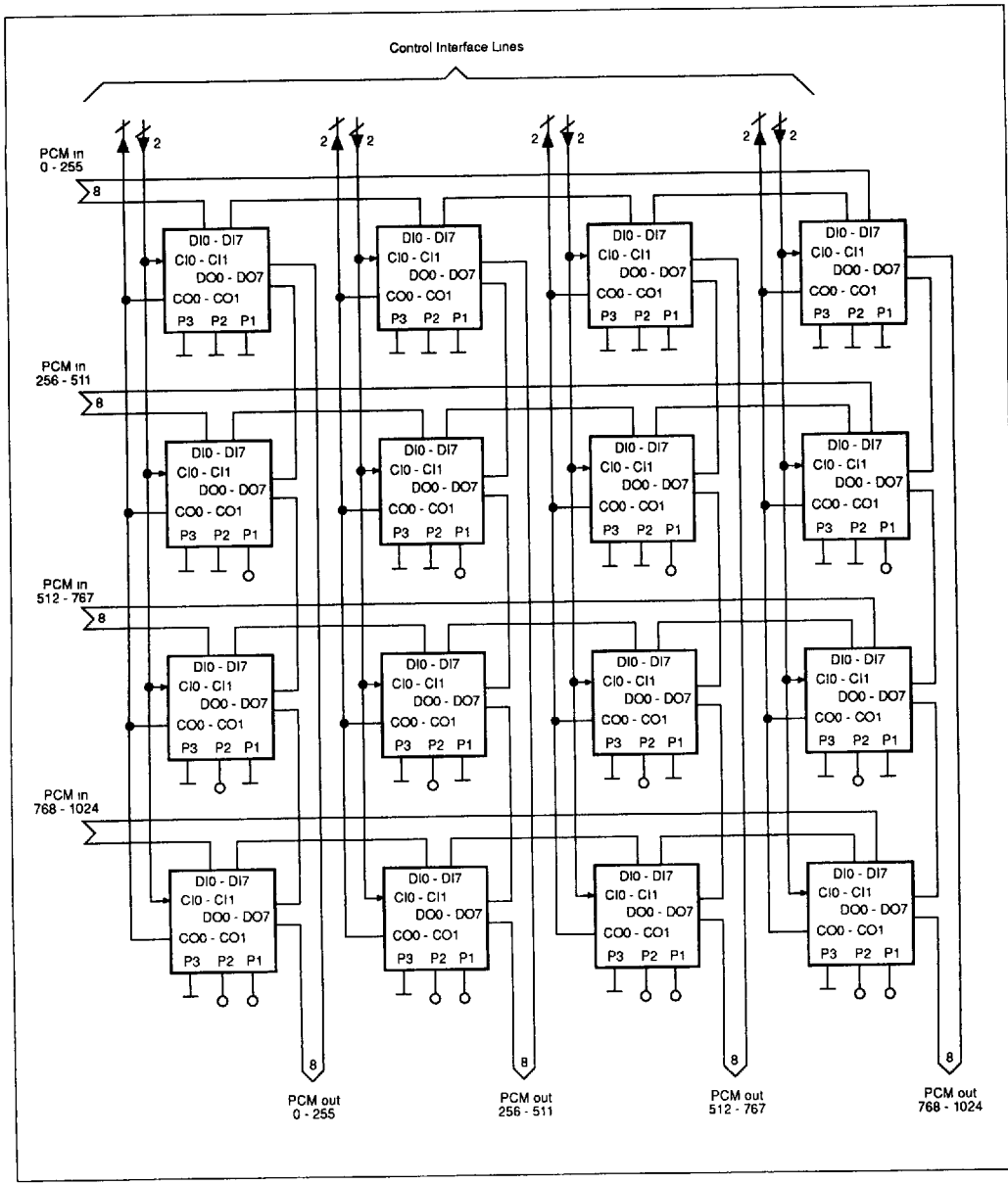

Figure 7

ABSOLUTE MAXIMUM RATINGS*

	Max	Units	Min
Supply voltage V_{DD}	-0 3	6.5	V
Voltage on any pin	V_{SS}-0.3	V_{DD}+0.3	V
Operating temperature	0	70	°C
Storage temperature	-55	+ 125	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS at V_{DD} = 5V ±%, Ambient temperature = 25°C

	Symbol	Min	Typ	Max	Units	Conditions
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}	-0.3		0.8	V	
Supply current			<5	10	mA	CLK=4.096 MHz
Input current	I_{IH}			10	µA	$V_{IH} = V_{DD} + 0.3V$
	I_{IL}			10	µA	-0.3V V_{IL} 0.8V except Pin 9
				100	µA	-0.3V V_{IL} 0.8V Pin 9
Low level output voltage	V_{OL}			0 4	V	Rpu = 1 Kohm
High level output voltage	V_{OH}	2.8			V	Rpu = 1 Kohm
Input capacitance	C_I			5	pF	
Output capacitance	C_O			5	pF	

AC ELECTRICAL CHARACTERISTICS † at V_{DD} = 5V ±5%, Ambient temperature 0 to + 70°C

	Symbol	M in	Typ	Max	U nits	Conditiom
Master clock period	t_c	240	244	2400	nS	
Master clock low period	t_{cl}	80			nS	
Master clock high period	t_{ch}	80			nS	
Frame sync period	t_f	512		512		Master clock periods
Frame sync set up time	t_{fss}	50			nS	
Frame sync hold time	t_{fsh}	50			nS	
Input data set up time	t_{ds}	50			nS	
Input data hold time	t_{dh}	50			nS	
Master clock to output delay	t_{od}	5		150	nS	

† See Fig. 4(b)