PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD82821

2-PORT 25M ATM PHY LSI

DESCRIPTION

The μPD82821 is an ATM physical layer LSI IC that complies with ATM25 (25.6 Mbps) and which supports TC sublayer and PMD sublayer functions. Interfacing with the ATM layer and AAL layer LSI is implemented at UTOPIA Level 2.

FEATURES

- Provides a 25.6-Mbps ATM PHY (PMD & TC) function for two ports
- Conforms to the ATM Forum PHY interface specifications (af-phy-0040.000 November 1995).
- UTOPIA Level 2 V1.0 (af-phy-0039.000 June 1995: max. 8 bits/40 MHz) interface
- Direct Status Indication support for each of the two ATM25 Ports
- Three-cell built-in transmit/receive FIFOs for each circuit
- PMD sublayer functions:
  - (a) Built-in clock recovery.
  - (b) Built-in equalizer.
- TC sublayer functions:
  - (a) NRZI encoder/decoder.
  - (b) Command byte insertion/detection.
  - (c) 4B/5B encoder/decoder.
  - (d) Cell scrambler/descrambler.
  - (e) HEC generation/verification.
- CPU interface: Intel or Motorola can be selected.
- Supports STP and UTP (Categories 3, 4, 5).
- Loopback function: available in the PMD and ATM layers.
- Operation And Maintenance (OAM) functions: Input failure detection, HEC error detection and 4B/5B code error detection.
- Test function: Supports JTAG.
- 5 V tolerant buffers on all pins with Receive Buffers
- Power supply voltage: 3.3 V ± 5 %.

ORDERING INFORMATION

Part Number	Package
μPD82821GJ-031-3ED	120-pin plastic QFP (fine pitch) (20 x 20 mm)

Remark: This document indicates active low pins in the format of “xxx_B” (_B after the pin name).

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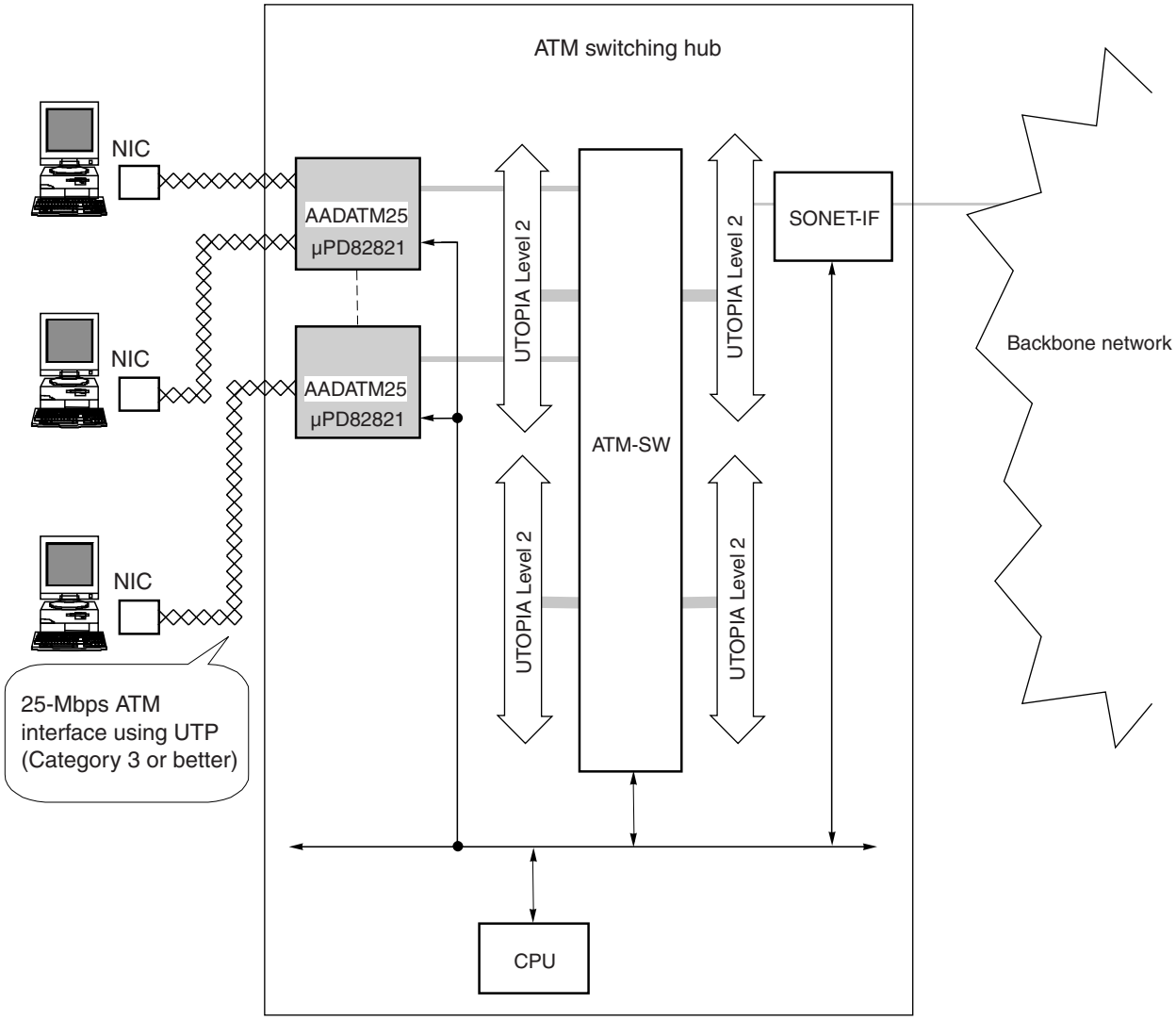
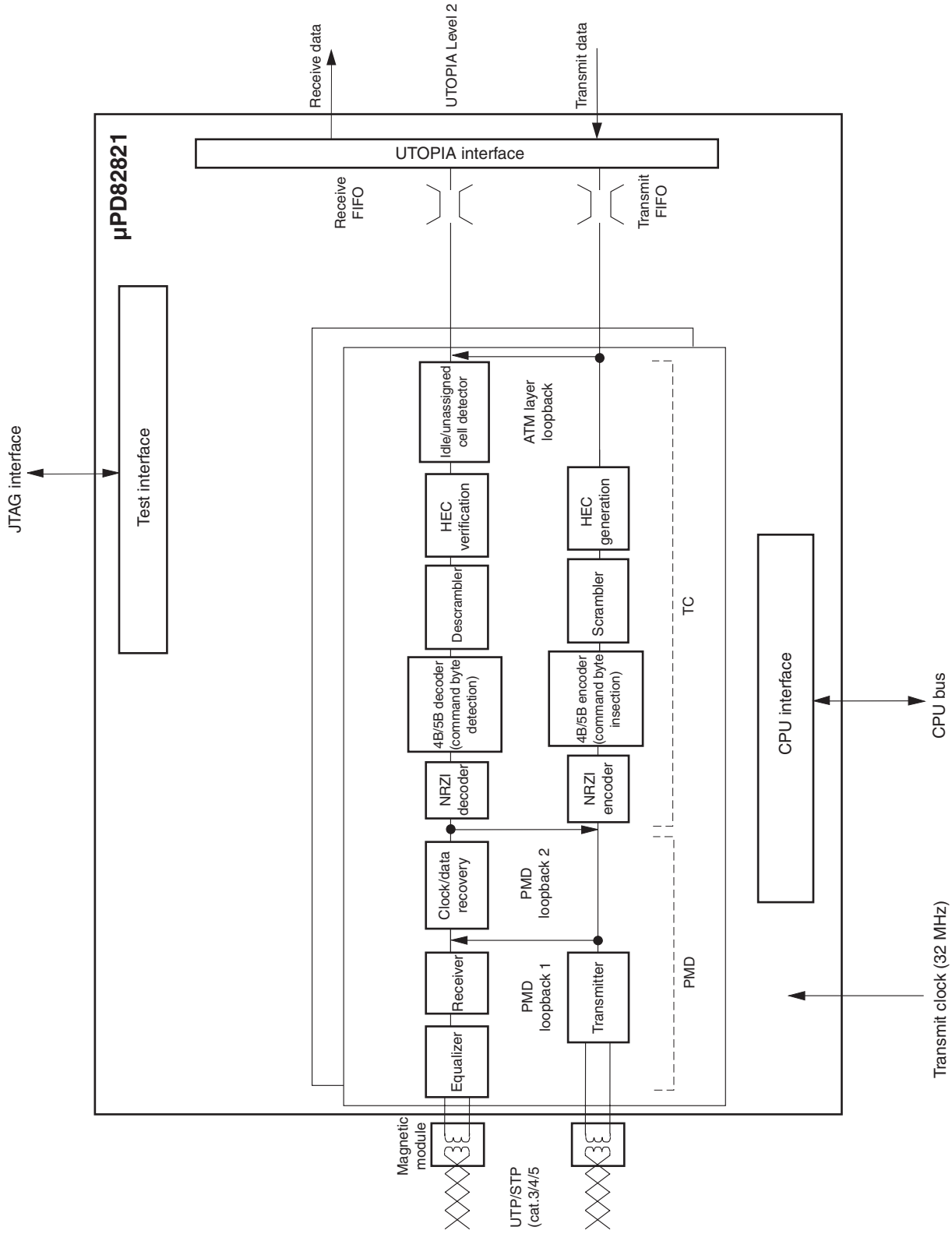
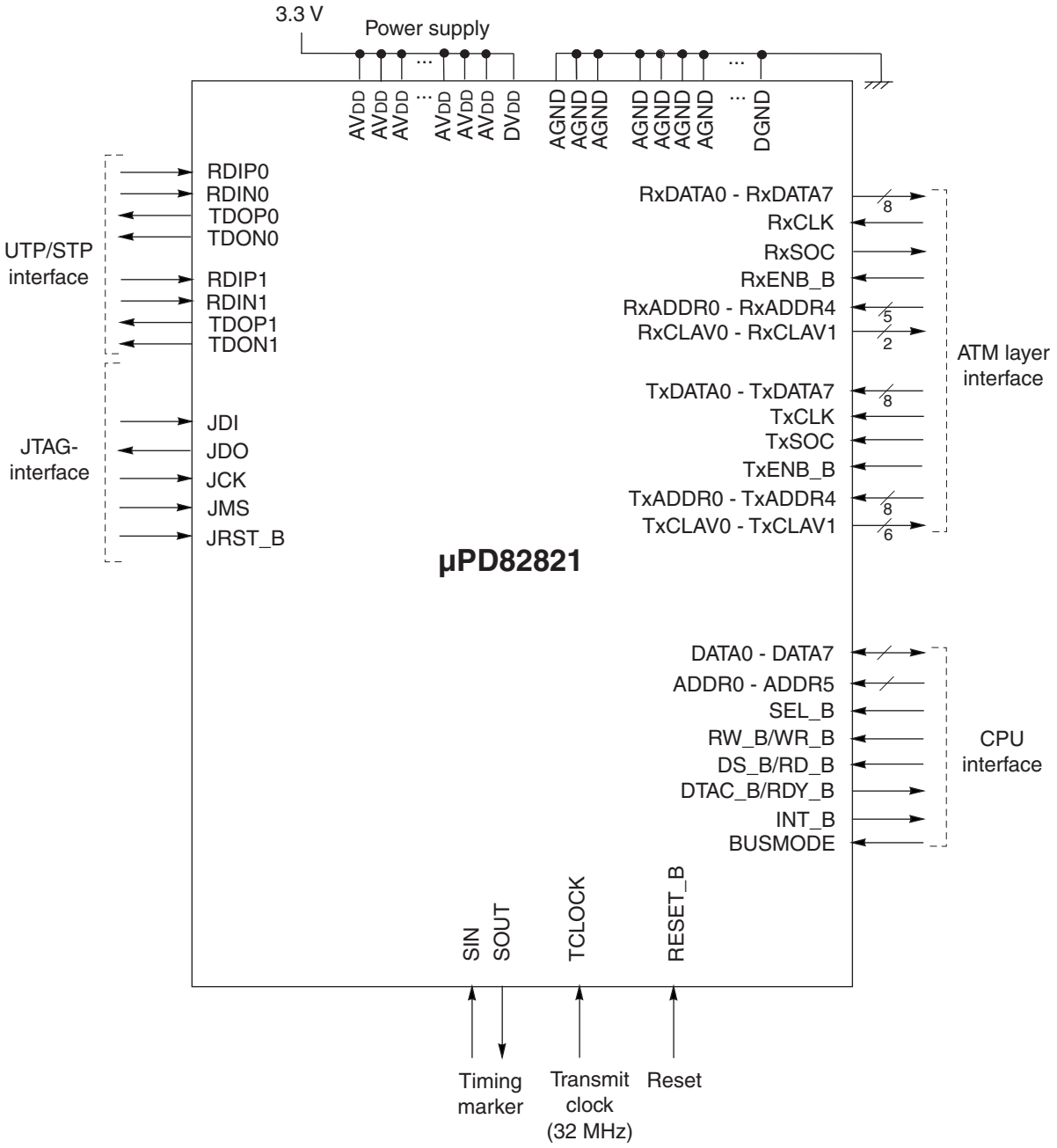
System Configuration Example (Aplication)



Block Diagram

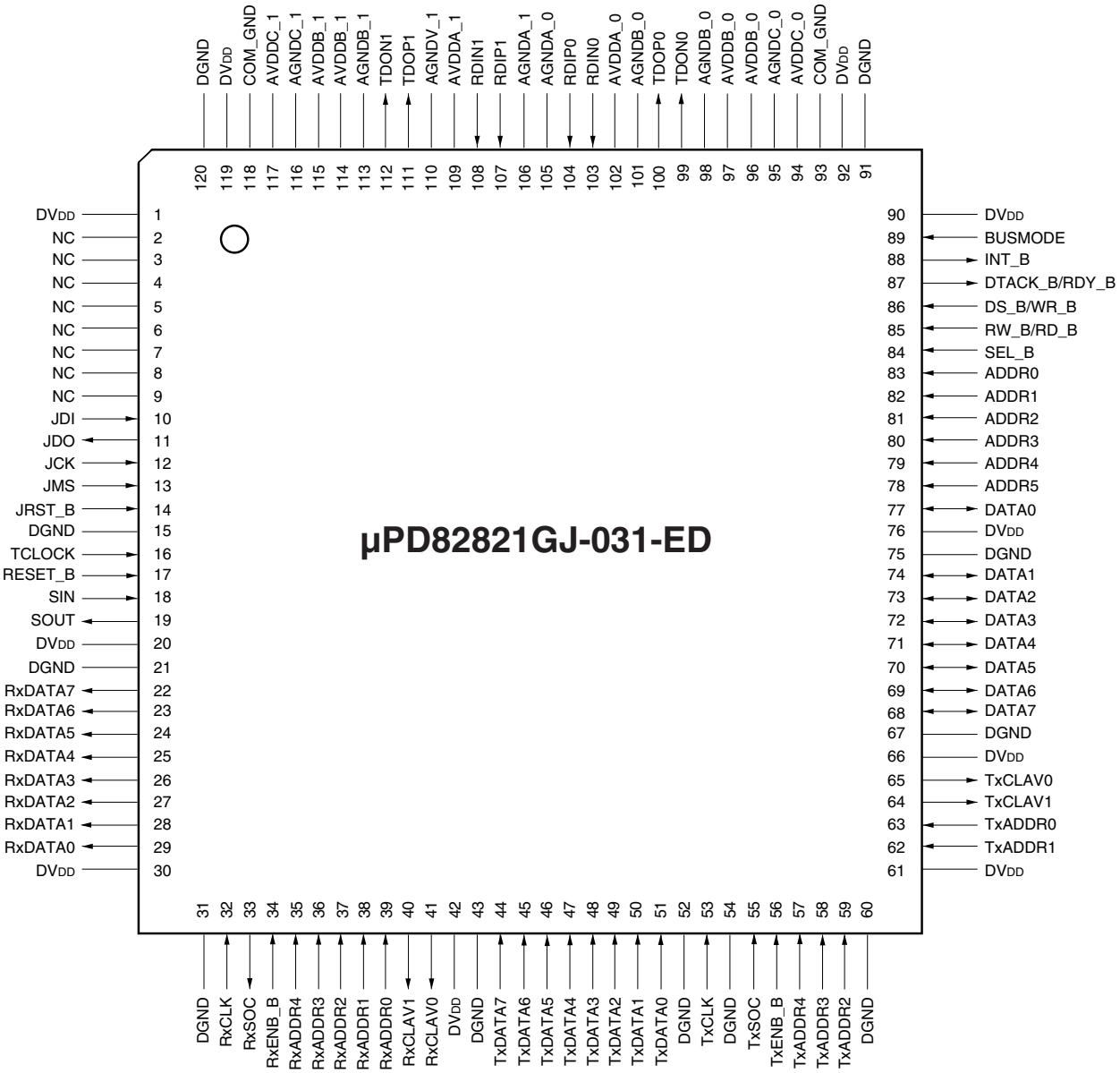


Pin Layout


3.3 V
Power supply
AVDD
AVDD
AVDD
AVDD
AVDD
AVDD
DVDD
AGND
AGND
AGND
AGND
AGND
AGND
AGND
DGND
UTP/STP interface
RDIP0
RDIN0
TDOP0
TDON0
RDIP1
RDIN1
TDOP1
TDON1
JTAG-interface
JDI
JDO
JCK
JMS
JRST_B
μPD82821
RxDATA0 - RxDATA7
RxCLK
RxSOC
RxENB_B
RxADDR0 - RxADDR4
RxCLAV0 - RxCLAV1
TxDATA0 - TxDATA7
TxCLK
TxSOC
TxENB_B
TxADDR0 - TxADDR4
TxCLAV0 - TxCLAV1
8
5
2
8
8
6
ATM layer interface
DATA0 - DATA7
ADDR0 - ADDR5
SEL_B
RW_B/WR_B
DS_B/RD_B
DTAC_B/RDY_B
INT_B
BUSMODE
CPU interface
SIN
SOUT
TCLOCK
RESET_B
Timing marker
Transmit clock (32 MHz)
Reset

Pin Configuration

120-pin plastic QFP (fine pitch) (20 x 20 mm)



Pin Names

ADDR0-ADDR5	: Address	RxADDR0-RxADDR4	: Receive Address
AGND	: Analog Ground		
AV_{DD}	: Analog Supply Voltage	RxCLAV0-RxCLAV1	: Receive Cell Available
BUSMODE	: Bus Mode	RxCLK	: Receive Data Clock
CG	: Connect GND	RxDATA0-RxDATA7	: Receive Data
DATA0-DATA7	: Data	RxENB_B	: Receive Enable
DGND	: Digital Ground	RxSOC	: Receive Start Address of ATM Cell
DS_B/RD_B	: Data Strove/Read		
DTACK_B/RDY_B	: Data Acknowledge/Ready	SEL_B	: Chip Select (CPU Interface)
DV_{DD}	: Digital Supply Voltage	SIN	: Signal In (X_8 timebase in)
IC	: Internal Connect	SOUT	: Signal Out (X_8 timebase out)
RCLK0- RCLK1	: Receive Clock	TCLOCK	: Transmit Clock
RDATA0- RDATA1	: Receive Data	TDON0-TDON1	: Transmit Data Output Negative
TCLK0-TCLK1	: Transmit Clock	TDOP0-TDOP1	: Transmit Data Output Positive
TDATA0- TDATA 1	: Transmit Data	TxADDR0-4	: Transmit Address
INT_B	: Interrupt	TxCLAV0-TxCLAV1	: Transmit Cell Available
JCK	: JTAG Test Clock	TxCLK	: Transmit Data Clock
JDI	: JTAG Test Data Input	TxDATA0-TxDATA7	: Transmit Data
JDO	: JTAG Test Data Output	TxENB_B	: Transmit Enable
JMS	: JTAG Test Mode Select	TxSOC	: Transmit Start Address of ATM Cell
JRST_B	: JTAG Test Reset		
RDIN0-RDIN1	: Receive Data Input Negative		
RDIP0-RDIP1	: Receive Data Input Positive		
RESET_B	: Reset		
RW_B/WR_B	: Read Write/Write		

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1. PIN FUNCTIONS

1.1 Power Supply

Table 1-1: Power Supply

Pin name	Pin No.	I/O	Function
AVDD	94, 96, 97, 102, 109, 114, 115, 117	-	+3.3-volt power input for analog section
DVDD	1, 20, 30, 42, 61, 66, 76, 90, 92, 119	-	+3.3-volt power input for digital section
AGND	93, 95, 98, 101, 105, 106, 110, 113, 116, 118	-	Ground input for analog section
DGND	15, 21, 31, 43, 52 ,54 ,60, 67, 75, 91, 120	-	Ground input for digital section

Caution: In PC board layout, connect AGND and DGND to the same, wide plane.
In PC board layout, connect AV_{DD} and DV_{DD} to the same, wide plane.
For details, refer to μPD82821 User's Manual.

1.2 UTP/STP Interface

Table 1-2: UTP/STP Interface

Pin name	Pin No.	I/O	Function
RDIP0	104	I	Receive data input from port #0 (positive) (Balanced analog signal input)
RDIN0	103	I	Receive data input from port #0 (negative) (Balanced analog signal input)
TDOP0	100	O	Transmit data output to port #0 (positive) (Balanced analog signal output)
TDON0	99	O	Transmit data output to port #0 (negative) (Balanced analog signal output)
RDIP1	107	I	Receive data input from port #1 (positive) (Balanced analog signal input)
RDIN1	108	I	Receive data input from port #1 (negative) (Balanced analog signal input)
TDOP1	111	O	Transmit data output to port #1 (positive) (Balanced analog signal output)
TDON1	112	O	Transmit data output to port #1 (negative) (Balanced analog signal output)

1.3 UTOPIA Interface

Table 1-3: UTOPIA Interface

Pin name	Pin No.	I/O	Function
RXDATA0 RXDATA7	29, 28, 27, 26, 25, 24, 23, 22	O (3-state output)	These pins represent an 8-bit data bus that outputs the receive data to an ATM layer device. The data is output at the rising edge of RXCLK.
RXCLK	32	I	This pin supplies the clock signal for the receive data which is output to an ATM layer device.
RXSOC	33	O (3-state output)	This output indicates to the ATM layer device the position of the first byte of a receive cell. RXSOC is set to 1 along with the first data byte of a cell on the RXDATA0-7 bus.
RXENB_B	34	I	This pin inputs an enable signal for RXDATA0-RXDATA7 and RXSOC. When the signal is set to 0, the outputs from RXDATA0-RXDATA7 and RXSOC are enabled.
RXADDR0 - RXADDR4	39, 38, 37, 36, 35	I	These input pins carry the address of PD82821 s PHY RX-Port which status is being polling.
RXCLAV0- RXCLAV1	41, 40	O (3-state output)	These pins output receive cell available signals. When PD82821 has a complete cell for output, it asserts RXCLAV0/1 high to indicate that RX cells in the corresponding port0 or port1 are available for transfer to ATM layer device.
TXDATA0 - TXDATA7	51, 50, 49, 48, 47, 46, 45, 44	I	These pins represent an 8-bit data bus that inputs the transmit data from an ATM layer device. The data is input at the rising edge of TXCLK.
TXCLK	53	I	This pin supplies clock signals for the transmit data from an ATM layer device.
TXSOC	55	I	This input indicates the position of the first byte of a transmit cell, which is input from an ATM layer device. TXSOC is set to 1 along with the first data byte of a cell on the TXDATA0-7 bus.
TXENB_B	56	I	This pin inputs a transmission enable signal. The signal indicates whether an ATM layer device outputs valid transmit data to TXDATA0 to TXDATA7. When valid data is output, the signal is set to 0. Otherwise, the signal is set to 1.
TXADDR0 - TXADDR4	63, 62, 59, 58, 57	I	These input pins carry the address of PD82821 s PHY TX-Port which status is being polling.
TXCLAV0- TXCLAV1	65, 64	O (3-state output)	These pins output transmit cell available signals. When PD82821 can accept a complete transmit cell, it asserts TXCLAV0/1 high to indicate that TX cells can be transfer to it s corresponding port0 or port1 by an ATM layer device.

1.4 CPU Interface

Table 1-4: CPU Interface

Pin name	Pin No.	I/O	Function
BUSMODE	89	I	This pin selects the operating mode of the CPU interface. 0: <DS_B, RW_B, DTACK_B> style (Motorola compatible) 1: <RD_B, WR_B, RDY_B> style (Intel compatible)
DATA0 - DATA7	77, 74, 73, 72, 71, 70, 69, 68	I/O	These pins transfer data (8 bits) between the CPU and internal registers. DATA7 corresponds to the most significant bit.
ADDR0-ADDR5	83, 82, 81, 80, 79, 78	I	These pins set the address (6 bits) of an internal register.
SEL_B	84	I	This pin enables or disables register accesses. When set to 0, access is enabled.
DS_B/WR_B	86	I	• When BUSMODE is set to 0, the input of this pin functions as a data strobe (DS_B) signal of the Motorola compatible interface. In a read cycle: DS_B, when set to 0, enables read data. In a write cycle: DS_B, when set to 0, functions as a write data strobe signal. • When BUSMODE is set to 1, the input of this pin functions as a write instruction of the Intel-compatible interface. WR_B, when set to 0, functions as a write instruction.
RW_B/RD_B	85	I	• When BUSMODE is set to 0, the input of this pin functions as a read/write control (RW_B) signal of the Motorola compatible Interface. 0: Write cycle 1: Read cycle • When BUSMODE is set to 1, the input of this pin functions as a read instruction of the Intel-compatible interface (RD_B).
DTACK_B /RDY_B	87	O (3-state output)	• When BUSMODE is set to 0, the output of this pin functions as an acknowledge signal (DTACK_B) of the Motorola compatible interface. The signal indicates whether data transmission on the data bus has been completed. If so, DTACK_B is driven to 0. • When BUSMODE is set to 1, the output of this pin functions as a ready signal (RDY_B) of the Intel compatible interface. The signal indicates whether data transmission on the data bus has been completed. If so, RDY_B is driven to 0.
INT_B	88	O	The output of this pin informs the CPU that an interrupt source has been detected.

1.5 Other Pins

Table 1-5: Other Pins

Pin name	Pin No.	I/O	Function
JDI	10	I	This pin functions as a JTAG test data input.
JDO	11	O	This pin functions as a JTAG test data output.
JCK	12	I	This pin functions as a clock input for the JTAG test.
JMS	13	I	This pin functions as a JTAG test mode input.
JRST_B	14	I	This pin inputs the JTAG test reset signal.
SIN	18	I (with pull-down resistor)	This pin functions as the X_8 command transmission timing input.
SOUT	19	O	This pin functions as the X_8 command reception timing output.
TCLOCK	16	I	This pin supplies a transmit clock (32 MHz).
RESET_B	17	I	This pin inputs the signal to reset the entire chip.
IC	2, 3, 4, 5, 6, 7, 8, 9	-	Internally connected, please leave open.

1.6 Handling Unused Pins

Table 1-6: Handling Unused Pins

Pin Name	Input/Output	Recommended connection for unused pins
RDIP0-RDIP1	Input	pull-up through 1kΩ the resistor
RDIN0-RDIN1	Input	pull-down through 1kΩ the resistor
TDOP0-TDOP1	Output	open
TDON0-TDON1	Output	open
JDI	Input	pull-up through resistor
JDO	Output	open
JCK	Input	pull-up through resistor
JMS	Input	pull-up through resistor
JRST_B	Input	pull-down through resistor
SIN	Input (with pull-down resistor)	open
SOUT	Output	open

1.7 Pin Conditions at Reset

Table 1-7: Pin Conditions at Reset

Pin Name	Input/Output	Pin conditions while reset
TDOP0-TDOP1	Output	Unknown
TDON0-TDON1	Output	Unknown
RXDATA0-RXDATA7	Output (3-state)	Hi-Z
RXSOC	Output (3-state)	Hi-Z
RXCLAV0- RXCLAV1	Output (3-state)	Hi-Z
TXCLAV0- TXCLAV1	Output (3-state)	Hi-z
DATA0-DATA7	Input/Output	Hi-Z
DTACK_B/RDY_B	Output	High-Z
INT_B	Output	High
JDO	Output	Unknown
SOUT	Output	Low

1.8 CPU Interface

1.8.1 Write Operation (Intel Mode, BUSMODE = 1)

a) *States of Write operation access:*
M(aster) = CPU or ATM SAR Device
S(lave) = μPD82821 or μPD82387

b) *Write operation in detail:*
1. M applies valid ADDR0-5
2. M selects Slave by SEL_B = '0'
3. M indicates write operation with WR_B = '0' while RD_B = '1'
4. S processes write operation; indicates 'Ready for Write' by asserting RDY_B = '0'
5. If RDY_B = '0' M finishes write operation by driving the valid DATA0-7 and de-assertion of WR_B (data is written with the rising edge of WR_B)

Note: The handshake signal RDY_B needs NOT to be used. If it is NOT used, the Master can de-assert the WR_B signal after a specified minimal time (check values with * in the table bellow), instead of waiting for RDY_B.
BUT this decreases the CPU interface access time up to 300% (compared to the case in which RDY_B is used for handshaking)!

(1) Write operation (when BUSMODE = 1)

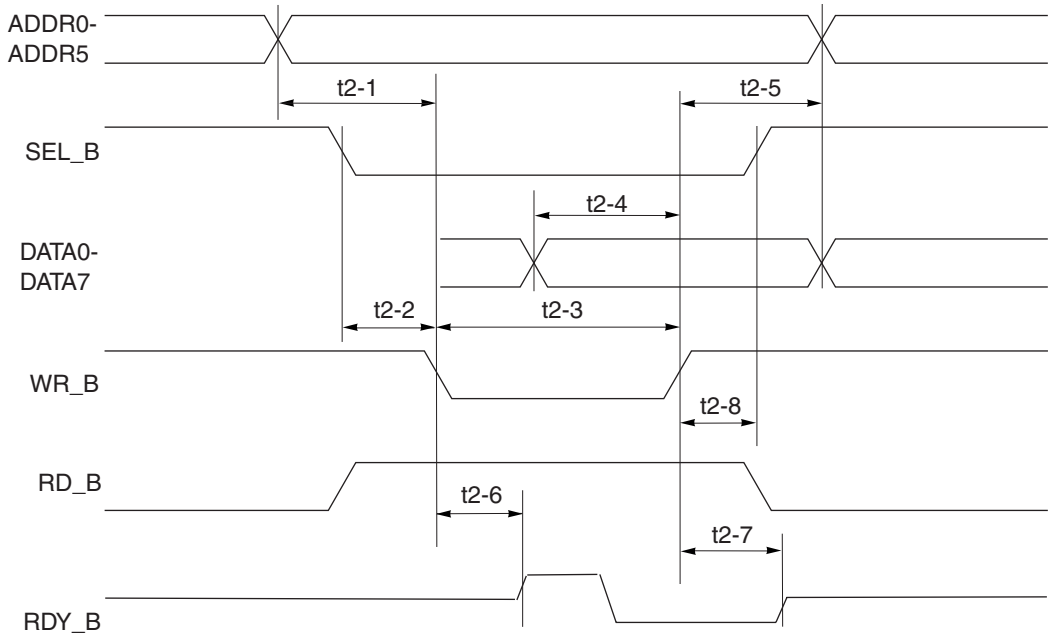
Table 1-8: Write operation (when BUSMODE = 1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to WR_B↓)	t2-1		7	–	–	ns
SEL_B setup time (referred to WR_B↓)	t2-2		5	–	–	ns
WR_B pulse width	t2-3		120*	–	–	ns
DATA setup time (referred to WR_B↑)	t2-4		7	–	–	ns
ADDR/DATA hold time (referred to WR_B↑)	t2-5		0	–	–	ns
RDY_B valid time (referred to WR_B↓)	t2-6		–	–	10	ns
RDY_B invalid/tri-state time (referred to WR_B↑)	t2-7		–	–	10	ns
SEL_B hold time (referred to WR_B↑)	t2-8		0	–	–	ns

* Only if the handshake signal RDY_B is NOT used. See "States of Write operation" for more information.

CPU Interface Write Operation (BUSMODE = 1)

Figure 1-1: CPU Interface Write Operation (BUSMODE = 1)



1.8.2 Read Operation (Intel Mode, BUSMODE = 1)

a) *States of Read operation access:*
M(aster) = CPU or ATM SAR Device
S(lave) = µPD82821 or µPD82387

b) *Read operation in detail:*
1. M applies valid ADDR0-5
2. M selects Slave by SEL_B = '0'
3. M indicates read operation with WR_B = '1' while RD_B = '0'
4. S processes read operation and indicates 'Ready for Read' by RDY_B = '0' when it drives the valid DATA0-7 on the bus.
5. If RDY_B = '0' M finishes read operation by fetching the valid DATA0-7 and de-assertion of RD_B (data is read with the rising edge of RD_B).

(2) Read operation (when BUSMODE = 1)

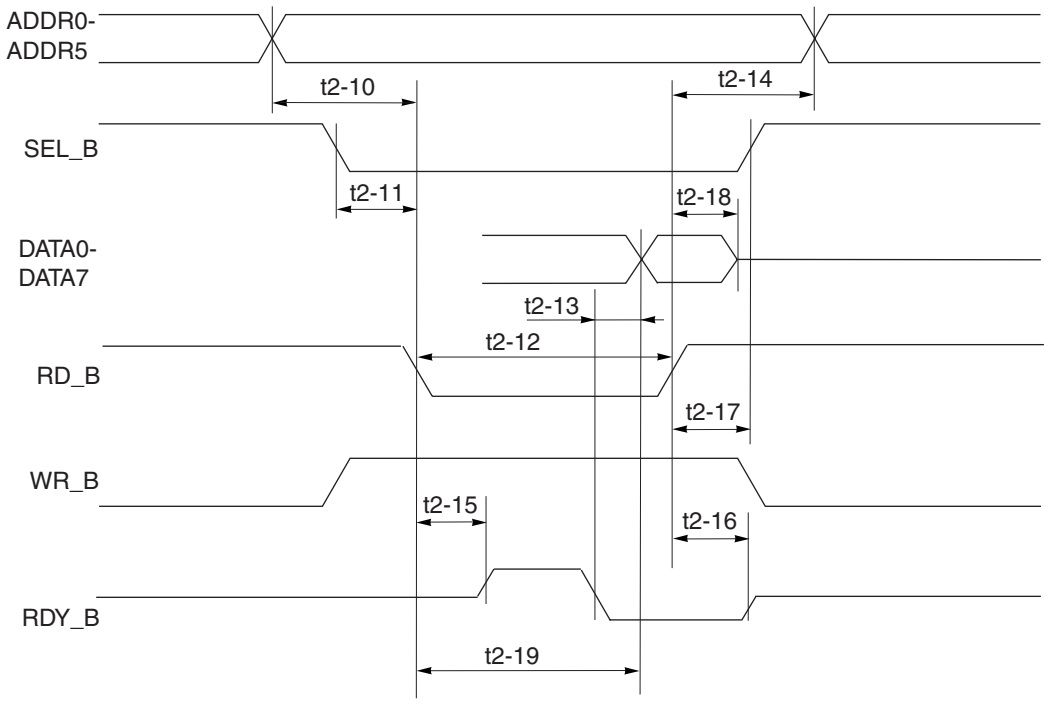
Table 1-9: Read operation (when BUSMODE = 1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to RD_B↓)	t2-10		7	–	–	ns
SEL_B setup time (referred to RD_B↓)	t2-11		5	–	–	ns
RD_B pulse width	t2-12		120*	–	–	ns
DATA fixed time (referred to RDY_B↓)	t2-13		–	–	8	ns
ADDR hold time (referred to RD_B↑)	t2-14		0	–	–	ns
RDY_B valid time (referred to RD_B↓)	t2-15		–	–	10	ns
RD_B de-assert to RDY_B tri-state (referred to RD_B↑)	t2-16		–	–	10	ns
SEL_B hold time (referred to RD_B)	t2-17		0	–	–	Ns
RD_B de-assert to Data tri-state (referred to RD_B↑)	t2-18		–	–	10	ns
RD_B assert to Data valid (referred to RD_B↓)	t2-19		–	–	96*	ns

* Only if the handshake signal RDY_B is NOT used. See “States of Read operation” for more information.

CPU Interface Read Operation (BUSMODE = 1)

Figure 1-2: CPU Interface Read Operation (BUSMODE = 1)



1.8.3 Write Operation (Motorola Mode, BUSMODE = 0)

a) *States of Write operation access:*
M(aster) = CPU or ATM SAR
S(lave) = µPD82821 or µPD82387

b) *Write operation in detail:*
1. M applies valid ADDR0-5
2. M selects Slave by SEL_B = '0'
3. M indicates write operation with RW_B = '0'
4. S processes write operation; indicates 'Ready for Write' by asserting DTACK_B = '0'
5. If DTACK_B = '0' M finishes write operation by driving the valid DATA0-7 and de-assertion of RW_B (data is written with the rising edge of RW_B)

Note: The handshake signal DTACK_B needs NOT to be used. If it is NOT used, the Master can de-assert the WR_B signal after a specified minimal time (check values with * in the table bellow), instead of waiting for DTACK_B.
BUT this decreases the CPU interface access time up to 300% (compared to the case in which DTACK_B is used for handshaking)!

(3) Write operation (when BUSMODE = 0)

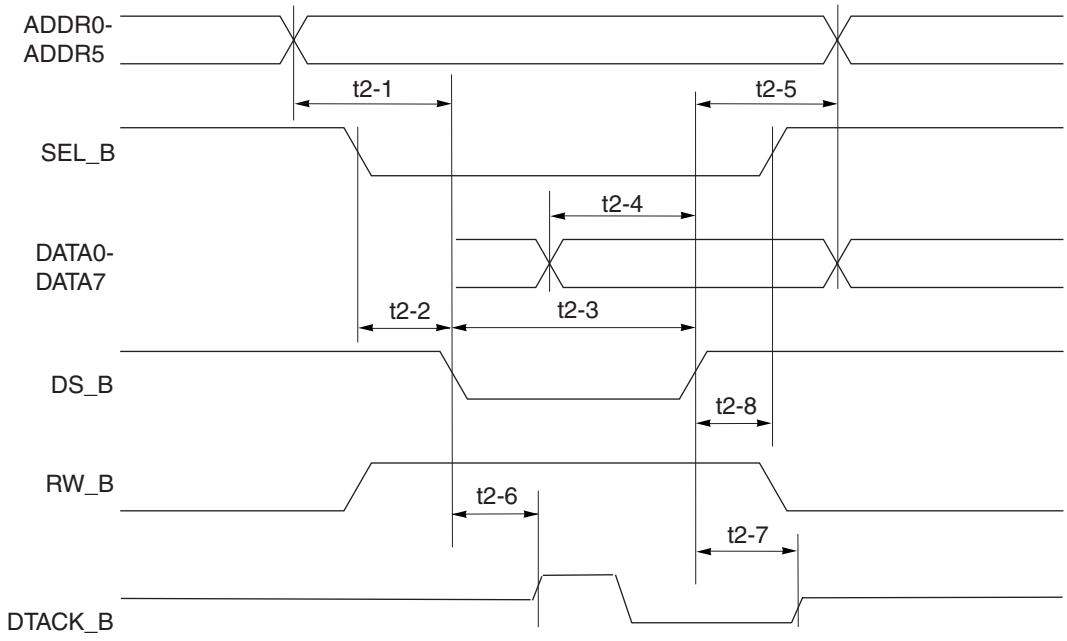
Table 1-10: Write operation (when BUSMODE = 0)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to DS_B↓)	t2-1		7	–	–	ns
SEL_B or RW_B setup time (referred to DS_B↓)	t2-2		5	–	–	ns
DS_B pulse width	t2-3		120*	–	–	ns
DATA setup time (referred to DS_B↑)	t2-4		7	–	–	ns
ADDR/DATA hold time (referred to DS_B↑)	t2-5		0	–	–	ns
DTACK_B valid time (referred to DS_B↓)	t2-6		–	–	8	ns
DTACK_B invalid/tri-state time (referred to DS_B↑)	t2-7		–	–	10	ns
SEL_B or RW_B hold time (referred to DS_B↑)	t2-8		0	–	–	ns

* CPU Interface Write Operation (BUSMODE = 0)

CPU Interface Write Operation (BUSMODE = 0)

Figure 1-3: CPU Interface Write Operation (BUSMODE = 0)



1.8.4 Read Operation (Motorola Mode, BUSMODE = 0)

a) *States of Read operation access:*
M(aster) = CPU or ATM SAR Device
S(lave) = µPD82821 or µPD82387

b) *Read operation in detail:*
1. M applies valid ADDR0-5
2. M selects Slave by SEL_B = '0'
3. M indicates read operation with RW_B = '1'
4. S processes read operation; indicates 'Ready for Read' by asserting DTACK_B = '0' when it drives the valid DATA0-7 on the bus.
5. If RDY_B = '0' M finishes read operation by fetching the valid DATA0-7 and de-assertion of RW_B (data is read with the rising edge of RW_B)

(4) Read operation (when BUSMODE = 0)

Table 1-11: Read operation (when BUSMODE = 0)

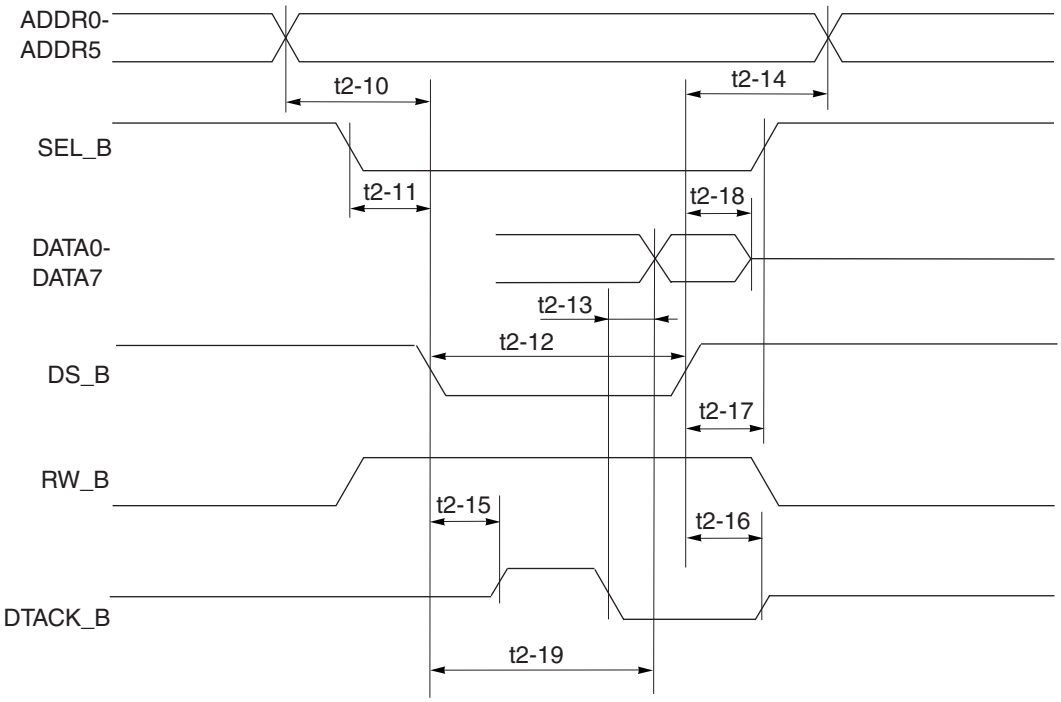
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to DS_B↓)	t2-10		7	–	–	ns
SEL_B or RW_B setup time (referred to DS_B↓)	t2-11		5	–	–	ns
DS_B pulse width	t2-12		120*	–	–	ns
DATA fixed time (referred to DTACK_B↓)	t2-13		–	–	8	ns
ADDR hold time (referred to DS_B↑)	t2-14		0	–	–	ns
DTACK_B valid time (referred to DS_B↓)	t2-15		–	–	10	ns
DS_B deassert to DTACK_B tri-state (referred to DS_B↑)	t2-16		–	–	10	ns
SEL_B or RW_B hold time (referred to DS_B↑)	t2-17		0	–	–	ns
DS_B deassert to DATA tri-state (referred to DS_B↑)	t2-18		–	–	10	ns
DS_B assert to DATA valid (referred to DS_B↓)	t2-19		–	–	96*	ns

* CPU Interface Read Operation (BUSMODE = 0)

Note: The handshake signal DTACK_B needs NOT to be used. If it is NOT used, the Master can de-assert the RW_B signal after a specified minimal time (check values with * in the table bellow), instead of waiting for DTACK_B.
BUT this decreases the CPU interface access time up to 300% (compared to the case in which DTACK_B is used for handshaking)!

CPU Interface Read Operation (BUSMODE = 0)

Figure 1-4: CPU Interface Read Operation (BUSMODE = 0)



1.9 UTOPIA Interface

(1) Transmission

Table 1-12: Transmission

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TxCLK frequency	t3-1		0	–	40	MHz
TxCLK duty cycle	t3-2		40	–	60	%
TxCLK jitter (peak to peak)	t3-3		–	–	5	%
TxCLK rise time	t3-4	Measurement of 10 to 90 % transition time	–	–	3	ns
TxCLK fall time	t3-5	Measurement of 10 to 90 % transition time	–	–	3	ns
TxDATA[7:0], TxSOC, TxENB_B, or TxADDR[4:0] setup time	t3-6		8	–	–	ns
TxDATA[7:0], TxSOC, TxENB_B, or TxADDR[4:0] hold time	t3-7		1	–	–	ns
TxCLAV[1..0] setup time (referred to TxCLK↑)	t3-8		10	–	–	ns
TxCLAV hold time (referred to TxCLK↑)	t3-11		2	–	–	ns
TxCLAV high-impedance setup time (referred to TxCLK↑)	t3-9		10	–	–	ns
TxCLAV low-impedance delay time (referred to TxCLK↑)	t3-10		2	–	–	ns

(2) Reception

Table 1-13: Reception

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RxCLK frequency	t3-12		0	–	40	MHz
RxCLK duty cycle	t3-13		40	–	60	%
RxCLK jitter (peak to peak)	t3-14		–	–	5	%
RxCLK rise time	t3-15	Measurement of 10 to 90 % transition time	–	–	3	ns
RxCLK fall time	t3-16	Measurement of 10 to 90 % transition time	–	–	3	ns
RxENB_B or RxADDR[4:0] Setup time	t3-17		8	–	–	ns
RxENB_B or RxADDR[4:0] Hold time	t3-18		1	–	–	ns
RxDATA[7:0], RxSOC or RxCLAV[1..0] setup time (referred to RxCLK↑)	t3-19		10	–	–	ns
RxDATA[7:0], RxSOC or RxCLAV[1..0] hold time (referred to RxCLK↑)	t3-22		2	–	–	ns
RxDATA[7:0], RxSOC or RxCLAV0[1..0] high-impedance setup time (referred to RxCLK↑)	t3-20		10	–	–	ns
RxDATA[7:0], RxSOC or RxCLAV[1..0] high-impedance hold time (referred to RxCLK↑)	t3-21		2	–	–	ns

Figure 1-5: TxCLK or RxCLK Timing - 1

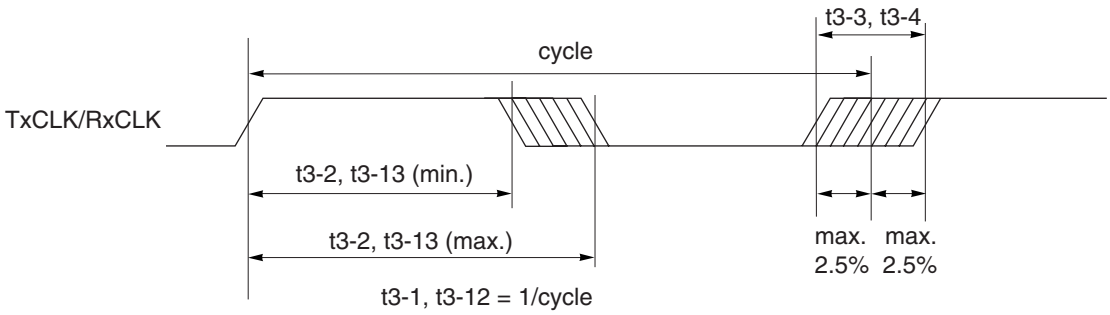


Figure 1-6: TxCLK or RxCLK Timing - 2

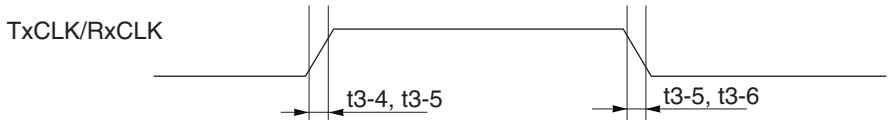


Figure 1-7: Input Signal Setup Timing

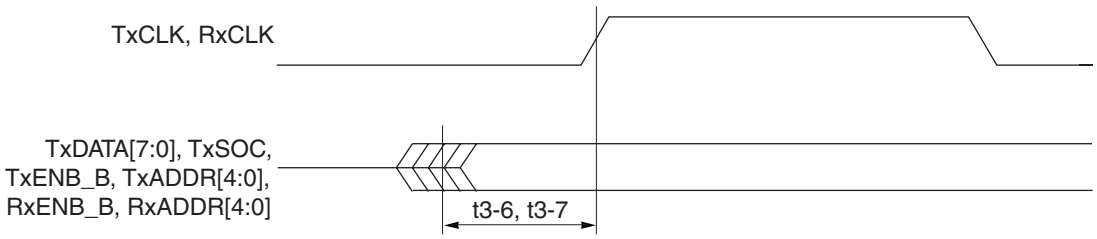


Figure 1-8: Input Signal Hold Timing

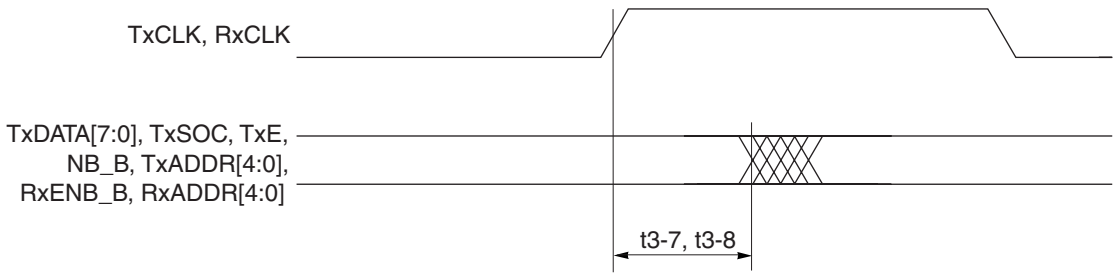


Figure 1-9: Output Delay Time - 1

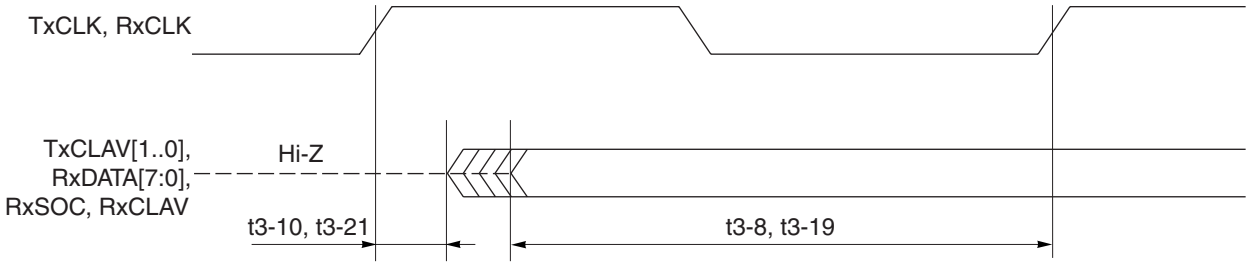
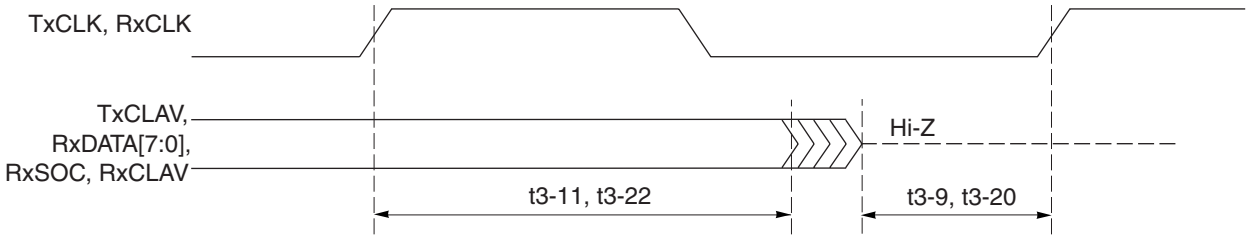


Figure 1-10: Output Delay Time - 2



1.10 Others

Table 1-14: Others

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIN pulse width	t5-1		11	–	–	TCLOCK clock
SOUT pulse width	t5-2		–	15	–	TCLOCK clock
RESET_B pulse width	t5-3		50	–	–	ns

Figure 1-11: SIN and SOUT Timings

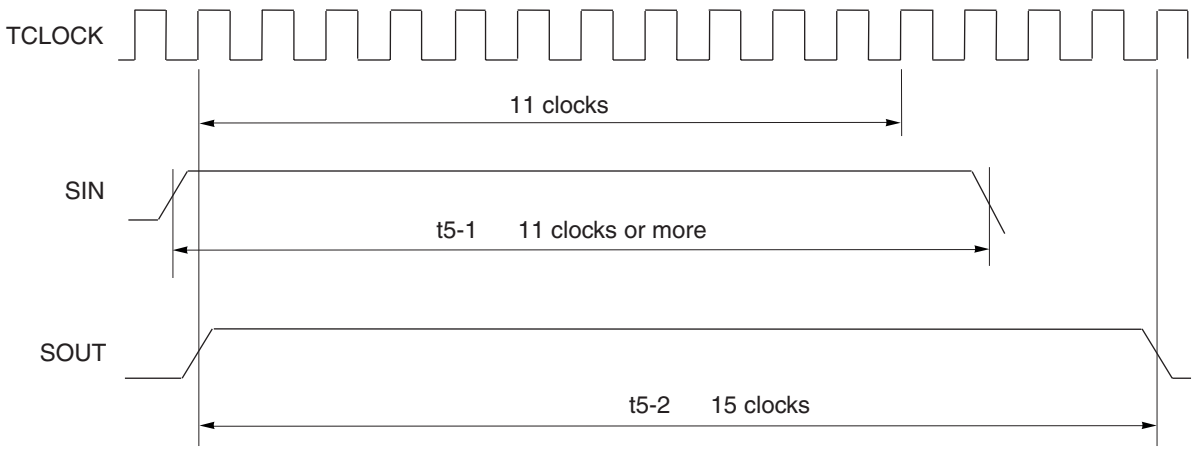
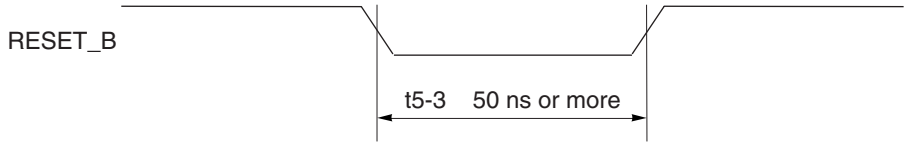


Figure 1-12: RESET_B Timing



2. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}		-0.5 to +4.6	V
Input voltage	V_I		-0.5 to +6.6	V
Output voltage	V_O		-0.5 to +6.6	V
Output current	I_{O1}	**Note 1**	10	mA
	I_{O2}	**Note 2**	30	mA
Storage temperature	T_{STG}		-65 to +150	°C

Caution: Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Notes: 1. Applies to pins JDO and SOUT.
2. Applies to pins RxDATA0-RxDATA7, RxSOC, RxCLAV0-RxCLAV1, TxCLAV0-TxCLAV1, INT_B, DTACK_B/RDY_B, and DATA0-DATA7.

Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}		3.135	3.3	3.465	V
High-level input voltage	V_{IH}		2.0	–	5.5	V
Low-level input voltage	V_{IL}		0	–	0.8	V
Operating ambient temperature	T_A		-40	–	+85	°C

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 3.3 V ± 5 %)

Table 2-3: DC Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}	V_I = V_{DD} or GND	–	–	2	μA
High-level output current	$I_{OH}1$	V_{OH} = 2.4 V Note 1	-3.0	–	–	mA
	$I_{OH}2$	V_{OH} = 2.4 V Note 2	-8.0	–	–	mA
Low-level output current	$I_{OL}1$	V_{OL} = 0.4 V Note 1	3.0	–	–	mA
	$I_{OL}2$	V_{OL} = 0.4 V Note 2	9.0	–	–	mA
High-level output voltage	V_{OH}	I_{OH} = 0 mA	V_{DD} - 0.2	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = 0 mA	–	–	0.1	V
Supply current	I_{DD}	In operation	–	105	280	mA

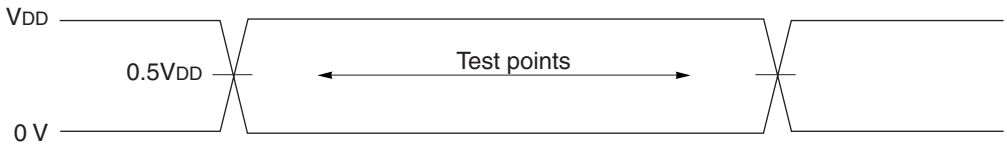
Notes: **1**. Applies to pins JDO and SOUT.
2. Applies to pins RxDATA0-RxDATA7, RxSOC, RxCLAV0-RxCLAV1, TxCLAV0-TxCLAV1, INT_B, DTACK_B/RDY_B, and DATA0-DATA7.

Capacitance

Table 2-4: Capacitance

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	Frequency = 1 MHz	–	10	20	pF
Output capacitance	C_O	Frequency = 1 MHz	–	10	20	pF
I/O capacitance	C_{IO}	Frequency = 1 MHz	–	10	20	pF

Figure 2-1: AC Test I/O Waveform



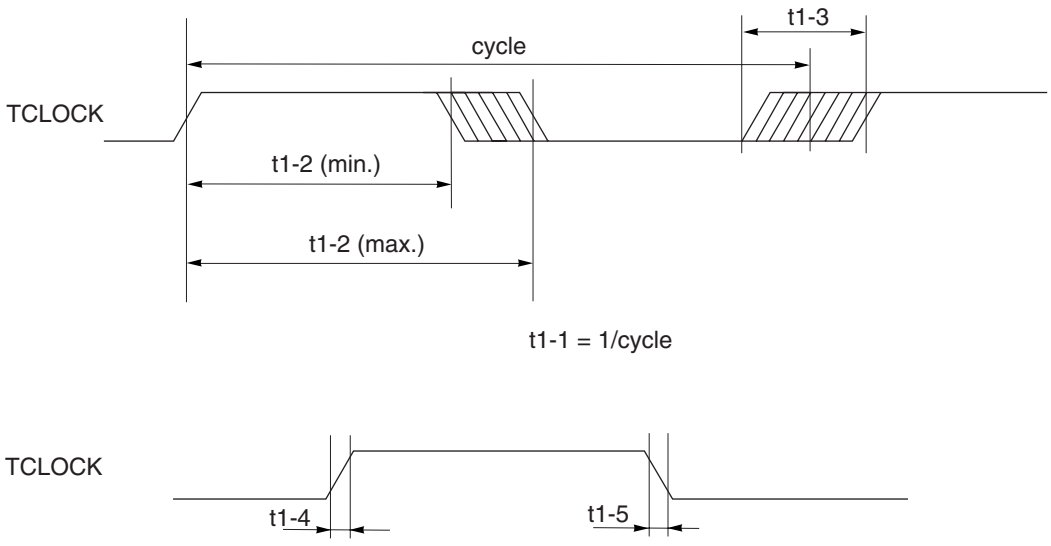
AC Characteristics (T_A = -40 to +85 °C, V_{DD} = 3.3 V ± 5 %)

TCLOCK

Table 2-5: TCLOCK

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCLOCK frequency	t1-1		–	32	–	MHz
TCLOCK duty	t1-2		40	–	60	%
TCLOCK frequency accuracy	t1-3		–	–	100	ppm
TCLOCK rise time	t1-4	Measurement of 10 to 90 % transition time	–	–	5	ns
TCLOCK fall time	t1-5	Measurement of 10 to 90 % transition time	–	–	5	ns

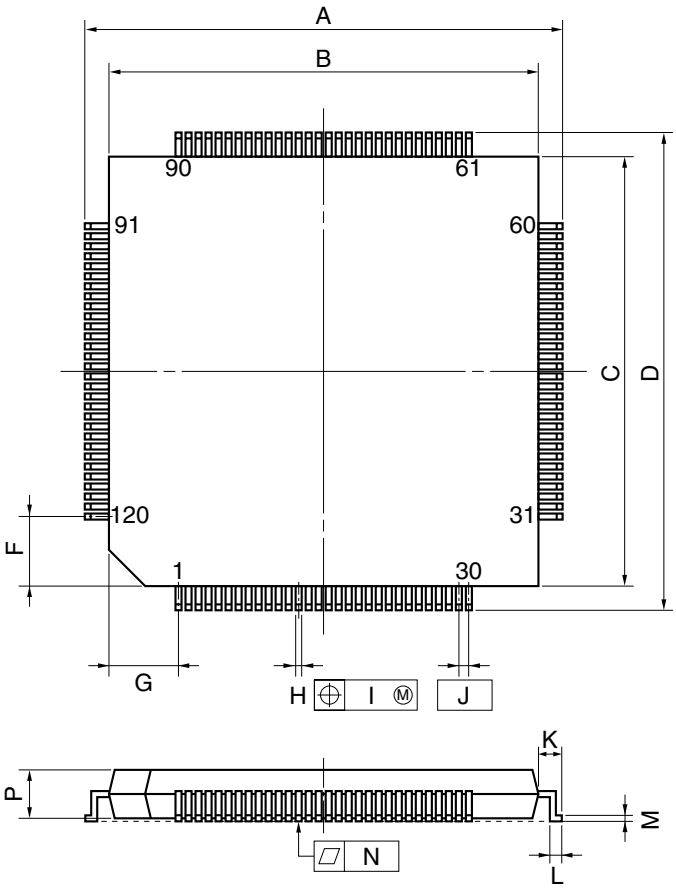
Figure 2-2: TCLOCK Input

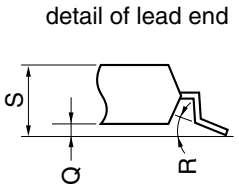


3. PACKAGE DRAWING

Figure 3-1: Package Drawing

120 PIN PLASTIC QFP (FINE PITCH) (□20)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	22.0±0.2	0.866±0.008
F	2.75	0.108
G	2.75	0.108
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5 ±5	5 ±5
S	3.0 MAX.	0.119 MAX.

S120GJ-50-3EB-2

4. RECOMMENDED SOLDERING CONDITIONS

To be defined

Notes for CMOS Devices

① Precaution against ESD for Semiconductors

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② Handling of unused input pins for CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ Status before initialization of MOS devices

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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