

Type	Ordering code	Package
SDA 5640	Q67100-H8087	DIP 14

Description of function

In conjunction with a video processor (data slicer), the SDA 5640 as data line decoder, receives and decodes additional information for the video program system (VPS) in data line 16 of the TV signal (see diagram 1, 2). Subsequently, the information is forwarded for further processing via the I²C bus interface.

Since each program is identified by an encoded label during transmission, the data line decoder provides for the recording and controlling of a specific program on the video recorder. As a result, erroneous recordings caused by program changes or postponements are prevented.

Description of applications

The application circuit 1 shows a complete data line recorder comprising a VPS decoder and a data slicer.

Circuit description

Essentially, the data line decoder consists of three function blocks, namely, a timing, a data acquisition and a data output block.

Timing block

This unit recognizes line 16 from the VCS signal (see diagram 3) and enables the data acquisition block for this time period. By means of counters, the pulse widths of the VCS signal are measured and the vertical sync signals are subsequently derived from these measurements. The location of the first line pulse after the frame sync roll pulses (including the post-equalizing pulse), defines the first or second half-frame. In the case of the first half-frame, a counter counts up to the 16th line pulse and enables the data acquisition block until the 17th line pulse.

Data acquisition block

While the timing block indicates line 16, the biphasic data signal arriving on the DZDA line is searched for the start bit (see diagram 4). This bit is used to synchronize the decoding circuitry and is the only bit that does not comply with the biphasic code format (Manchester code format). As a prerequisite for transferring the data into the output register, the start code must be recognized in the six bits following the start bit.

From a total of 15 words with 8 bits each, only words 5 and 11 to 14 are relevant to the evaluation process in the video recorder. Therefore, only these 40 bits are transferred into the shift register. During the entire data telegram the biphasic antivalence rule is checked. At the end of word 14, the relevant 5 words are transferred into the transmit register bank if the start code is identified, no biphasic violations are detected, and the IC is not simultaneously addressed via the I²C bus interface.

After reading out the VPS data, the transmit registers are cleared (all bits logic "1") and reloaded after line 16 is received without errors. As data line 16 is transmitted once within a full frame, the intervals between reads should be greater than 40 ms.

Data output

Data output is performed via an I²C bus interface (slave transmitter). The time relationship between the SDA and the SCL signal lines during the read-out phase is shown in diagrams 5 and 6.

The data transfer format is:

START	Chip address f. master	AS	Word 11 f. slave	AM	Word 14 f. slave	AM	Word 5 f. slave	NAM	STOP
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The information contents of words 11...14 and word 5 are shown in the data sheet on page 312.

Sequence

1. The processor (master) prompts a start condition (SDA changes from High to Low, while SCL = High). Subsequently the master clocks the SCL line for the duration of the protocol.
The word address counter is reset and points to word 11.
2. Synchronous to the first 8 SCL clocks, the master forwards an 8 bit chip address onto the SDA line (VPS decoder must be hardware programmed for this address).
3. During the ninth clock phase, the master enables the SDA line (SDA changes to high, due to an external pull-up resistor) and the decoder (slave) generates an acknowledge (returns SDA line to low; AS).
4. During the next 8 SCL clocks the slave forwards the address word to the SDA line.
5. Intermediate clock for master acknowledge (AM), causes the slave transmitter to increment its word address counter.
6. Repetition of steps 4 and 5, until all data values are output. However, the master does not acknowledge the fifth data word, indicating to the slave the end of transmission (no acknowledge; NAM).
7. The master ends the protocol with the stop condition during the last SCL clock period (low-high change of SDA while SCL = high).

Description of additional decoder functions

1. Without special measures, the color burst would be available as a data signal on the DZDA line in addition to the VPS data. In order to prevent the VPS decoder from synchronizing to the color burst, the decoder supplies the data slicer with a color burst blanking signal (SAND) to reset the data separation circuitry and the clock phase detector in the video processor (see diagram 7). The data output of the data slicer as well as the DZDA input of the VPS decoder are forced to low for the duration of the SAND pulse, so that the coupling capacitor is precharged to low during the SAND pulse phases. The decoder generates the SAND pulse for each TV line, it is however synchronized with the VCS signal only once per full frame.
2. The DAVN signal indicates whether VPS data is being received by the SDA 5640. When a data line is present, pulses with the vertical frame frequency appear at the DAVN output (see diagram 3). The output is set each time at the beginning of line 16 and reset with the data transfer pulse (internal signal at the end of word 14 within line 16). When the transfer pulse is not generated due to missing data line information, the signal line DAVN will remain high. In addition the DAVN signal is set to high when the chip is addressed via the I²C bus. This corrects an accidental low level on DAVN due to a missing CVBS (composite video blanking signal).
3. By means of the test pin (TI = high) the DAVN output can be switched to serve as a test signal output. The internal signal Z16N (when CS0 = low) or ADIX (when CS0 = high) is connected to the DAVN output.
4. A data query via the I²C bus is started by the master by transmitting the chip address, which must be identical with the hardware address of the VPS decoder. Two different chip addresses can be selected through input CS0:

CS0	Chip address (hexadecimal)
low	21 H
high	23 H

Maximum ratings

		min	typ	max		Remarks
Supply voltage range	V_{DD}	-0.3		6	V	
Input voltage for DZCL, DZDA	V_{IM2}	-0.3		10.5	V	
Input voltage	V_{IM1}	-0.3		6	V	Exception: DZCL, DZDA (see V_{IM2})
Ambient temperature range	T_A	0		70	°C	
Storage temperature range	T_{stg}	-40		125	°C	
Total power dissipation	P_{tot}			300	mW	
Power dissipation per output	P_Q			10	mW	

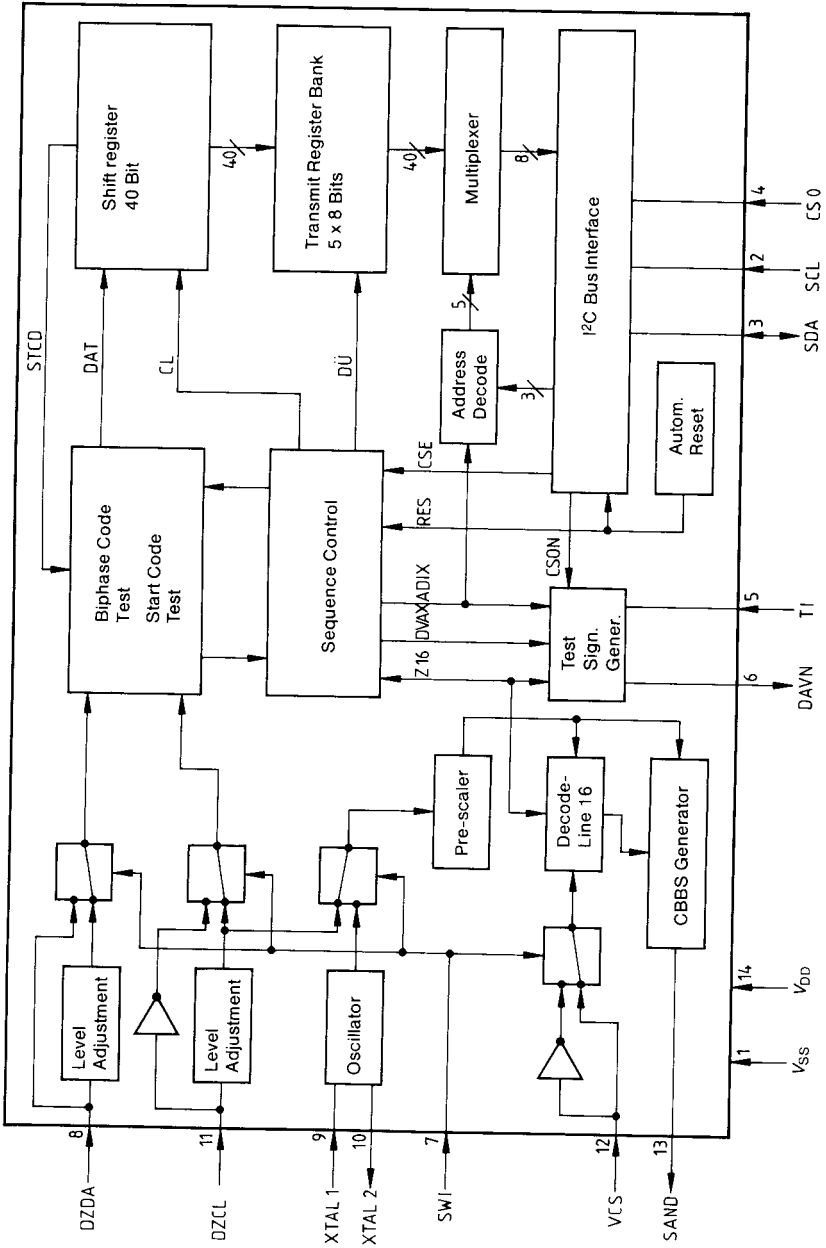
Operating range

Supply voltage	V_{DD}	4.5		5	5.5	V
Supply current	I_{DD}				50	mA
Operating frequency	f_S	4		5	6	MHz
Ambient temperature	T_A	0			70	°C

Characteristics $T_A = 25\text{ }^\circ\text{C}$

			min	typ	max	
Input signals SDA, SCL						
H input voltage		V_{IH}	3.0		V_{DD}	V
L input voltage		V_{IL}	0		0.8	V
Input capacitance		C_I			10	pF
Input current		I_{IM}			10	μA
Input signals VCS, CS0, TI, SWI						
H input voltage		V_{IH}	2.0		V_{DD}	V
L input voltage		V_{IL}	0		0.8	V
Input capacitance		C_I			10	pF
Input current		I_{IM}			10	μA
Input signal DZCL						
H input voltage	SWI > 2 V	V_{IH}	2.0		V_{DD}	V
L input voltage	SWI > 2 V	V_{IL}	0		0.8	V
DC voltage portion	SWI < 0.8 V	$V_{CL/DC}$	4		8	V
Amplitude	SWI < 0.8 V	$V_{CL/SS}$	1		4	V
Input capacitance		C_I			10	pF
Input current		I_{IM}			10	μA
Input signal DZDA						
H input voltage	SWI > 2 V	V_{IH}	2.0		V_{DD}	V
L input voltage	SWI > 2 V	V_{IL}	0		0.8	V
Amplitude	SWI < 0.8 V	$V_{CL/SS}$	2		7	V
Input capacitance		C_I			10	pF
Ext. coupling capacitance	SWI < 0.8 V	C_C		10	50	nF
Input current	SWI > 2 V	I_{IM}			10	μA
Output signals SAND, DAVN						
H output voltage	$I_Q = -100\text{ }\mu\text{A}$	V_{QH}	$V_{DD}-0.5$			V
L output voltage	$I_Q = 1.6\text{ mA}$	V_{QL}			0.4	V
Output signal SDA (open drain stage)						
L output voltage	$I_Q = 3.0\text{ mA}$	V_{QL}			0.4	V
permissible H-output voltage		V_{QH}			5.5	V
Crystal oscillator input XTAL1						
H input voltage		V_{IH}	2.0		V_{DD}	V
L input voltage		V_{IL}	0		0.8	V
With external clock injection at XTAL2						
H input voltage	XTAL1 = 0 V	V_{IH}	2.5		V_{DD}	V
L input voltage	XTAL1 = 0 V	V_{IL}	0		0.8	V
Crystal characteristics						
Resonance resistance		R_r			100	Ω
Load capacitance		C_L		20		pF
Shunt capacitance		C_0			4.5	pF
Max. permissible load					10	mW

Block diagram for data line decoder

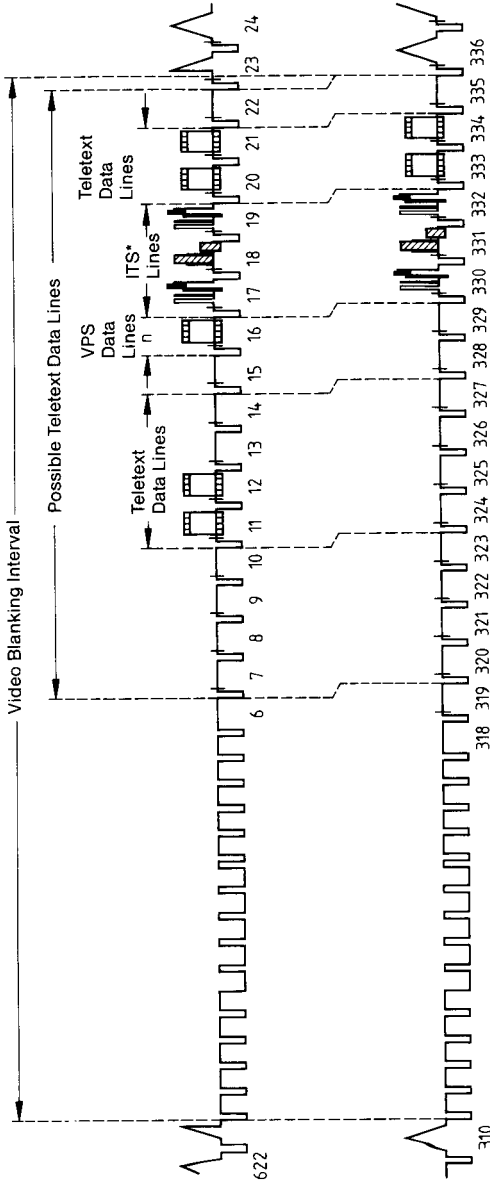


Pin description

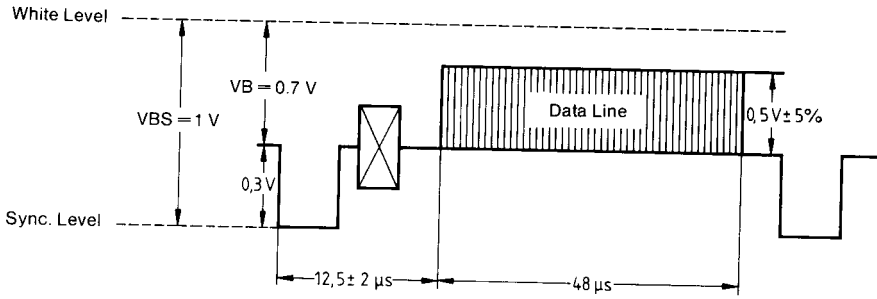
Pin	Symbol	Designation	Function
1	V _{SS}	Ground	Negative voltage supply
2	SCL	I ² C bus clock	Clock line for I ² C bus
3	SDA	I ² C bus data	Data line for I ² C bus
4	CS0	Chip select	To switch the hardware address of the chip from 21H (CS0 = low) to 23H (CS0 = high) with pin CS0
5	TI	Test switch	To switch the DAVN output for use as test signal output with the test pin. As a function of the CS0 pin, the internal signal Z16N (when CS0 = low) or ADIX (when CS0 = high) is connected to the DAVN output for test purposes
6	DAVN	VPS transmitter recognition	The form of the output signal provides information whether the set transmitter is transmitting a VPS data line.
7	SWI	Data slicer sel.	The interface can be adapted to different types of video processors via the SWI pin
8	DZDA	Biphase data	VPS bi-phase data arrival at the DZDA pin (transmission rate 2.5 Mbit/s)
9	XTAL1	Osc. input	Crystal oscillator input
10	XTAL2	Osc. output	Oscillator output for system clock generation, in case data clock DZCL cannot be used as system clock
11	DZCL	Reg. data clock	Regenerated biphase data clock
12	VCS	Sync. signal	Data slicer derives the synchronous signal from the composite video blanking signal
13	SAND	CBBS	Blanking signal forwarded from VPS decoder to data slicer to separate color burst from biphase data (is used at the same time as control for an active clamping circuitry in the VPS decoder)
14	V _{DD}	Supply voltage	Positive voltage supply

Diagram 1

CVBS signal with position of VPS data line



* Insertion Test Signal

Diagram 2**Insertion of data line into CVBS signal**

Degree of Modulation = 71.4%

Diagram 3

VCS - DAVN

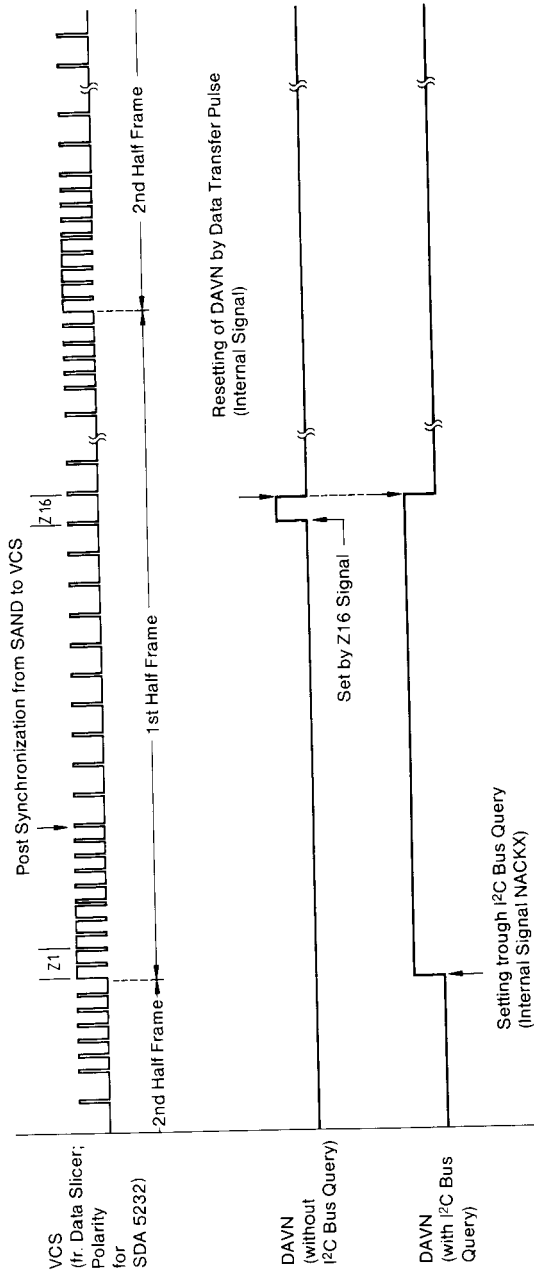


Diagram 4
 DZCL, DZDA

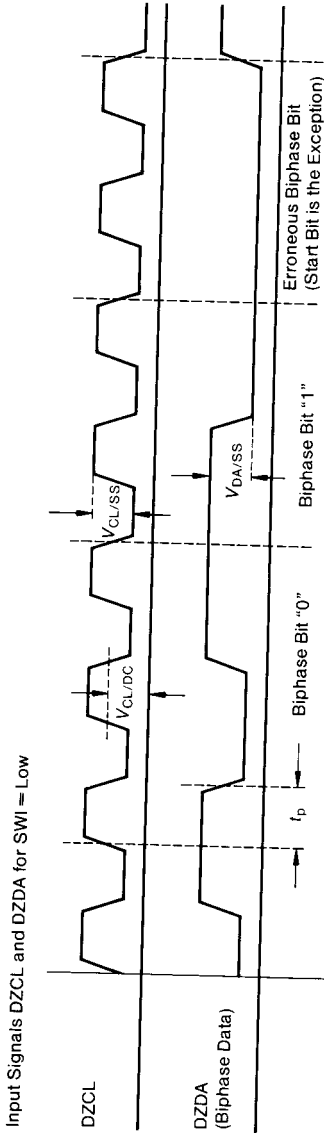
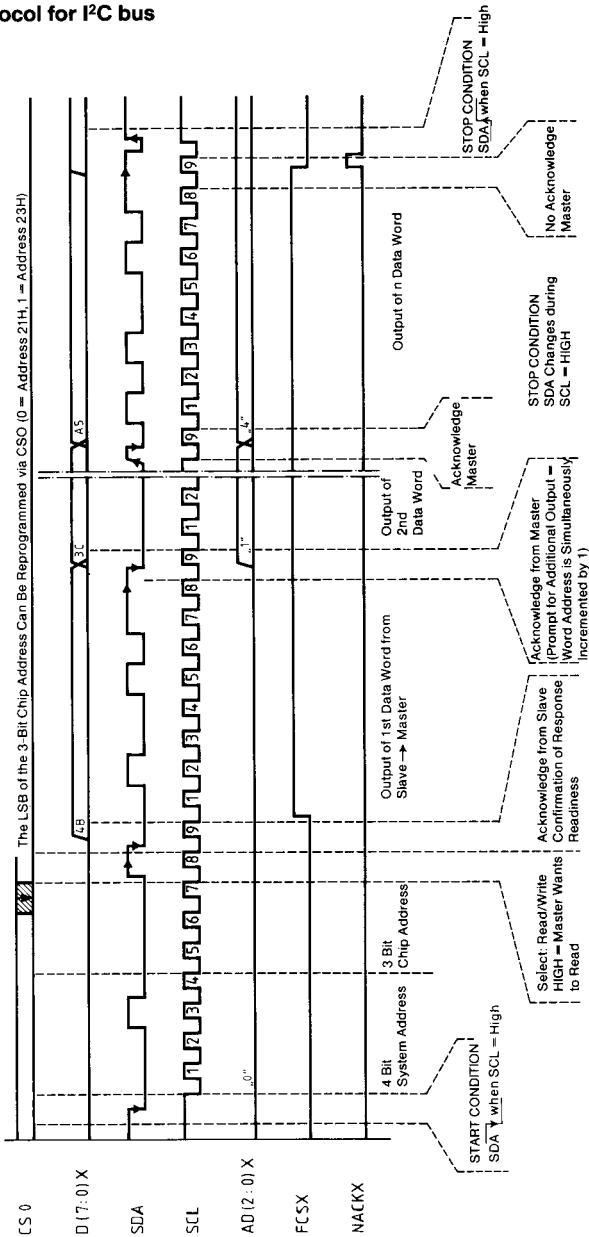


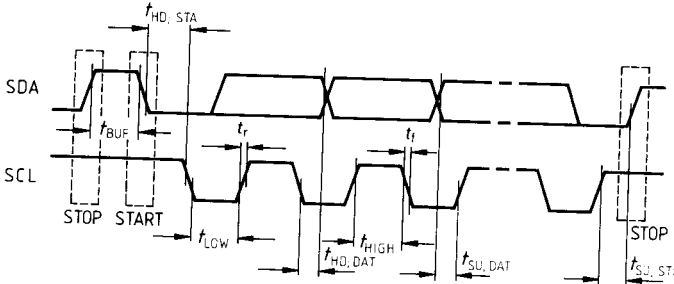
Diagram 5

Transfer protocol for I²C bus



Signals with Additional X Identification are Circuit-Internal Signals

Diagram 6
I²C bus timing



		min	max	
Clock frequency	f_{SCL}	0	100	kHz
Inactive time period prior to new transmission start-up	t_{BUF}	4.7		μs
Hold time during start condition (subsequent to this time period the first CLOCK pulse will be generated)	$t_{HD, STA}$	4.0		μs
LOW phase of clock	t_{LOW}	4.7		μs
HIGH phase of clock	t_{HIGH}	4.0		μs
Start-up for data	$t_{SU, DAT}$	250		ns
Rise time for SDA and SCL signal	t_r		1	μs
Fall time for SDA and SCL signal	t_f		300	ns
Start-up time for SCL clock during STOP conditions	$t_{SU, STO}$	4.7		μs

All values referred to V_{IH} and V_{IL} levels.

Diagram 7

Video signal – SAND – DZDA

