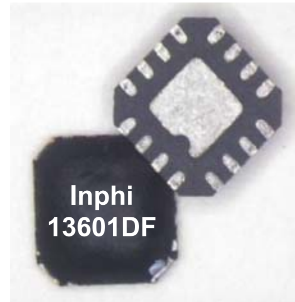
Think fast.

# 13601DF
# 13 Gbps D Flip-Flop
# Data Sheet




## Applications

- High-speed (up to 13 GHz) digital logic
- High-speed (up to 13 Gbps) serial data transmission systems
- Broadband test and measurement equipment

## Features

- Supports data rates up to 13 Gbps
- Very low random jitter: 37 fs rms typical
- Fast rise and fall times: < 25 ps
- Low power consumption: 300 mW
- Supports single-ended and differential operation
- Output signal swing 1200 mVpp differential
- Low Added Deterministic Jitter: 2 ps pp typical
- Single power supply: +3.3 V
- Available in QFN package
- Evaluation board available

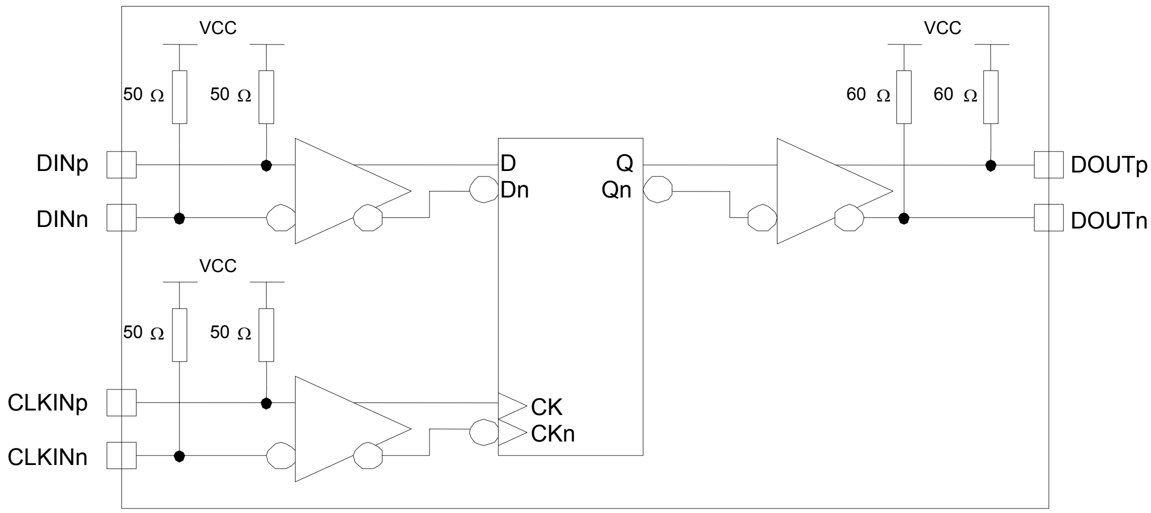
## Description

The 13601DF D flip-flop (DFF) is designed to support data rates up to 13 Gbps. The part is nominally positive-edge triggered; however, by reversing the positive and negative clock connections, a negative-edge triggered application can be accommodated.

All differential data and differential clock inputs are on-chip DC coupled and terminated with 50 Ω resistors to $V_{CC}$. For direct-coupled applications, the differential data outputs should be terminated off chip with 50 Ω resistors to $V_{CC}$ (+3.3 V). For applications requiring termination to DC levels other than $V_{CC}$ (i.e. ground referenced systems), external AC coupling to a good RF ground is required. See the application note for various termination examples.

The 13601DF operates from a single +3.3 V power supply and is available in a 3 x 3 $mm^2$ quad flat no-lead (QFN) package. The packaged part is also available on an evaluation board with SMA connectors.

## Block Diagram




## Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | | –0.5 | +3.6 | V |
| Input Signals (Data & Clock) | | | $V_{CC}$ – 2 | $V_{CC}$ + 1 | V |
| Output Signals | | | $V_{CC}$ – 2 | $V_{CC}$ + 1 | V |
| Junction Temperature – Die | $T_J$ | | –5 | +175 | °C |
| Case Temperature – Package paddle | $T_C$ | | –15 | +125 | °C |
| Shipping/Storage Temperature | $T_{STORE}$ | | –40 | +125 | °C |
| Humidity | RH | | 0 | 100 | % |
| ESD Protection (Human Body Model) | ESD | Clock and Data inputs | 500 | --- | V |
| | | Data outputs | 250 | --- | V |
| | | Power Supply | 500 | --- | V |

## Operating Conditions

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | ± 5% Tolerance | +3.135 | +3.300 | +3.465 | V |
| On-Chip Power Dissipation | $P_D$ | | --- | 300 | 410 | mW |
| Power Supply Current | $I_{CC}$ | | 70 | 91 | 115 | mA |
| Operating Temperature (Junction) – Die | $T_J$ | | +15 | --- | +125 | °C |
| Operating Temperature (Case) – Package | $T_C$ | Bottom of paddle | –5 | --- | +85 | °C |
| Thermal Resistance – junction to paddle | $R_{JC}$ ($\theta_{JC}$) | Bottom of paddle | --- | 51 | --- | °C/W |

# Electrical Specifications

**WARNING** – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum Data Rate | | $10^{-12}$ BER (NRZ format) | 13 | --- | --- | Gbps |
| Maximum Clock Frequency | $f_{MAX}$ | | 13 | --- | --- | GHz |
| Minimum Clock Slew Rate | $S_{MIN}$ | At crossing of CLKINp and CLKINn | --- | --- | 1 | V/ns |
| Input High Level (Data & Clock) | $V_{IH}$ | | $V_{CC} - 0.5$ | --- | $V_{CC} + 0.5$ | V |
| Input Low Level (Data & Clock) | $V_{IL}$ | | $V_{CC} - 1.0$ | --- | $V_{CC}$ | V |
| Input Amplitude (Data & Clock) | $VIN_{PP}$ & $VCLK_{PP}$ | Differential peak-to-peak | 300 | --- | 2000 | mVpp |
| | | Single-ended peak-to-peak | 300 | --- | 1000 | mVpp |
| Input Return Loss (Data & Clock) [1] | $RL_{IN}$ | Freq. < 13 GHz and Input common mode ($V_{ICM}$) $\leq V_{CC}$ | 10 | --- | --- | dB |
| Clock Phase Margin | CPM | $V_{IH} \leq V_{CC}$+0.3V | 280 | 300 | --- | deg |
| | | $V_{IH} > V_{CC}$+0.3V | 260 | 300 | --- | deg |
| Data Output Amplitude[2] | $D_{OUT}$ | Differential peak-to-peak | 900 | 1200 | 1400 | mVpp |
| Output High Voltage | $V_{OH}$ | DC coupled | $V_{CC} - 50$ | $V_{CC} - 4$ | $V_{CC}$ | mV |
| Output Common Mode | $V_{OCM}$ | DC coupled | --- | $V_{CC} - 300$ | --- | mV |
| Output Rise/Fall Time | $t_r/t_f$ | 20–80% | --- | 16 | 25 | ps |
| Output Return Loss[3] | $RL_{OUT}$ | Freq. < 13 GHz | 10 | --- | --- | dB |
| Added Deterministic Jitter[4, 5] | $J_D$ | Peak-to-peak at 12.5 Gbps | --- | 2 | 4 | ps |
| Added Random Jitter[4, 6] | $J_R$ | RMS at 10 GHz | --- | 37 | 80 | fs |
| Clock to Data Output Delay[4] | $t_Q$ | Packaged | 50 | 65 | 80 | ps |

Notes:

[1] Inputs are designed to be a broadband match a 50 Ω impedance and are terminated with a 50 Ω resistor to $V_{CC}$.

[2] Outputs are CML. Values are based on DC measurements.

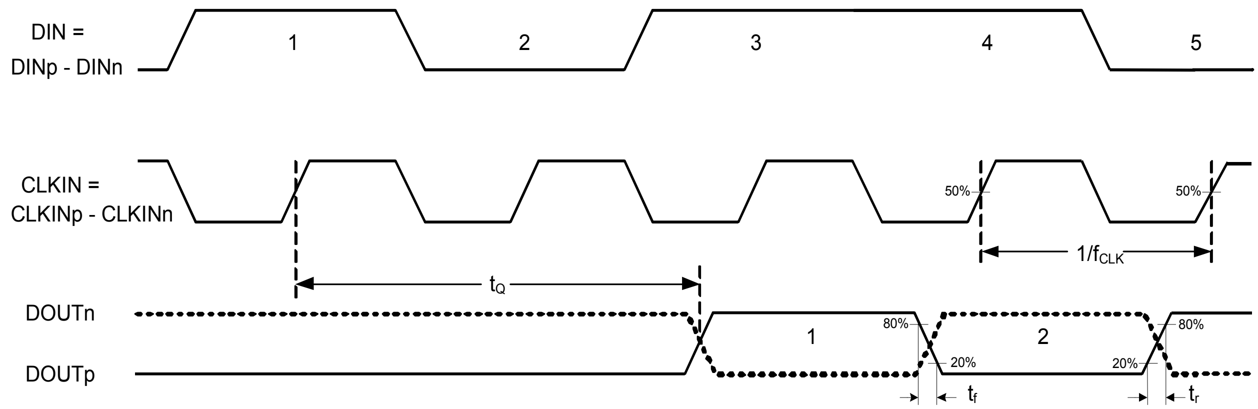
[3] Outputs are designed to be a broadband match a 50 Ω impedance and are terminated with a 60 Ω resistor to $V_{CC}$.

[4] Valid when clock to data phase is near center of CPM window. Propagation delay is based on simulations.

[5] The added deterministic jitter ($J_D$) specified is the total peak-to-peak jitter measured using a $2^{31}$-1 PRBS data pattern less the measured peak-to-peak jitter of the input clock source.

[6] The added random jitter ($J_R$) is the calculated RMS jitter based on residual phase noise measurements.

## Timing Diagram




Note: Not drawn to scale

## D-Flip Flop Truth Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| $DINp_{k-1}$ | $DINn_{k-1}$[1] | CLKINp | CLKINn[1] | $DOUTp_k$ | $DOUTn_k$[1] |
| L | H | ↑ | ↓ | L | H |
| H | L | ↑ | ↓ | H | L |

[1] DIN1n, CLKINn and DOUTn are complementary signals to DIN1p, CLKINp and DOUTp, respectively.

H Denotes a HIGH voltage level
L Denotes a LOW voltage level
↑ Denotes a rising clock transition
↓ Denotes a falling clock transition

# Typical DC Operating Characteristics

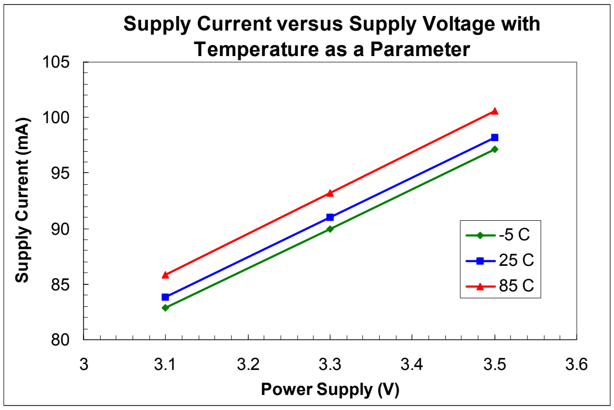



**Figure 1.** Power supply current vs. power supply voltage

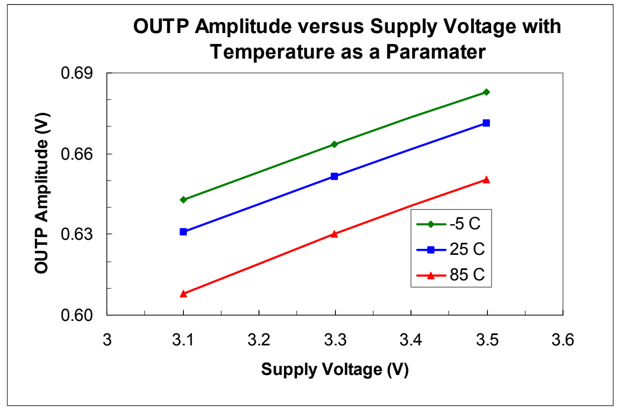



**Figure 2.** Single-ended, peak-to-peak output amplitude (on wafer) vs. power supply

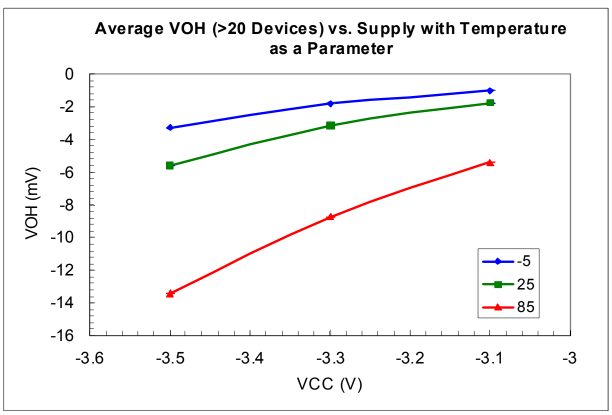



**Figure 3.** Single-ended, output high level (on wafer) vs. power supply

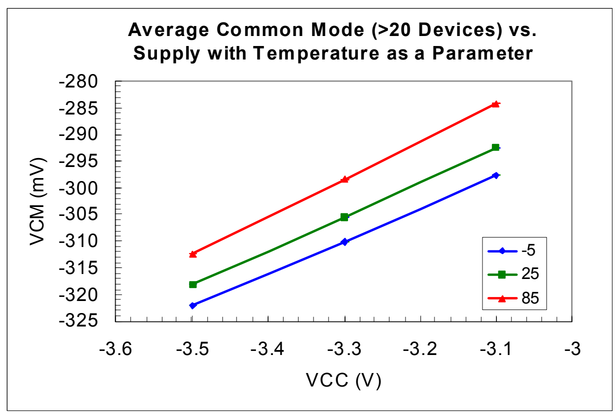



**Figure 4.** Output common mode (on wafer) vs. power supply

## Time Domain Operating Characteristics

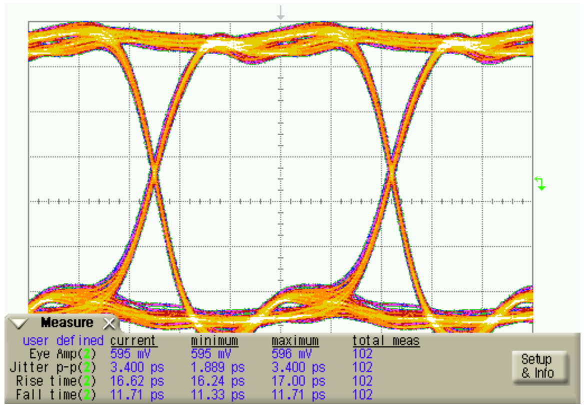



**Figure 5.** Output DOUTp (QFN package)

10 Gbps $2^{31-1}$ PRBS data input
100 mV/div 20 ps/div.

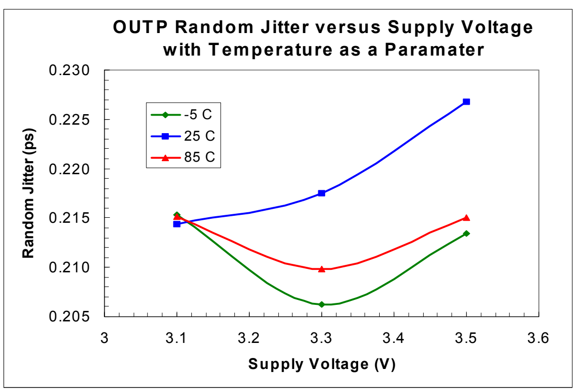



**Figure 6.** Output random jitter (on wafer) vs. power supply - refer to note #3 under Electrical Spec.

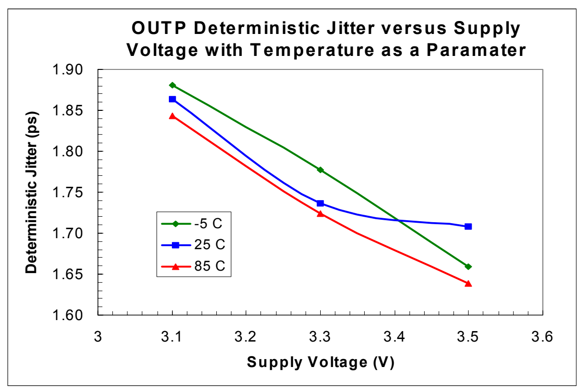



**Figure 7.** Output deterministic jitter (on wafer) vs. power supply - refer to note #3 under Electrical Spec.

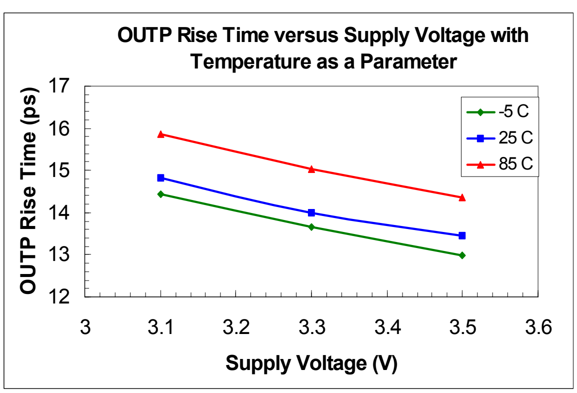



**Figure 8.** Output rise time (on wafer) vs. power supply

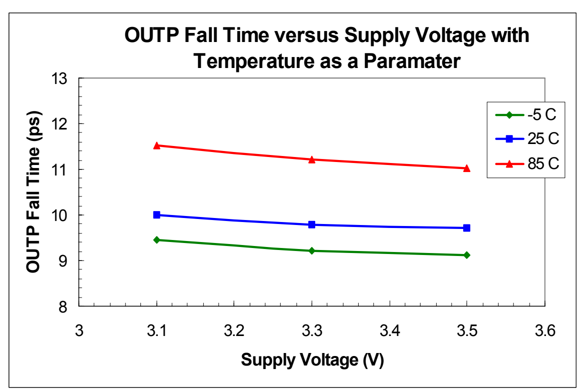



**Figure 9.** Output Fall Time (on wafer) vs. Power Supply

# Typical Return Losses

All S-parameter measurements were made single-ended. S-parameters for the packaged part are not given here due to the unavailability of calibration standards for the evaluation board.

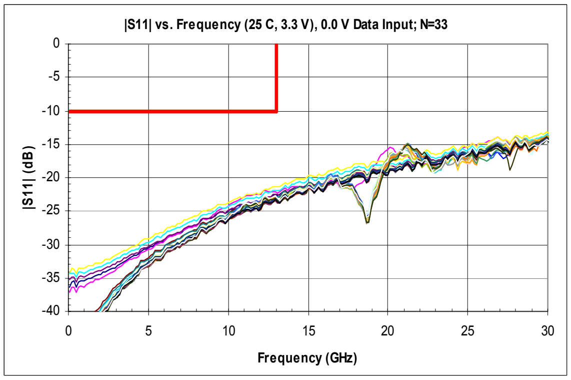



**Figure 10.** Data Input |S11| versus frequency of 33 die on wafer at Vcc = 3.3 V and 25° C; Input common mode = Vcc.

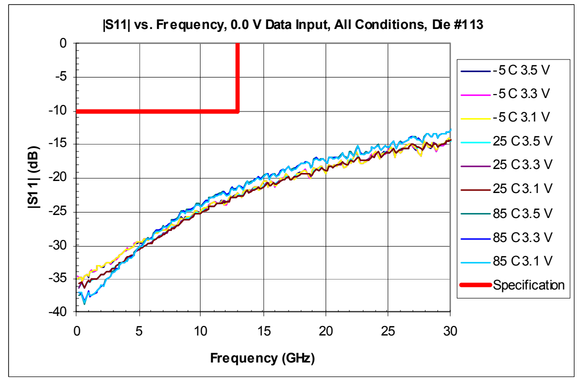



**Figure 11.** Data Input |S11| versus frequency of one dice on wafer at Vcc = 3.3 V and 25° C; Input common mode = Vcc.

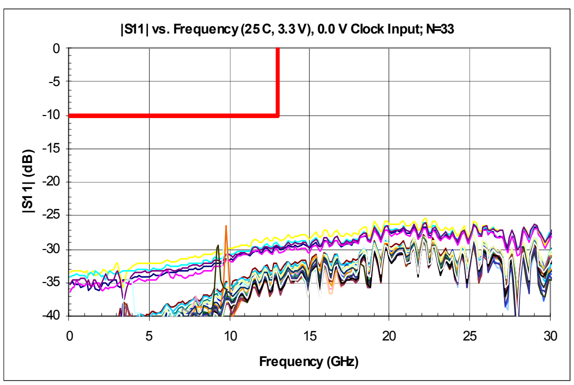



**Figure 12.** Clock Input |S11| versus frequency of 33 die on wafer at Vcc = 3.3 V and 25° C; Input common mode = Vcc.

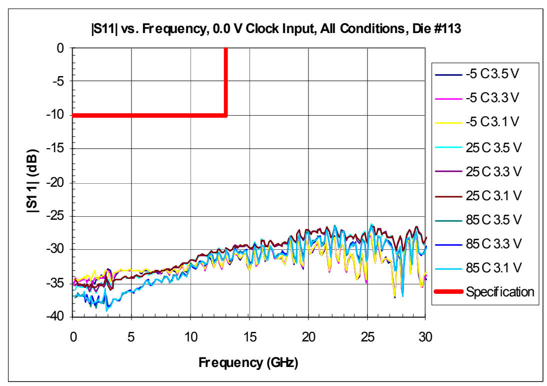



**Figure 13.** Clock Input |S11| versus frequency of one dice on wafer at Vcc = 3.3 V and 25° C; Input common mode = Vcc.

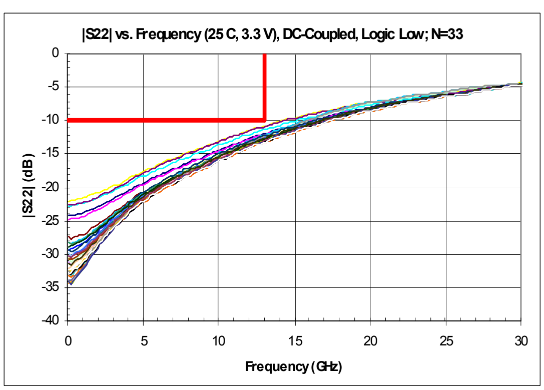



**Figure 14.** Data Output |S22| versus frequency of 33 die on wafer at Vcc = 3.3 V and 25° C; Output in logic low state. The output logic high state has about 3dB more margin.

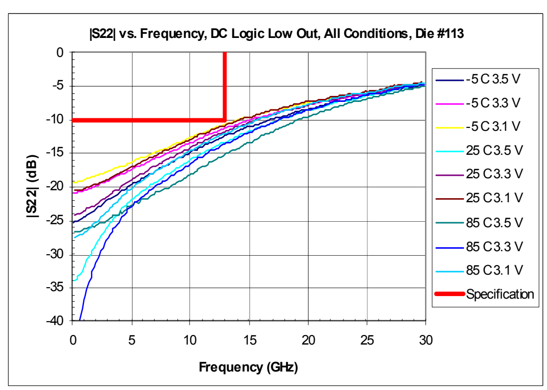
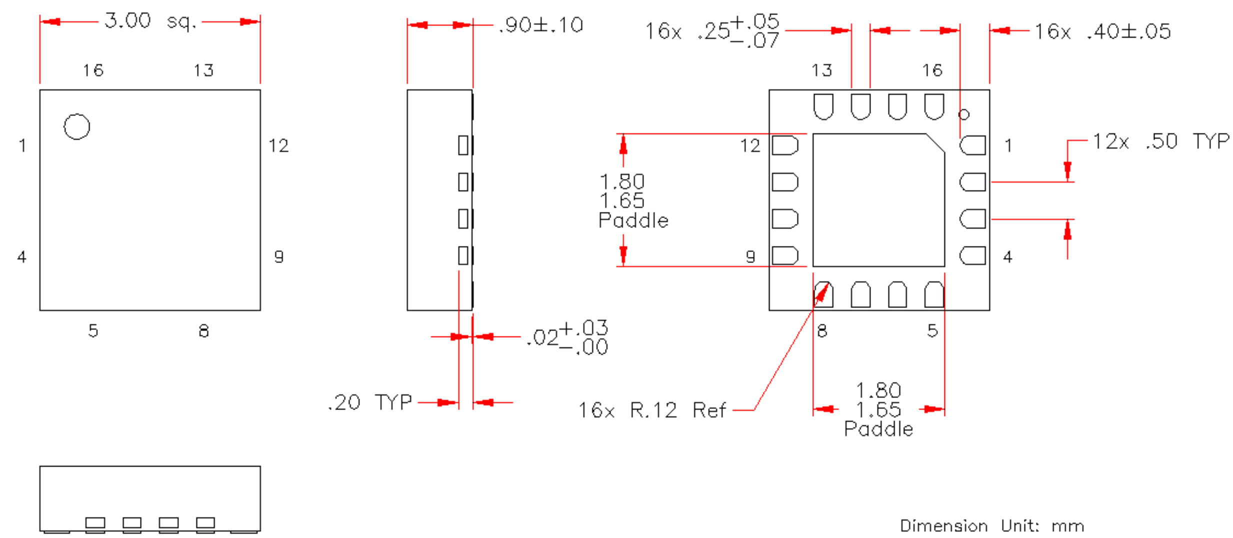



**Figure 15.** Data Output |S22| versus frequency of one dice on wafer at Vcc = 3.3 V and 25° C; Output in logic low state. The output logic high state has about 3dB more margin.

# QFN Package Outline Drawing and Pin Assignment




| Name | Pin | Description | Function |
|---|---|---|---|
| DINp | 3 | Non-inverting Data Input | Input |
| DINn | 2 | Inverting Data Input | Input |
| CLKINp | 6 | Non-inverting Clock Input | Input |
| CLKINn | 7 | Inverting Clock Input | Input |
| DOUTp | 11 | Non-inverting Data Output | Output |
| DOUTn | 10 | Inverting Data Output | Output |
| GND | 1, 4, 5, 8, 9, 12, 14, paddle | Ground | Supply |
| $V_{CC}$ | 13, 15, 16 | Power Supply: Connect to +3.3 V | Supply |

Note:
The paddle is the heat dissipation path and must be tied to the PCB ground planes by means of thermal vias.

## Order Information

| Part No. | Description |
|---|---|
| 13601DF-S02QFN | 13 Gbps D Flip-Flop (+3.3 V Supply) in QFN Package |
| 13601DF-S02QFN-EVB | 13 Gbps D Flip-Flop (+3.3 V Supply) in QFN Package on an Evaluation Board with SMA Connectors |

## Contact Information

**Inphi Corporation**
**2393 Townsgate Road, Suite 101**
**Westlake Village, CA 91361**

- Phone: (805) 446-5100
- Fax: (805) 446-5189
- E-mail: products@inphi-corp.com

Visit us on the Internet at: http://www.inphi-corp.com



## Qualification Notification

The 13601DF-S02 is fully qualified. Please contact Inphi for the qualification report.

**Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.**

## Version Updates

### From Version 2.2 to 2.3 (dated 2008-04-04)

1. Added the typical random and deterministic jitter numbers to the Features section (page 1).
2. Changed the jitter specifications in the Electrical Specifications table (page 3):
   a. Changed "Deterministic Jitter" parameter name to "Added Deterministic Jitter".
      i. Added "at 12.5 Gbps" to the Test Conditions.
      ii. Changed typical spec from 3 ps to 2 ps.
      iii. Changed Max spec from 6 ps to 4 ps.
      iv. Modified note #5.
   b. Changed "Random Jitter" parameter name to "Added Random Jitter".
      i. Added "at 10 GHz" to the Test Conditions.
      ii. Changed typical spec from 0.3 ps to 37 fs.
      iii. Changed Max spec from 0.6 ps to 80 fs.
      iv. Added note #6.
3. Added the requirement to use thermal vias from the package paddle to the PCB in the notes of the QFN Package Outline Drawing and Pin Assignment section (page 8).