

# OKI Semiconductor

## MSM514256H

262,144-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

### DESCRIPTION

The MSM514256H is a 262,144-word × 4-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM514256H achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon single metal CMOS. The MSM514256H is available in a 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP.

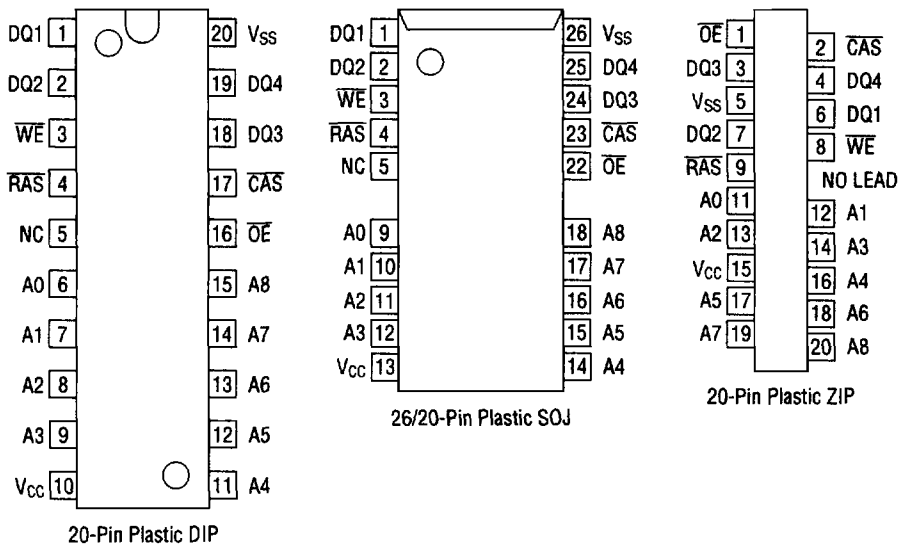
### FEATURES

- 262,144-word × 4-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 512 cycles/8 ms
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
- Package options:
  - 20-Pin 300 mil plastic DIP (DIP20-P-300-W1) (Product : MSM514256H-xxRS)
  - 26/20-Pin 300 mil plastic SOJ (SOJ26/20-P-300) (Product : MSM514256H-xxJS)
  - 20-Pin 400 mil plastic ZIP (ZIP20-P-400) (Product : MSM514256H-xxZS)xx indicates speed rank.

### PRODUCT FAMILY

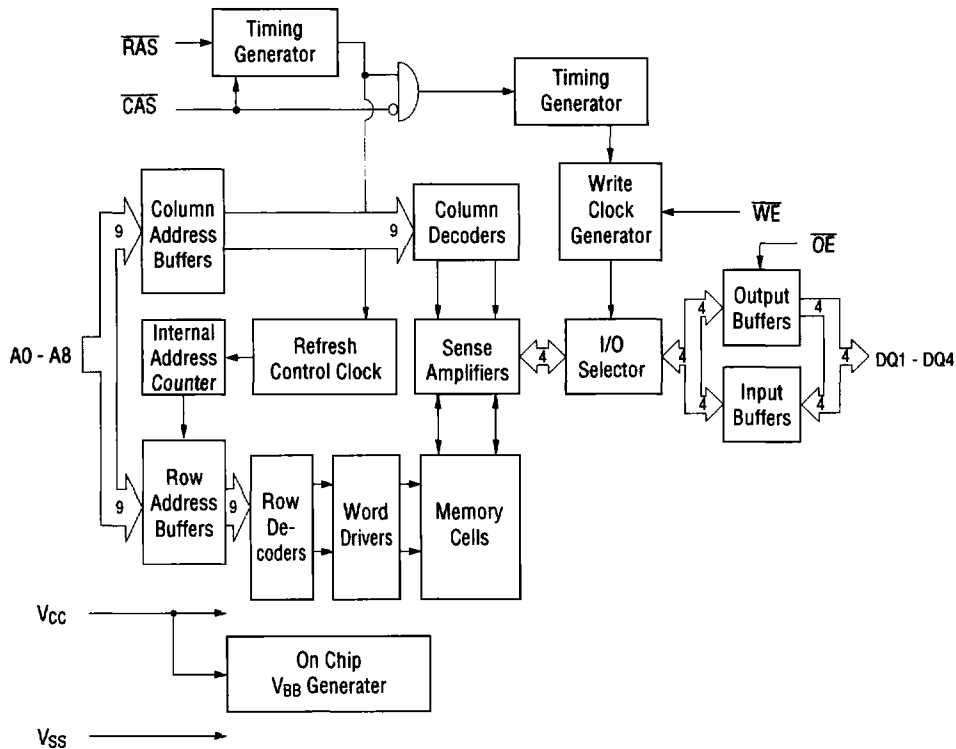
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating (Max.)	Standby (Max.)
MSM514256H-45	45 ns	24 ns	14 ns	14 ns	90 ns	550 mW	5.5 mW
MSM514256H-50	50 ns	26 ns	14 ns	14 ns	100 ns	523 mW	
MSM514256H-60	60 ns	30 ns	15 ns	15 ns	120 ns	468 mW	

## PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 - DQ4	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V <sub>CC</sub>	Power Supply (5 V)
V <sub>SS</sub>	Ground (0 V)
NC	No Connection

**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_T$	-1.0 to 7.0	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25^\circ\text{C}$ **Recommended Operating Conditions** $(T_a = 0^\circ\text{C to } 70^\circ\text{C})$ 

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.6	—	6.5	V
Input Low Voltage	$V_{IL}$	-1.0	—	0.8	V

**Capacitance** $(V_{CC} = 5\text{ V} \pm 10\%, T_a = 25^\circ\text{C}, f = 1\text{ MHz})$ 

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	$C_{IN1}$	—	5	pF
Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ )	$C_{IN2}$	—	5	pF
Output Capacitance (DQ1 - DQ4)	$C_{I/O}$	—	7	pF

## DC Characteristics

 $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ\text{C} \text{ to } 70^\circ\text{C})$ 

Parameter	Symbol	Condition	MSM514256 H-45		MSM514256 H-50		MSM514256 H-60		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	$I_{OH} = -5.0 \text{ mA}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2 \text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0V \leq V_I \leq 6.5V$ ; All other pins not under test = 0V	-10	10	-10	10	-10	10	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	DQ disable $0V \leq V_O \leq 5.5V$	-10	10	-10	10	-10	10	$\mu\text{A}$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	100	—	95	—	85	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ $\geq V_{CC} - 0.2V$	—	1	—	1	—	1		
Average Power Supply Current ( $\overline{\text{RAS}}$ -only Refresh)	$I_{CC3}$	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ , $t_{RC} = \text{Min.}$	—	100	—	95	—	85	mA	1, 2
Power Supply Current (Standby)	$I_{CC5}$	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	$I_{CC6}$	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	100	—	95	—	85	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$	—	95	—	90	—	80	mA	1, 3

- Notes :
1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.
  2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .
  3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C, Input Pulse Levels 0 V to 3 V) Note 1, 2, 3

Parameter	Symbol	MSM514256 H-45		MSM514256 H-50		MSM514256 H-60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	90	—	100	—	120	—	ns	
Read Modify Write Cycle Time	t <sub>RWC</sub>	140	—	150	—	170	—	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	34	—	36	—	40	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRWC</sub>	75	—	78	—	85	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	45	—	50	—	60	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	14	—	14	—	15	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	24	—	26	—	30	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	28	—	30	—	34	ns	4
Access Time from $\overline{\text{OE}}$	t <sub>OEA</sub>	—	14	—	14	—	15	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	10	0	10	0	10	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	10	0	10	0	10	ns	7
Transition Time	t <sub>r</sub>	3	50	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	8	—	8	—	8	ms	
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	35	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	45	10,000	50	10,000	60	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	45	100,000	50	100,000	60	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	14	—	14	—	15	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t <sub>ROH</sub>	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t <sub>CP</sub>	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	14	10,000	14	10,000	15	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	45	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>RHCP</sub>	28	—	30	—	34	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	17	31	18	36	20	45	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	12	21	13	24	15	30	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	7	—	8	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	12	—	13	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t <sub>AR</sub>	35	—	40	—	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	24	—	26	—	30	—	ns	

## AC Characteristics (2/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C, Input Pulse Levels 0 V to 3 V) Note 1, 2, 3

Parameter	Symbol	MSM514256 H-45		MSM514256 H-50		MSM514256 H-60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—		
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	9
Write Command Hold Time	t <sub>WCH</sub>	12	—	13	—	15	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t <sub>WCR</sub>	35	—	40	—	50	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OEH</sub>	12	—	13	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	14	—	14	—	15	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	14	—	14	—	15	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	10
Data-in Hold Time	t <sub>DH</sub>	12	—	13	—	15	—	ns	10
Data-in Hold Time from $\overline{\text{RAS}}$	t <sub>DHR</sub>	35	—	40	—	50	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t <sub>OED</sub>	12	—	13	—	15	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	36	—	38	—	42	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	48	—	52	—	58	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	70	—	75	—	85	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	52	—	56	—	62	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	0	—	0	—	0	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	25	—	25	—	25	—	ns	

- Notes:
1. A start-up delay of  $100\ \mu\text{s}$  is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5\ \text{ns}$ .
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  9.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  10. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in an early write cycle, and to  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle or a read modify write cycle.

**See ADDENDUM F for AC Timing Waveforms**