Data Sheet, DS2, Nov. 2000

# SLIC-S/-S2

## Subscriber Line Interface Circuit Standard Feature Set

## PEB 4264/-2 Version 1.1


Wired Communications

Infineon technologies

Never stop thinking.

**Edition 2000-11-09**

**Published by Infineon Technologies AG,**
**St.-Martin-Strasse 53,**
**D-81541 München, Germany**



**Attention please!**

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

**Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

**Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

# SLIC-S/-S2

## Subscriber Line Interface Circuit Standard Feature Set

## PEB 4264/-2 Version 1.1



Wired Communications

Infineon technologies

Never stop thinking.

**SLIC-S/-S2**
**Preliminary**
**Revision History:** **2000-11-09** DS2

Previous Version: Data Sheet DS1

| Page | Subjects (major changes since last revision) |
|---|---|
| **Page 3** | Note on SLIC clockwise pin counting added. |
| **Page 4** | Note on SLIC clockwise pin counting added. |
| **Page 4** | Pins DCN, DCP: factors – 30 and – 60 instead of 30 and 60 |
| **Page 9** | Description for modes modified. |
| **Page 11** | Junction temperature added,<br>conditions for "$V_{DD}$ supply voltage" changed,<br>"Input voltages" and "Voltages on current outputs" modified,<br>"Total battery supply voltage" changed from 95 V to 90 V,<br>Ring, Tip pulse < 10 ms: representation changed from voltage to power, footnote added |
| **Page 12** | Footnote on voltage range added; $V_{IT}$, $V_{IL}$, $V_{ACDC}$: condition added. |
| **Page 13** | Abstract about temperature range modified. |
| **Page 16** | Temperature range added. |
| **Page 19** | Temperature range added. |
| **Chapter 4** | All test figures: 470 nF condensator on pin CEXT is connected to ground. |
| **Page 31** | Note on SLIC clockwise pin counting added. |

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

## Table of Contents

## List of Figures

Page

# 1 Overview

The High Voltage Subscriber Line Interface Circuit PEB 4264/-2 (SLIC-S/-S2) is a reliable interface between the telephone line and the Dual Channel Codec IC PEB 3264/-2 (SLICOFI-2S/-2S2). It is fabricated in well-proven Smart Power Technology.

The PEB 4264/-2 provides battery feeding between – 15 V and – 65 V and internal ringing injection with a differential ringing voltage up to 45 Vrms. In order to achieve this, an auxiliary positive battery voltage is used during ringing to enhance the useable power voltage range to 90 V.

The SLIC is designed for a voltage-feeding/current-sensing line interface concept and senses the transversal and longitudinal current.

To minimize system power dissipation, a power-down mode can be used; the SLIC is switched off and the line outputs go to a high-impedance mode. Off-hook supervision is provided by activating a simple line current sensor with lowest power consumption.

For saving power in active mode with short loops, a switch for selecting between two different battery voltages is integrated into the chip.

**Preliminary**

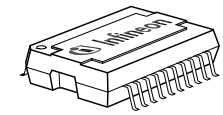
# Subscriber Line Interface Circuit Standard Feature Set SLIC-S/-S2

**PEB 4264/-2**

**Version 1.1**

## 1.1 Features

- High-voltage line feeding
- Battery voltage – 15 V … – 65 V
- Integrated balanced ringing with up to 45 Vrms ringing voltage
- Power-saving active mode (ACTL) with reduced battery voltage
- Sensing of transversal and longitudinal line currents
- Small P-DSO-20-5 power package
- Reliable Smart Power technology



P-DSO-20-5

| Type | Package |
|---|---|
| PEB 4264/-2 | P-DSO-20-5 |

## 1.2 Logic Symbol

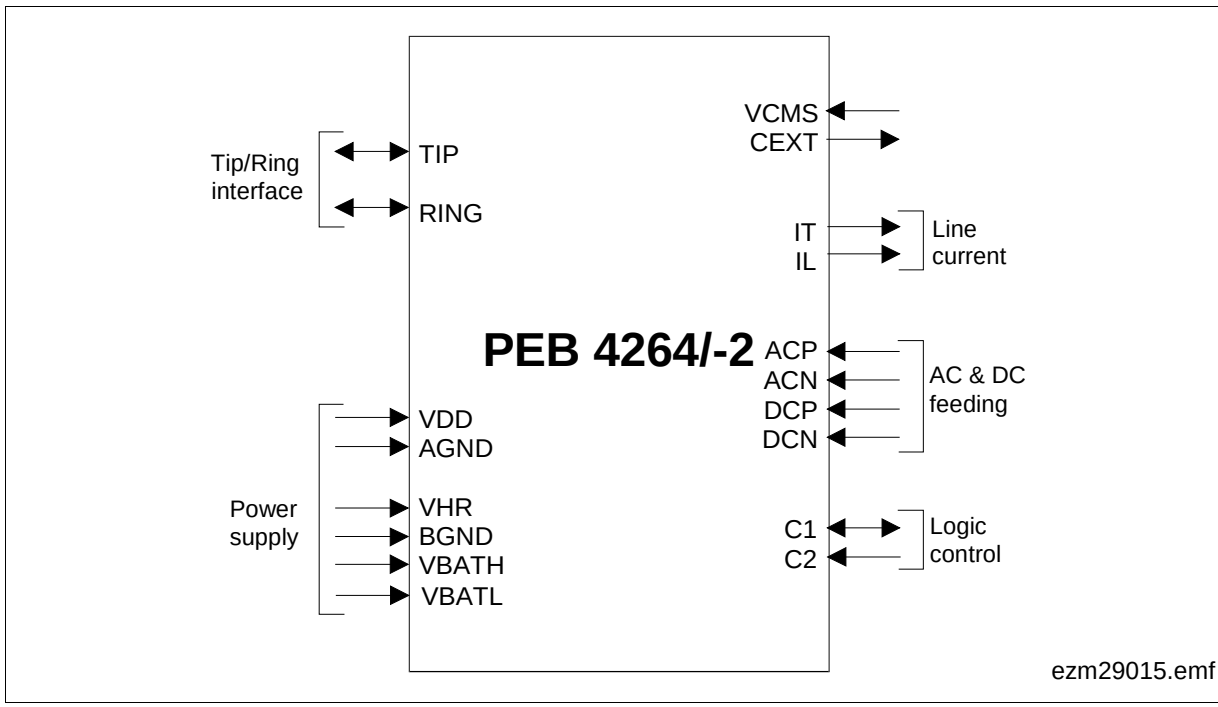



**Figure 1 Logic Symbol**

## 1.3 Pin Configuration

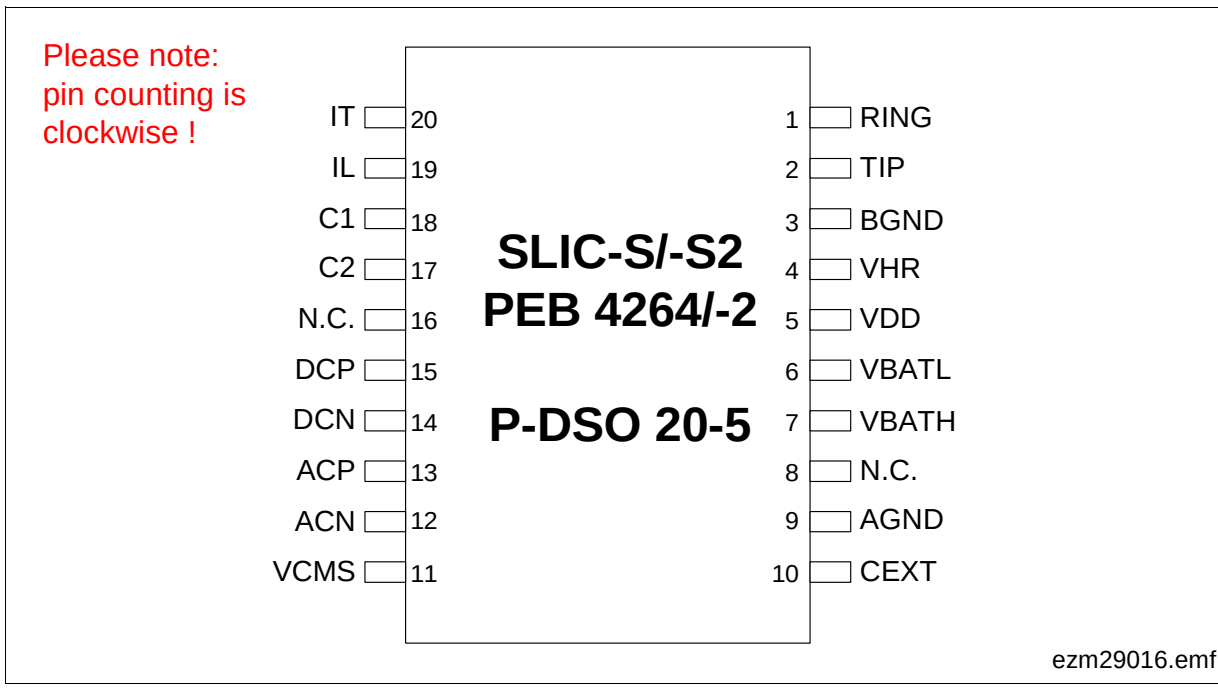



**Figure 2 Pin Configuration** (top view)

## 1.4 Pin Definitions and Functions SLIC-S/-S2

**Table 1 Pin Definitions and Functions SLIC-S/-S2**

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---|---|---|---|
| 1 | RING | I/O | Subscriber loop connection RING |
| 2 | TIP | I/O | Subscriber loop connection TIP |
| 3 | BGND | Power | Battery ground: TIP, RING, VBATH, VBATL and VHR refer to this pin |
| 4 | VHR | Power | Auxiliary positive battery supply voltage used in ringing mode |
| 5 | VDD | Power | Positive supply voltage (+ 5 V), referred to AGND |
| 6 | VBATL | Power | Negative battery supply voltage ($-15\ V \geq V_{BATL} \geq V_{BATH}$) |
| 7 | VBATH | Power | Negative battery supply voltage ($-20\ V \geq V_{BATH} \geq -65\ V$) |
| 8 | N.C. | | Not connected |
| 9 | AGND | Power | Analog ground: $V_{DD}$, and all signal and control pins with the exception of TIP and RING refer to AGND |
| 10 | CEXT | O | Output of voltage divider defining DC line potentials; an external capacitance allows supply voltage filtering (output resistance about 30 kΩ) |
| 11 | VCMS | I | Reference voltage for differential two wire interface, typical 1.5 V |
| 12, 13 | ACN, ACP | I | Differential two-wire AC input voltage; multiplied by – 6 and related to $(V_{HI} + V_{BI})/2$, ACN appears at TIP and ACP at RING output, respectively |
| 14, 15 | DCN, DCP | I | Differential two-wire DC input voltage; multiplied by a factor (– 30 in ACTH and ACTL mode, – 60 in ACTR mode) and related to $(V_{HI} + V_{BI})/2$[1)], DCN appears at TIP and DCP at RING output, respectively |
| 16 | N.C. | | Not connected |

**Table 1 Pin Definitions and Functions SLIC-S/-S2** (cont'd)

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---|---|---|---|
| 17 | C2 | I | Ternary logic input, controlling the operation mode |
| 18 | C1 | I/O | Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding 165 °C) this pin sinks a current of typically 150 µA |
| 19 | IL | O | Current output: longitudinal line current scaled down by a factor of 100. |
| 20 | IT | O | Current output representing the transversal current scaled down by a factor of 50. |

[1] $V_{HI}$ is the output voltage of the positive battery switch,
$V_{BI}$ is the output voltage of the negative battery switch (see **Figure 3**).

*Note: The SLIC is only available in a P-DSO-20-5 package with heatsink on top. Please note that the pin counting for the P-DSO-20-5 package is clockwise (top view) in contrast to similar type packages which mostly count counterclockwise.*

## 1.5 Functional Block Diagram

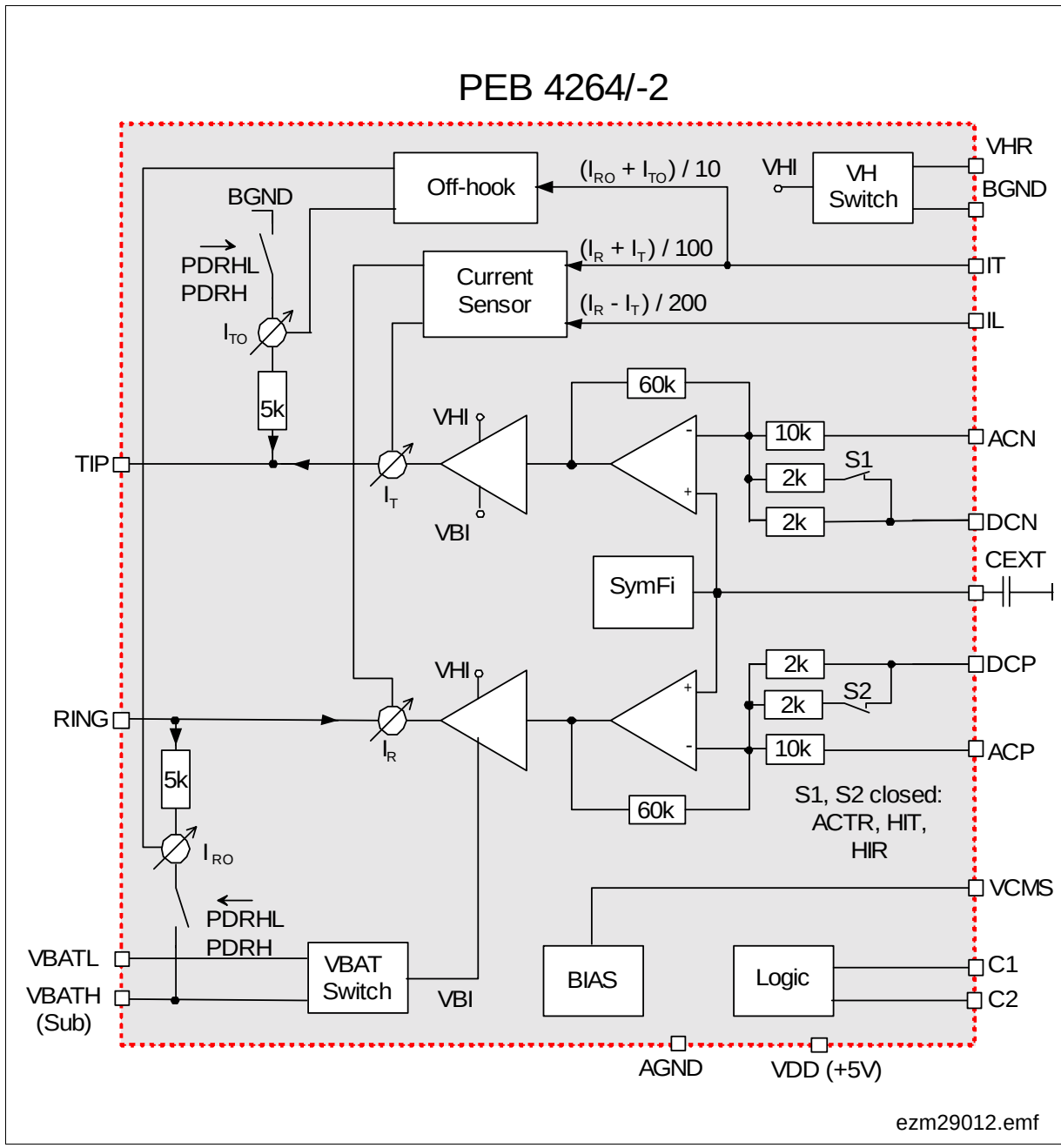



**Figure 3 Block Diagram**

# 2 Functional Description

The PEB 4264/-2 supports AC and DC control loops based on feeding a voltage $V_{RT}$ to the line and sensing the transversal line current $I_{Trans}$ and the longitudinal current $I_{Long}$ (**Figure 4**).

DC and AC voltages are handled separately with different gains on the SLIC. Both are applied differentially via, respectively, pins DCP and DCN or ACP and ACN.

The line voltages $V_R$ and $V_T$ are the amplified input voltages, related to the mean supply voltage $V_M = (V_{HI}{}^{1)} + V_{BI}{}^{1)})/2$, so in the active modes ACTH with $V_M = V_{BATH}/2$ and ACTL with $V_M = V_{BATL}/2$:

$$V_T = V_{TIP} = V_M - 30 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$
$$V_R = V_{RING} = V_M - 30 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS})$$

and in ringing mode ACTR with $V_M = [V_{HR} + V_{BATH}]/2$:

$$V_T = V_{TIP} = V_M - 60 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$
$$V_R = V_{RING} = V_M - 60 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS})$$

Depending on the operation mode, $V_{HI}$ is switched either to $V_{HR}$ or to $V_{BGND}$ via the VH switch. The transversal line voltage $V_{TR} = V_T - V_R$ has a simple relation to the input voltages:

$V_{TR} = V_T - V_R =$

$= 30 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$ ACTH, ACTL

$= 60 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$ ACTR

A reversed polarity of $V_{TR}$ is easily obtained by changing the sign of $(V_{DCP} - V_{DCN})$.

The transversal and longitudinal currents are measured in the buffers and scaled images are provided at the IT and IL pin, respectively:

| | |
|---|---|
| $I_{IT} = (I_T + I_R)/100 = I_{Trans}/50$ | $I_{IL} = -(I_T - I_R)/200 = -I_{Long}/100$ |
| $I_{Trans} = (I_T + I_R)/2$ | $I_{Long} = (I_T - I_R)/2$ |

1) $V_{HI}$ and $V_{BI}$ are internal voltages (see **Figure 3**).

The off-hook sensor currents $I_{T0}$, $I_{R0}$ in PDRH (and PDRHL) mode are measured via 5 kΩ resistors between TIP and BGND and RING and VBATH.
The scaled image is provided via the IT pin to the SLICOFI-2S/-2S2.

$I_{IT0} = (I_{T0} + I_{R0})/10 = I_{TRANS0}/5$

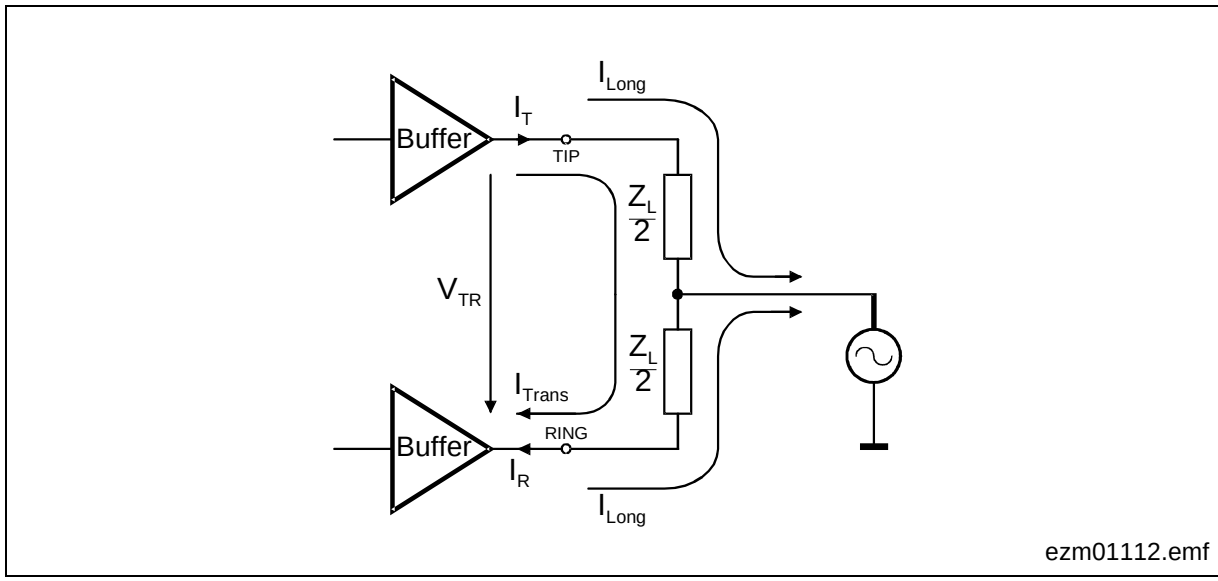



**Figure 4 Definition of Output Current Directions**

## 2.1 Operating Modes

The PEB 4264/-2 (SLIC-S/-S2) operates in the following modes controlled by ternary logic signals at the C1 and C2 inputs:

**Table 2 SLIC-S/-S2 Interface Code**

| | | C2 (Pin 17) | | |
|---|---|---|---|---|
| | | **L** | **M** | **H** |
| **C1 (Pin 18)** | **L**[1)] | PDH | PDRHL | PDRH |
| | **M** | ACTL | ACTH | ACTR |
| | **H** | unused | HIT | HIR |

1) No ‘Overtemp’ signaling possible via pin C1 if C1 is low.

Typical voltages for the C1 and C2 input pins are given at **Page 18**.

**Table 3 SLIC-S/-S2 Modes**

| SLIC-S/-S2 Mode | Mode Description | Used SLIC-S/-S2 Battery Voltage |
|---|---|---|
| **PDH** | Power Down High Impedance | $V_{BATH}$ |
| **PDRH** | Power Down Resistive High | $V_{BATH}$ |
| **PDRHL** | Power Down Resistive High Load | $V_{BATH}$ |
| **ACTL** | Active Low | $V_{BATL}$ |
| **ACTH** | Active High | $V_{BATH}$ |
| **ACTR** | Active Ring | $V_{BATH}$, $V_{HR}$ |
| **HIT** | High Impedance on TIP | $V_{BATH}$, $V_{HR}$ |
| **HIR** | High Impedance on RING | $V_{BATH}$, $V_{HR}$ |

With respect to the output impedance of TIP and RING, three Power Down modes have to be distinguished (see **Figure 5**):

**PDRH** is intended to reduce the power consumption of the linecard to a minimum by switching off the SLIC-S/-S2 completely. To allow off-hook detection, PDRH provides a connection of 5 kΩ each from TIP to $V_{BGND}$ and RING to $V_{BATH}$, respectively, while the output buffers show high impedance (see **Figure 5**). The current through these resistors is sensed and transferred to the IT pin for off-hook supervision.

**PDH** offers high impedance at TIP and RING and can be used to separate the Tip and Ring lines from the SLIC-S/-S2 outputs for testing purposes or when an error condition occurs. In PDH mode the current sensors are switched off. Off-hook detection is not available. PDH is also the safe operating mode for the SLIC-S/-S2 in case of overtemperature.

**PDRHL** is used as a transition state at a mode change from PDRH or PDH to ACTH mode (automatically initiated by SLICOFI-2S/-2S2 at a mode change). It is the same mode as PDRH with the exception of a preload of $C_{EXT}$.

**Active (ACTL, ACTH):** These are the regular transmission modes for voiceband. The line-driving section is operated between $V_{BATL}$, $V_{BATH}$ and $V_{BGND}$.

**Active Ring (ACTR):** This mode is used for balanced ringing of up to 45 Vrms or for extended battery feeding to drive longer telephone lines. An additional positive battery voltage $V_{HR}$ is used, making possible a higher voltage across the line.

**High Impedance (HIR/HIT):** In this mode each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer can still be measured by IT or IL.

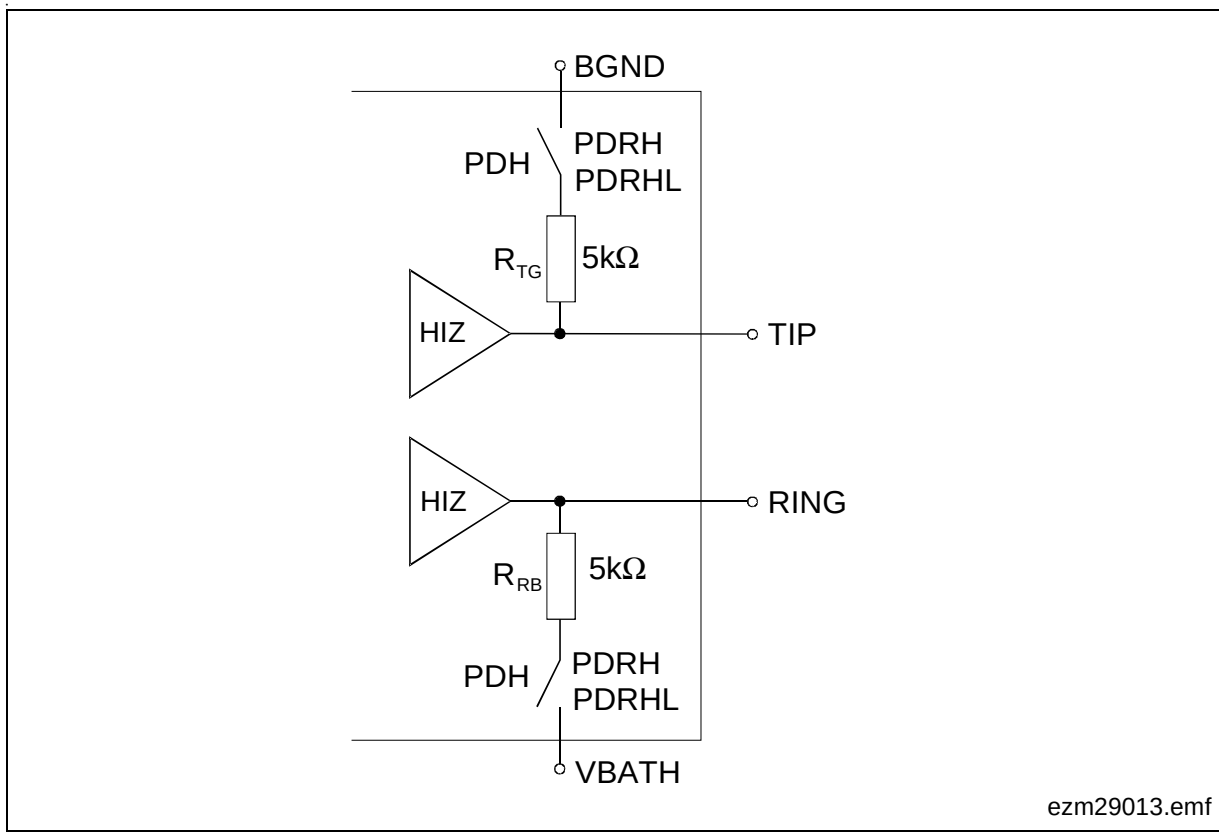



**Figure 5 TIP and RING Impedances in Power Down Modes**

# 3 Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Battery voltage L | $V_{BATL}$<br>$V_{BATL} - V_{BATH}$ | – 65<br>– 0.4 | 0.4 | V | referred to $V_{BGND}$ |
| Battery voltage | $V_{BATH}$ | – 70 | 0.4 | V | referred to $V_{BGND}$ |
| Auxiliary supply voltage | $V_{HR}$ | – 0.4 | 50 | V | referred to $V_{BGND}$ |
| Total battery supply voltage, continuous | $V_{HR} - V_{BATH}$ | – 0.4 | 90 | V | – |
| $V_{DD}$ supply voltage | $V_{DD}$ | – 0.4 | 7 | V | referred to $V_{AGND}$ |
| Ground voltage difference | $V_{BGND} - V_{AGND}$ | – 0.4 | 0.4 | V | – |
| Input voltages | $V_{DCP}$, $V_{DCN}$,<br>$V_{ACP}$, $V_{ACN}$,<br>$V_{C1}$, $V_{C2}$, $V_{CMS}$ | – 0.4 | $V_{DD}$ + 0.4 | V | referred to $V_{AGND}$ |
| Voltages on current outputs | $V_{IT}$, $V_{IL}$ | – 0.4 | $V_{DD}$ + 0.4 | V | referred to $V_{AGND}$ |
| RING, TIP voltages, continuous | $V_R$, $V_T$ | $V_{BATL}$ – 0.4<br>$V_{BATH}$ – 0.4<br><br>$V_{BATH}$ – 0.4 | 0.4<br>0.4<br><br>$V_{HR}$ + 0.4 | V<br>V<br><br>V | ACTL<br>ACTH, PDRH, PDRHL<br>ACTR, PDH, HIT, HIR |
| RING,TIP, pulse < 10 ms | $P_R$, $P_T$ [1)] | – | t.b.d | W | all modes |
| RING,TIP voltages, pulse < 100 µs | $V_R$, $V_T$ | $V_{BATH}$ – 10 | $V_{HR}$ + 10 | V | all modes |
| RING, TIP voltages, pulse < 1 µs | $V_R$, $V_T$ | $V_{BATH}$ – 10 | $V_{HR}$ + 30 | V | all modes |
| Junction temperature | $T_j$ | – | 150 [2)] | °C | – |
| ESD voltage, all pins | – | – | 1 | kV | SDM (Socketed Device Model)[3)] |

1) Power dissipation in the current limiting output buffer for Ring and Tip.

2) Even higher value is possible when internal junction temperature protection is operative.

3) EOS/ESD Assn. Standard DS5.3-1993.

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.*
*Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

## 3.2 Operating Range

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Battery voltage L [1] | $V_{BATL}$ | – 60 | – 15 | V | referred to $V_{BGND}$ |
| Battery voltage H [1] | $V_{BATH}$ | – 65 | – 20 | V | referred to $V_{BGND}$ |
| Auxiliary supply voltage | $V_{HR}$ | 5 | 45 | V | referred to $V_{BGND}$ |
| Total battery supply voltage | $V_{HR} - V_{BATH}$ | – | 90 | V | – |
| $V_{DD}$ supply voltage | $V_{DD}$ | 4.75 | 5.25 | V | referred to $V_{BGND}$ |
| Ground voltage difference | – | – 0.4 | 0.4 | V | – |
| Junction temperature | $T_j$ | – | 125 | °C | simulated for a lifetime of 15 years |
| Voltage at pins IT, IL | $V_{IT}$, $V_{IL}$ | – 0.4 | 3.5 | V | referred to $V_{AGND}$ |
| Input range $V_{DCP}$, $V_{DCN}$, $V_{ACP}$, $V_{ACN}$ | $V_{ACDC}$ | 0 | 3.3 | V | referred to $V_{AGND}$ |

1) If the battery switch is not used both pins VBATL and VBATH should be connected together externally. In this case the full voltage range of – 15 V to – 65 V can be used.

## 3.3 Thermal Resistances

| Parameter | Symbol | Limit Values | Unit | Test Condition |
|---|---|---|---|---|
| Junction to case | $R_{th, jC}$ | < 2 | K/W | – |
| Junction to ambient | $R_{th, jA}$ | < 50 | K/W | without heatsink |

## 3.4 Electrical Parameters

Minimum and maximum values are valid within the full operating range.

Functionality and performance is guaranteed for $T_A$ = 0 to 70 °C by production testing. Extented temperature range operation at – 40 °C < $T_A$ < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Testing is performed according to the specific test figures. Unless otherwise stated, load impedance $R_L$ = 600 Ω, $V_{BATH}$ = – 48 V, $V_{BATL}$ = – 24 V, $V_{HR}$ = + 32 V and $V_{DD}$ = + 5 V, $R_{IT}$ = 1 kΩ, $R_{IL}$ = 2 kΩ, $C_{EXT}$ = 470 nF. Typical values are tested at $T_A$ = 25 °C.

**Supply Currents and Power Dissipation**

($I_R$ = $I_T$ = 0 A; $V_{CMS}$ = $V_{ACP}$ = $V_{ACN}$ = $V_{DCP}$ = $V_{DCN}$ = 1.5 V)

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | |
| **Power Down High Impedance, Power Down Resistive High** | | | | | | | |
| 1.<br>2. | $V_{DD}$ current | $I_{DD}$ | PDH<br>PDRH | –<br>– | 120<br>120 | –<br>– | µA |
| 3.<br>4. | $V_{BATH}$ current | $I_{BATH}$ | PDH<br>PDRH | –<br>– | 65<br>80 | –<br>– | µA |
| 5.<br>6. | $V_{BATL}$ current | $I_{BATL}$ | PDH<br>PDRH | –<br>– | 0<br>0 | –<br>– | µA |
| 7.<br>8. | $V_{HR}$ current | $I_{HR}$ | PDH<br>PDRH | –<br>– | 0<br>0 | –<br>– | µA |
| 9.<br>10. | Quiescent power dissipation | $P_Q$ | PDH<br>PDRH | –<br>– | 3.7<br>4.4 | –<br>– | mW |
| **Power Down Resistive High Load** | | | | | | | |
| 11. | $V_{DD}$ current | $I_{DD}$ | PDRHL | – | 130 | – | µA |
| 12. | $V_{BATH}$ current | $I_{BATH}$ | PDRHL | – | 310 | – | µA |
| 13. | $V_{BATL}$ current | $I_{BATL}$ | PDRHL | – | 0 | – | µA |
| 14. | $V_{HR}$ current | $I_{HR}$ | PDRHL | – | 0 | – | µA |
| 15. | Quiescent power dissipation | $P_Q$ | PDRHL | – | 15.5 | – | mW |

## Supply Currents and Power Dissipation

($I_R$ = $I_T$ = 0 A; $V_{CMS}$ = $V_{ACP}$ = $V_{ACN}$ = $V_{DCP}$ = $V_{DCN}$ = 1.5 V) (cont'd)

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | |
| **Active Low** | | | | | | | |
| 16. | $V_{DD}$ current | $I_{DD}$ | ACTL | – | 1000 | 1200 | µA |
| 17. | $V_{BATH}$ current | $I_{BATH}$ | ACTL | – | 25 | 45 | µA |
| 18. | $V_{BATL}$ current | $I_{BATL}$ | ACTL | – | 2800 | 3400 | µA |
| 19. | $V_{HR}$ current | $I_{HR}$ | ACTL | – | 0 | 10 | µA |
| 20. | Quiescent power dissipation | $P_Q$ | ACTL | – | 73.4 | 89.8 | mW |
| **Active High** | | | | | | | |
| 21. | $V_{DD}$ current | $I_{DD}$ | ACTH | – | 1000 | 1300 | µA |
| 22. | $V_{BATH}$ current | $I_{BATH}$ | ACTH | – | 3500 | 4300 | µA |
| 23. | $V_{BATL}$ current | $I_{BATL}$ | ACTH | – | 0 | 10 | µA |
| 24. | $V_{HR}$ current | $I_{HR}$ | ACTH | – | 0 | 10 | µA |
| 25. | Quiescent power dissipation | $P_Q$ | ACTH | – | 173 | 213.5 | mW |
| **Active Ring** | | | | | | | |
| 26. | $V_{DD}$ current | $I_{DD}$ | ACTR | – | 500 | 700 | µA |
| 27. | $V_{BATH}$ current | $I_{BATH}$ | ACTR | – | 3100 | 3700 | µA |
| 28. | $V_{BATL}$ current | $I_{BATL}$ | ACTR | – | 0 | 10 | µA |
| 29. | $V_{HR}$ current | $I_{HR}$ | ACTR | – | 2300 | 2800 | µA |
| 30. | Quiescent power dissipation | $P_Q$ | ACTR | – | 225 | 271 | mW |
| **High Impedance on RING, High Impedance on TIP** | | | | | | | |
| 31. | $V_{DD}$ current | $I_{DD}$ | HIR, HIT | – | 500 | 700 | µA |
| 32. | $V_{BATH}$ current | $I_{BATH}$ | HIR, HIT | – | 2100 | 2600 | µA |
| 33. | $V_{BATL}$ current | $I_{BATL}$ | HIR, HIT | – | 0 | 10 | µA |
| 34. | $V_{HR}$ current | $I_{HR}$ | HIR, HIT | – | 1500 | 2200 | µA |
| 35. | Quiescent power dissipation | $P_Q$ | HIR, HIT | – | 151 | 199 | mW |

### 3.4.1 Power Calculation PEB 4264/-2

The total power dissipation consists of the quiescent power dissipation $P_Q$ given above, the current sensor power dissipation $P_I$, the gain stage power dissipation correction $P_G$[1)] and the output stage power dissipation $P_O$:

$$P_{tot} = P_Q + P_I + P_G + P_O$$

with $P_Q = V_{DD} \times I_{DD} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL} + V_{HR} \times I_{HR}$

## 3.5 Power Up Sequence of Supply Voltages

The supply voltages of the SLIC-S/-S2 have to be applied in the following order to the respective pin:

1) Ground to pins AGND and BGND
2) $V_{DD}$ to pin VDD
3) $V_{BATH}$ to pin VBATH
4) $V_{HR}$ to pin VHR and $V_{BATL}$ to pin VBATL

If the $V_{DD}$ voltage is applied more than one second later as $V_{BATH}$, $V_{HR}$ or $V_{BATL}$ thermal damage of the SLIC can accur.

If the above sequence of the battery voltages can not be guaranteed, a diode (1N4007) has to be inserted in the VBATH line.

1) The gain stage power dissipation correction $P_G$ is a correcting term necessary to ensure a correct power calculation if other as the defined supply voltages are used.

## 3.6 DC Characteristics

$T_A$ = – 40 °C to 85 °C, unless otherwise stated.

**Table 4**

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | | |
| **Line Termination TIP, RING** | | | | | | | | |
| 36. | DC line voltage | $V_{TR, DC}$ | ACTL, ACTH, ACTR | – 0.4 | 0 | 0.4 | V | $V_{DCP} = V_{DCN} = V_{ACP} = V_{ACN} = V_{CMS}$ = 1.5 V |
| 37. | | $V_{TIP, DC}$ | ACTL | – 13 | – 12 | – 11 | V | $V_{DCP} = V_{DCN} = V_{ACP} = V_{ACN} = V_{CMS}$ = 1.5 V |
| 38. | | | ACTH | – 25 | – 24 | – 23 | V | $V_{DCP} = V_{DCN} = V_{ACP} = V_{ACN} = V_{CMS}$ = 1.5 V |
| 39. | | | ACTR | – 12 | – 10 | – 8 | V | $V_{DCP} = V_{DCN} = V_{ACP} = V_{ACN} = V_{CMS}$ = 1.5 V |
| 40. | | $V_{TR, DC}$ | ACTH | 23.5 | 24 | 24.5 | V | $V_{DCP} – V_{CMS} = V_{CMS} – V_{DCN}$ = 0.4 V, $V_{ACP} = V_{ACN} = V_{CMS}$ = 1.5 V |
| 41. | | | | – 24.5 | – 24 | – 23.5 | V | $V_{DCP} – V_{CMS} = V_{CMS} – V_{DCN}$ = – 0.4 V, $V_{ACP} = V_{ACN} = V_{CMS}$ = 1.5 V |
| 42. | DC line voltage drop | $– V_{BATH}$ $– V_{TR, max}$ | ACTH | – | 2 | 3 | V | $I_{Trans}$ = 20 mA, $V_{DCP} – V_{CMS} = V_{CMS} – V_{DCN}$ = 1.5 V, $V_{ACP} = V_{ACN} = V_{CMS}$ = 1.5 V |
| 43. | Output current limit (see **Figure 7**) | $\|I_{R, max}\|$, $\|I_{T, max}\|$ | ACTL, ACTH, ACTR, ROR, ROT | 80 | 105 | 130 | mA | $V_R$, $V_T$ |
| 44. | | $\|I_{T, max}\|$ $\|I_{R, max}\|$ | HIR HIT | 80 80 | 105 105 | 130 130 | mA mA | |
| 45. | Loop open resistance TIP to $V_{BGND}$ (see **Figure 8**) | $R_{TG}$ | PDRHL, PDRH | 4.25 | 5 | 5.75 | kΩ | $I_T$ = 2 mA, Temp = 25 °C[1)] |
| 46. | Loop open resistance RING to $V_{BATH}$ (see **Figure 8**) | $R_{RB}$ | PDRHL, PDRH | 4.25 | 5 | 5.75 | kΩ | $I_R$ = 2 mA, Temp = 25 °C[1)] |

**Table 4** (cont'd)

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | | |
| 47. | Power down output leakage current | $I_{Leak,R}$ | PDH | – 30 | 0 | 30 | µA | $V_{BATH} < V_R < V_{HR}$ |
| 48. | | $I_{Leak,T}$ | | – 30 | 0 | 30 | µA | $V_{BATH} < V_T < V_{HR}$ |
| 49. | High impedance output leakage current | $I_{Leak,R}$ | HIR | – 30 | 0 | 30 | µA | $V_{BATH} < V_R < V_{HR} - 3$ |
| 50. | | $I_{Leak,T}$ | HIT | – 30 | 0 | 30 | µA | $V_{BATH} < V_T < V_{HR} - 3$ |
| **Inputs DCP, DCN, ACP, ACN** | | | | | | | | |
| 51. | Input resistance DCP, DCN | $R_{DC}$ | ACTR, HIR, HIT | 0.85 | 1 | 1.15 | kΩ | Temp = 25 °C[1] |
| 52. | | | all other | 1.7 | 2 | 2.3 | kΩ | Temp = 25 °C[1] |
| 53. | Input resistance ACP, ACN | $R_{AC}$ | all | 8.0 | 10 | 12 | kΩ | Temp = 25 °C[1] |
| 54. | Input resistance VCMS | $R_{CMS}$ | ACTR, HIR, HIT | 1.39 | 1.64 | 1.89 | kΩ | Temp = 25 °C[1] |
| 55. | | | all other | 2.55 | 3 | 3.45 | kΩ | Temp = 25 °C[1] |
| **Current Outputs IT, IL** | | | | | | | | |
| 56. | IT output current | $I_{IT}$ | ACTL, ACTH | – 15 | 0 | 15 | µA | $I_R = I_T = 0$ mA |
| 57. | Transversal current ratio | $1/G_{IT,DC}$ [2] | ACTL, ACTH | 49.5 | 50 | 50.5 | – | $I_R = I_T = 20$ mA |
| 58. | (guaranteed by design, see **Figure 9**) | | ACTL, ACTH | 49.5 | 50 | 50.5 | – | $I_R = I_T = – 20$ mA |
| 59. | Off-hook output current on $I_T$ | | PDRHL, PDRH | 780 | 960 | 1140 | µA | TIP/RING shorted<br>$V_{BATH} = – 48$ V<br>Temp = 25 °C[1] |

**Table 4** (cont'd)

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | | |
| 60. | IL output current | $I_{IL}$ | ACTL, ACTH | – 20 | 0 | 20 | µA | $I_R = I_T$ = 20 mA |
| 61. | (see **Figure 9**) | | ACTL, ACTH | 25 | 50 | 75 | µA | $I_R$ = 15 mA, $I_T$ = 25 mA |
| 62. | | | ACTL, ACTH | – 158 | – 125 | – 93 | µA | $I_R$ = 62.5 mA, $I_T$ = 37.5 mA |
| **Control Inputs C1, C2** | | | | | | | | |
| 63. | H-input voltage | $V_{IH}$ | all | 2.7 | – | $V_{DD}$ + 0.3 | V | – |
| 64. | M-input voltage | $V_{IM}$ | all | 1.2 | 1.65 | 2.1 | V | – |
| 65. | L-input voltage | $V_{IL}$ | all | – 0.3 | – | 0.6 | V | – |
| 66. | Input leakage current | $I_{Leak}$ | all | – 5 | 0 | 5 | µA | 0 < $V_{C1}$ ($V_{C2}$) < $V_{DD}$ |
| 67. | Thermal overload current C1 | $I_{therm}$ | ACTL, ACTH, ACTR, HIT, HIR | 130 | 150 | 250 | µA | $V_{C1}$ = 1.20 V |
| 68. | Junction temperature protection Jtp (guaranteed by design) | $T_{jLIM}$ | ACTL, ACTH, ACTR, HIT, HIR | – | 165 | – | °C | – |

1) The systematic temperature dependency of these resistances is + 0.1%/°C.

2) The offset ($I_R = I_T$ = 0 mA) has to be taken into account.

## 3.7 AC Characteristics

$T_A$ = – 40 °C to 85 °C, unless otherwise stated.

**Table 5**

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | | |
| **Line Termination TIP, RING** | | | | | | | | |
| 69.<br>70. | Receive gain (see **Figure 10**) | $G_r$ | ACTL<br>ACTH | 5.925<br>5.925 | 6.0<br>6.0 | 6.075<br>6.075 | –<br>– | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA (ACTH)<br>$V_{ACP} - V_{CMS} = V_{CMS} - V_{ACN}$ = 320 mVrms<br>$f$ = 1015 Hz |
| 71. | Total harmonic distortion $V_{TR}$ (see **Figure 10**) | *THD* | ACTL, ACTH | – | 0.03 | 0.3 | % | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA (ACTH)<br>$V_{ACP} - V_{CMS} = V_{CMS} - V_{ACN}$ = 320 mVrms<br>$f$ = 1015 Hz |
| 72.<br>73. | Teletax distortion | *THDTTX* | ACTL<br>ACTH | –<br>– | 0.4<br>0.8 | 2<br>3 | %<br>% | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 0 mA,<br>$I_{Trans,DC}$ = 25 mA (ACTH)<br>$V_{TR,AC}$ = 5 Vrms<br>$f$ = 16 kHz, $R_L$ = 200 Ω |
| 74. | Psophometric noise (see **Figure 10**) | $N_{pVTR}$ | ACTL, ACTH | – | – 78 | – 76 | dBmp | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA (ACTH) |
| 75. | Longitudinal to transversal rejection ratio $V_{long}/V_{TR}$ (see **Figure 11**) | *LTRR* | ACTL<br>ACTH | 60<br>60 | 70<br>70 | –<br>– | dB<br>dB | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA (ACTH)<br>$V_{long}$ = 3 Vrms<br>300 Hz < $f$ < 3.4 kHz |
| | Longitudinal to transversal rejection ratio $V_{long}/V_{TR}$ (loop) | *LTRR-1 loop* | ACTH | | | | | PEB 4264:<br>$I_{Trans,DC}$ = 25 mA<br>$V_{long}$ = 3 Vrms |
| 76.<br>77. | (see **Figure 12**) | | | 54<br>52 | 58<br>56 | –<br>– | dB<br>dB | 300 Hz < $f$ < 1 kHz<br>3.4 kHz |

**Table 5** (cont'd)

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | | |
| | Longitudinal to transversal rejection ratio $V_{long}/V_{TR}$ | *LTRR-2 loop* | ACTH | | | | | PEB 4264-2: $I_{Trans,DC}$ = 25 mA $V_{long}$ = 3 Vrms |
| 78. | (loop) | | | 61 | 65 | – | dB | 300 Hz < $f$ < 1 kHz |
| 79. | (see **Figure 12**) | | | 56 | 60 | – | dB | 3.4 kHz |
| 80. | Transversal to longitudinal rejection ratio $V_{TR}/V_{long}$ (see **Figure 13**) | *TLRR* | ACTL<br>ACTH | 48<br>48 | 58<br>58 | –<br>– | dB<br>dB | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA (ACTH)<br>$V_{ACP} - V_{CMS} = V_{CMS} - V_{ACN}$ = 960 mVrms<br>300 Hz < $f$ < 3.4 kHz |
| | Power supply rejection ratio | *PSRR* | | | | | | $I_{Trans,DC}$ = 25 mA (ACTH), $I_{Trans,DC}$ = 25 mA (ACTR) $I_{Trans,DC}$ = 15 mA (ACTL) $V_{SupplyAC}$ = 100 mVp |
| 81. | $V_{BATL}/V_{TR}$ | | ACTL | 40 | 60 | – | dB | 300 Hz < $f$ < 3.4 kHz |
| 82. | $V_{BATH}/V_{TR}$ | | ACTH | 40 | 60 | – | dB | |
| 83. | (see **Figure 10**) | | ACTR | 33 | 50 | – | dB | |
| 84. | $V_{HR}/V_{TR}$ | | ACTH, ACTR | 33 | 45 | – | dB | |
| 85. | $V_{DD}/V_{TR}$ | | ACTL | 33 | 50 | – | dB | |
| 86. | | | ACTH | 33 | 50 | – | dB | |
| 87. | | | ACTR | 25 | 35 | – | dB | |
| 88. | reserved | | | | | | | |
| 89. | reserved | | | | | | | |
| 90. | reserved | | | | | | | |
| 91. | reserved | | | | | | | |
| 92. | reserved | | | | | | | |
| 93. | reserved | | | | | | | |
| 94. | Ringing amplitude TIP/RING | $V_{RNG0}$ | ACTR | 43 | 45 | 47 | Vrms | $V_{DCP} - V_{DCN}$ = 0.15 V (DC) + 0.75 Vrms (sine wave), $V_{HR}$ = + 32 V |
| 95. | Ringing amplitude ringer | $V_{RNG}$ | | 33 | 35 | 37 | Vrms | $R_{line}$ = 1500 Ω, $R_R$ = 450 Ω, |
| 96. | Ringing distortion (see **Figure 14**) | RD | | – | 0.1 | 2 | % | $C_R$ = 3.4 µF, $f$ = 20 Hz |

**Table 5** (cont'd)

| No. | Parameter | Symbol | Mode | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | | |
| 97.<br>98. | Transversal current ratio (see **Figure 10**) | $1/G_{it}$ | ACTL<br>ACTH | 49.5<br>49.5 | 50<br>50 | 50.5<br>50.5 | –<br>– | $I_{Trans,DC}$ = 15 mA, $I_{Trans,DC}$ = – 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA, $I_{Trans,DC}$ = – 25 mA (ACTH)<br>$V_{ACP} - V_{CMS} = V_{CMS} - V_{ACN}$ = 320 mVrms<br>$f$ = 1015 Hz |
| 99.<br>100. | Total harmonic distortion $V_{IT}$ (see **Figure 10**) | $THD_{IT}$ | ACTL,<br>ACTH | –<br>–<br>– | 0.02<br>0.3<br>0.01 | 0.3<br>1.5<br>0.3 | %<br>%<br>% | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 0 mA,<br>$I_{Trans,DC}$ = 25 mA (ACTH)<br>$V_{ACP} - V_{CMS} = V_{CMS} - V_{ACN}$ = 320 mVrms<br>$f$ = 1015 Hz |
| 101. | Psophometric noise (see **Figure 10**) | $N_{pVIT}$ | ACTL,<br>ACTH | – | – 107 | – 105 | dBmp | $I_{Trans,DC}$ = 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA (ACTH) |
| 102.<br>103. | Longitudinal to transversal current output rejection ratio $V_{long}/V_{IT}$ (see **Figure 11**) | $LITRR$ | ACTL<br>ACTH | 78<br>78 | 81<br>81 | –<br>– | dB<br>dB | $I_{Trans,DC}$ = 15 mA, $I_{Trans,DC}$ = – 15 mA (ACTL)<br>$I_{Trans,DC}$ = 25 mA, $I_{Trans,DC}$ = – 25 mA (ACTH),<br>$V_{long}$ = 3 Vrms<br>300 Hz < $f$ < 3.4 kHz |
| | Power supply rejection ratio | $PSRR$ | | | | | | $I_{Trans,DC}$ = 25 mA (ACTH), $I_{Trans,DC}$ = 25 mA (ACTR) $I_{Trans,DC}$ = 15 mA (ACTL)<br>$V_{SupplyAC}$ = 100 mVp<br>300 Hz < $f$ < 3.4 kHz |
| 104. | $V_{BATL}/V_{IT}$ | | ACTL | 50 | 60 | – | dB | |
| 105. | $V_{BATH}/V_{IT}$ | | ACTH | 60 | 70 | – | dB | |
| 106. | $V_{HR}/V_{IT}$ | | ACTR | 60 | 70 | – | dB | |
| 107. | $V_{HR}/V_{IT}$ | | ACTR | 50 | 60 | – | dB | |
| 108. | $V_{DD}/V_{IT}$ (see **Figure 10**) | | ACTL<br>ACTH<br>ACTR | 55<br>55<br>50 | 70<br>70<br>60 | –<br>–<br>– | dB<br>dB<br>dB | |

# 4 Test Figures and Application Circuits

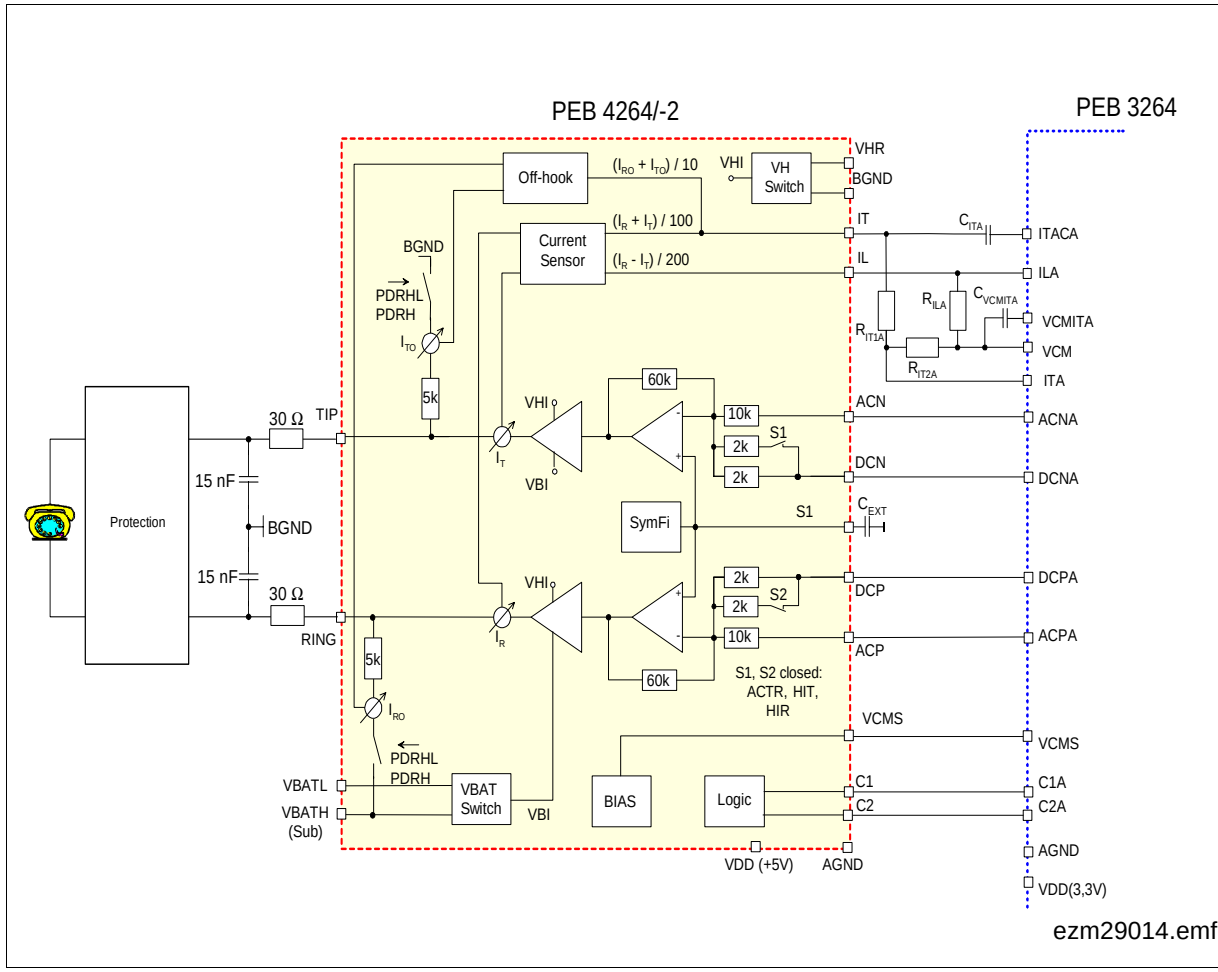



**Figure 6 Minimal Application Circuit**

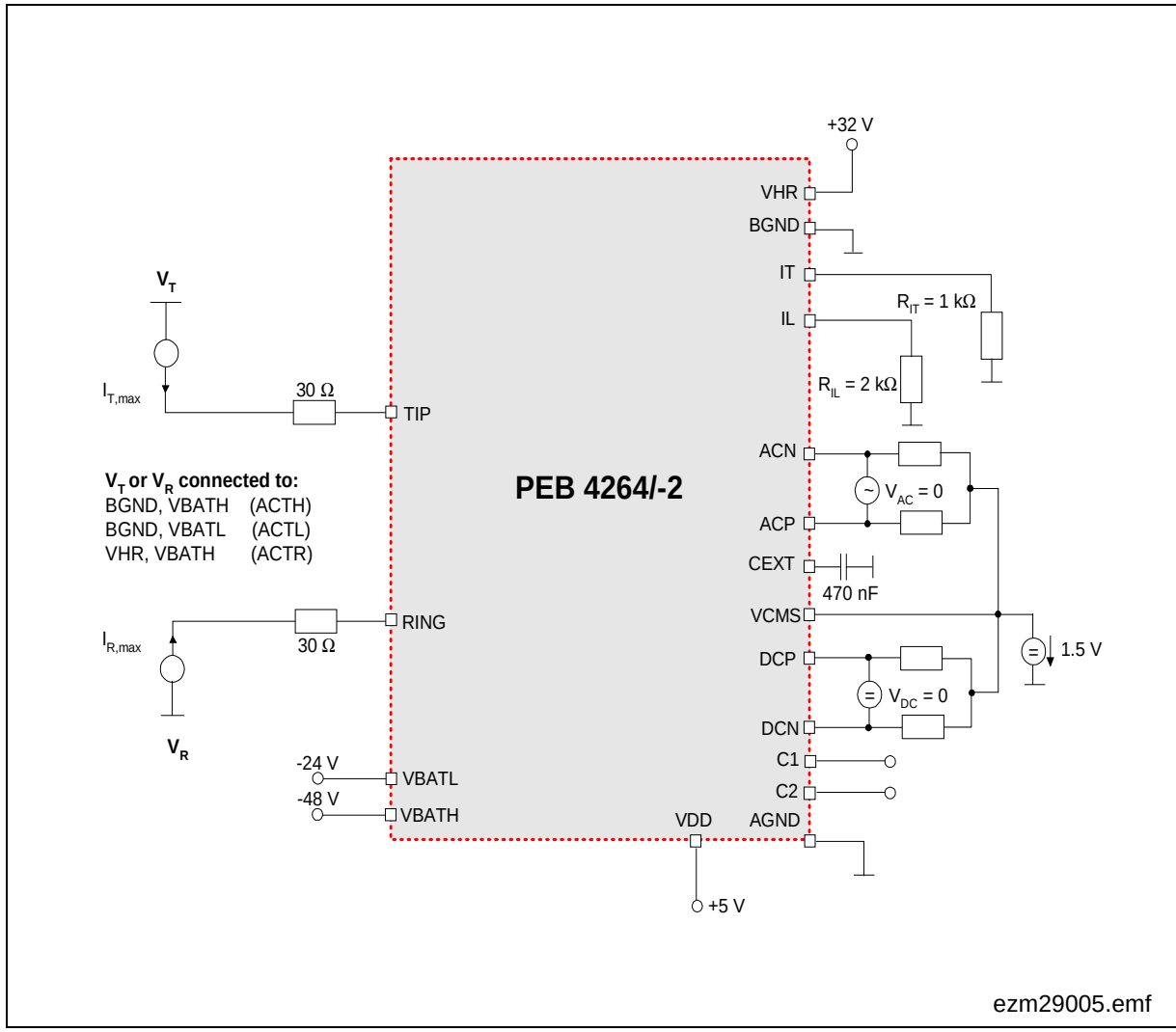



**Figure 7 Output Current Limit**

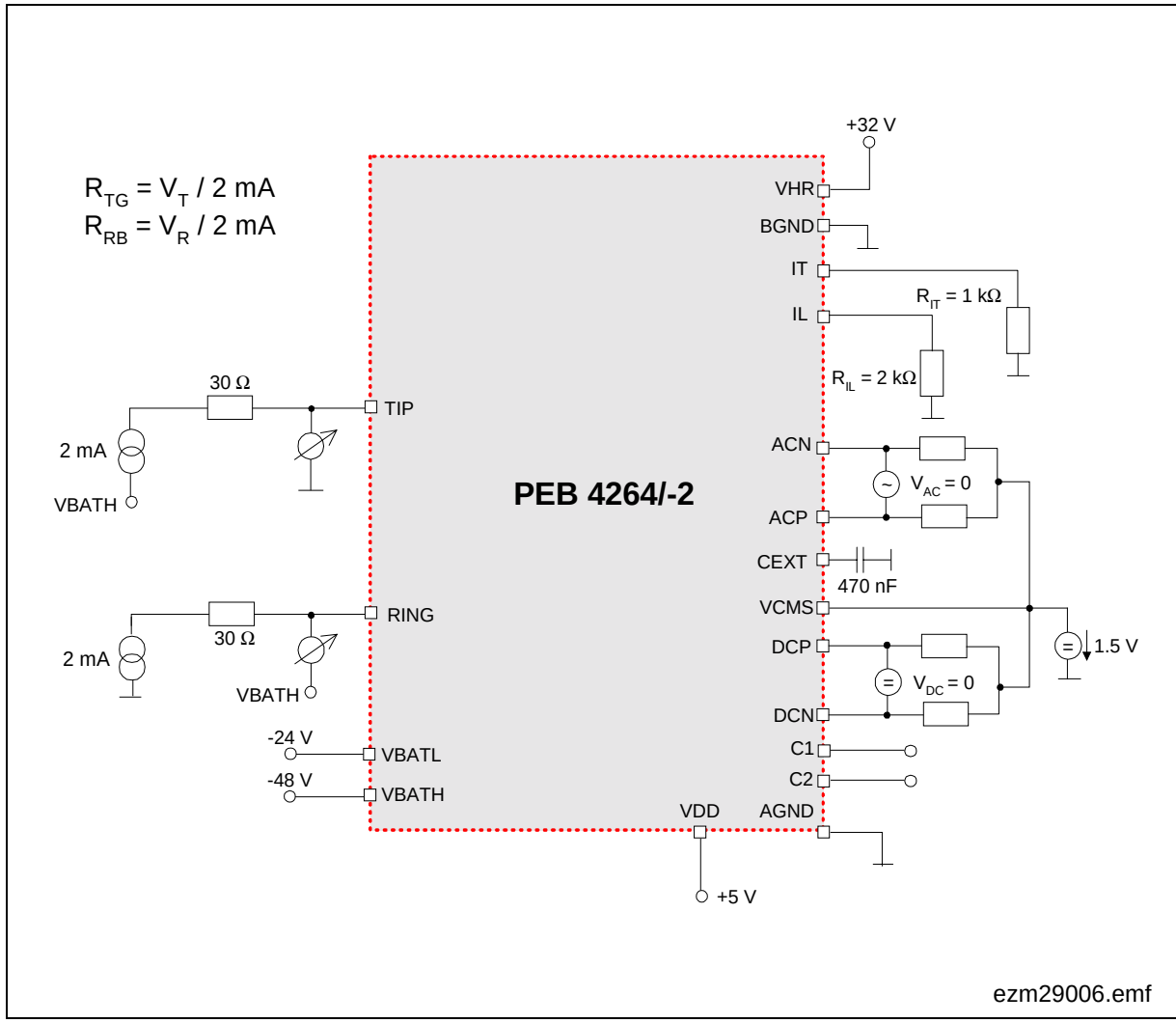



**Figure 8 Output Resistance PDRH, PDRHL**

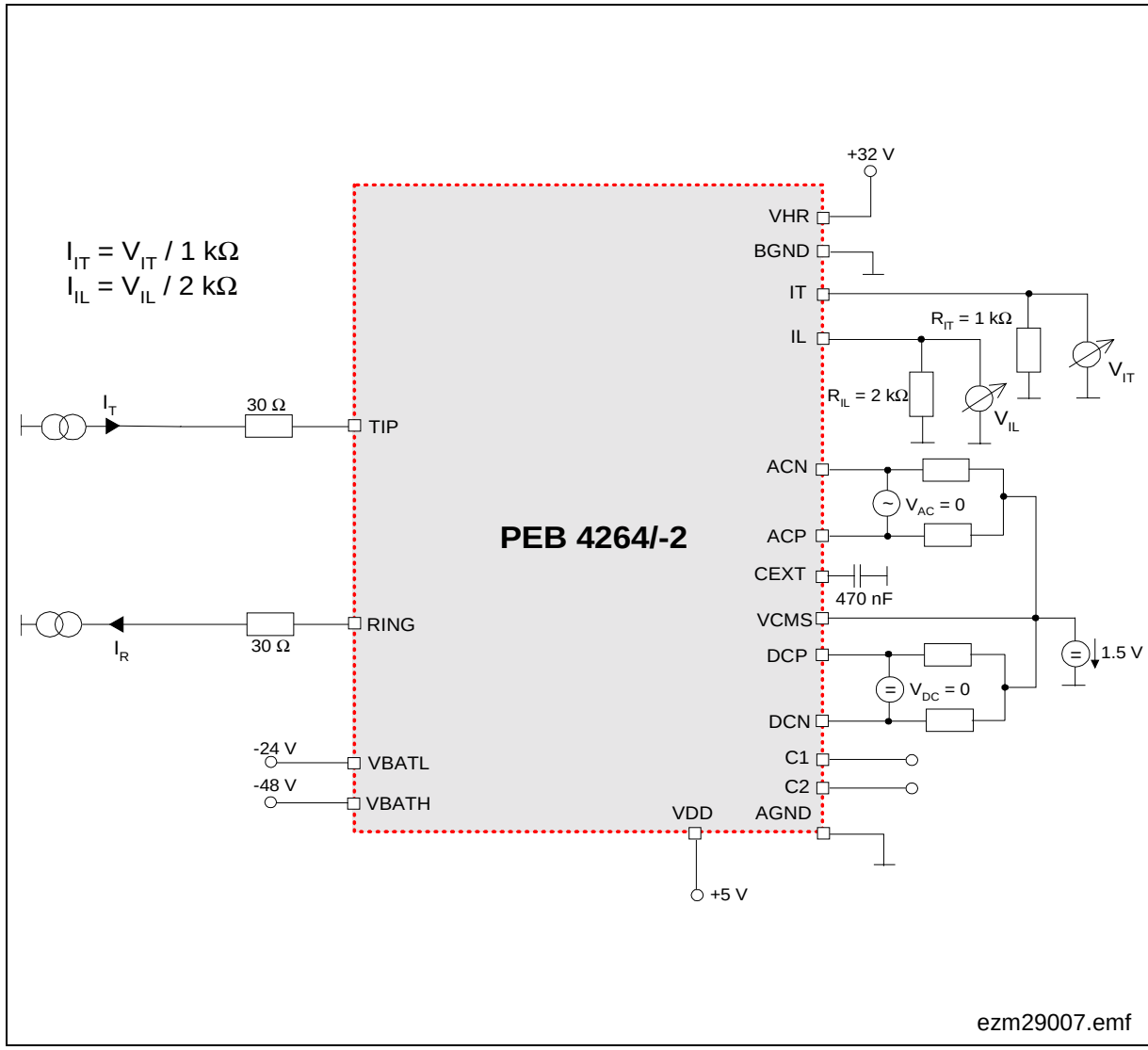



**Figure 9 Current Outputs IT, IL**

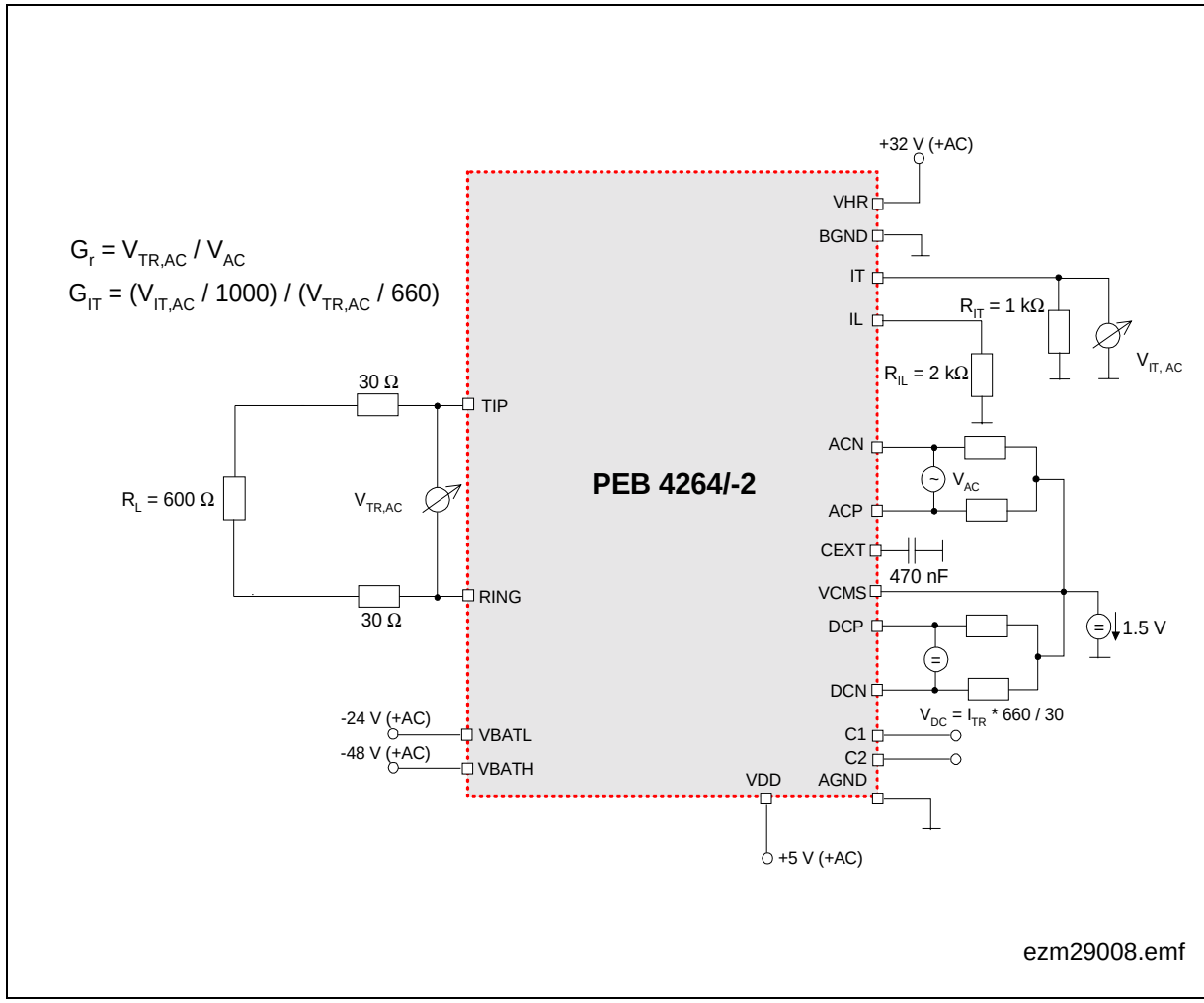



**Figure 10 Transmission Characteristics**

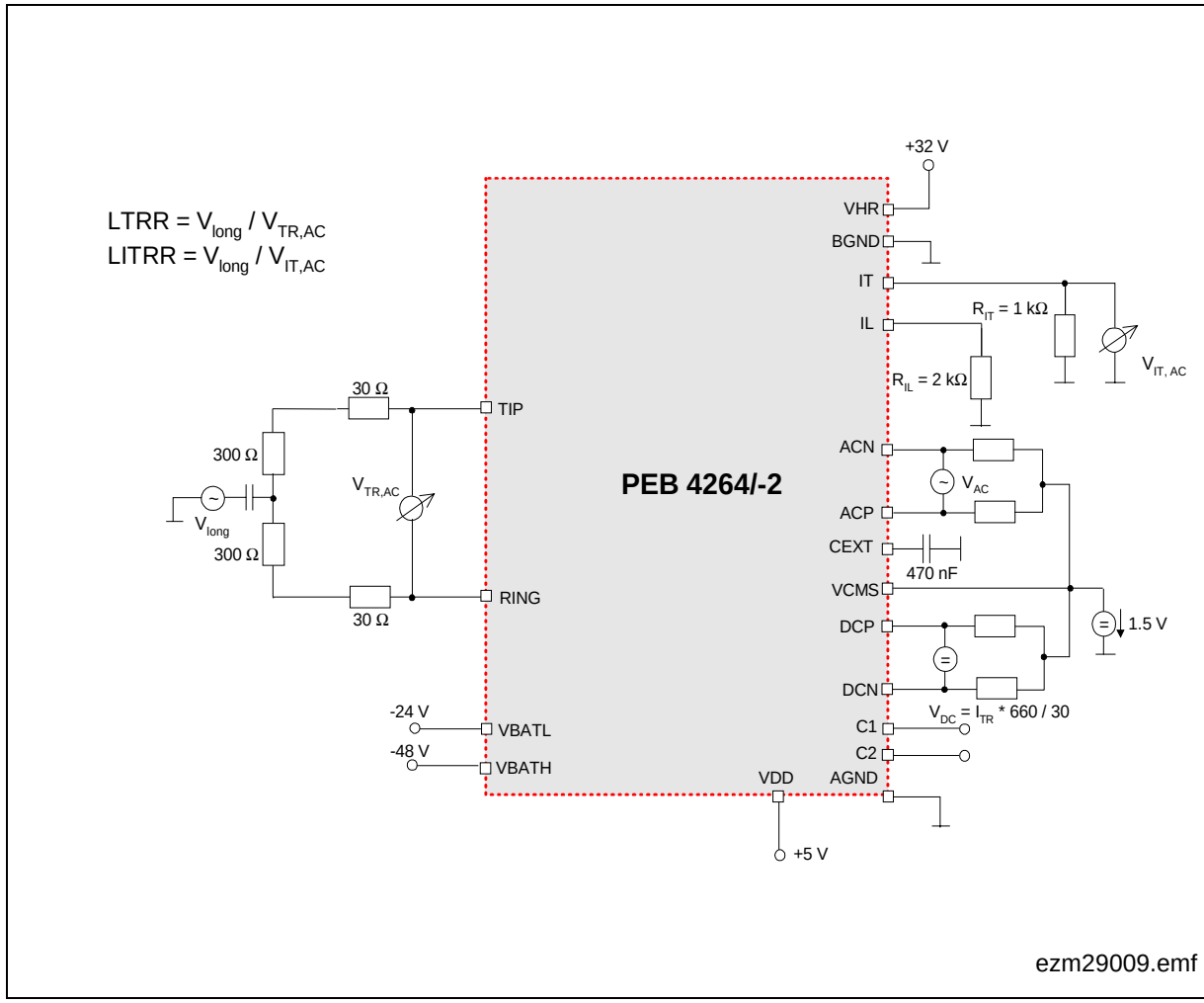



**Figure 11 Longitudinal to Transversal Rejection**

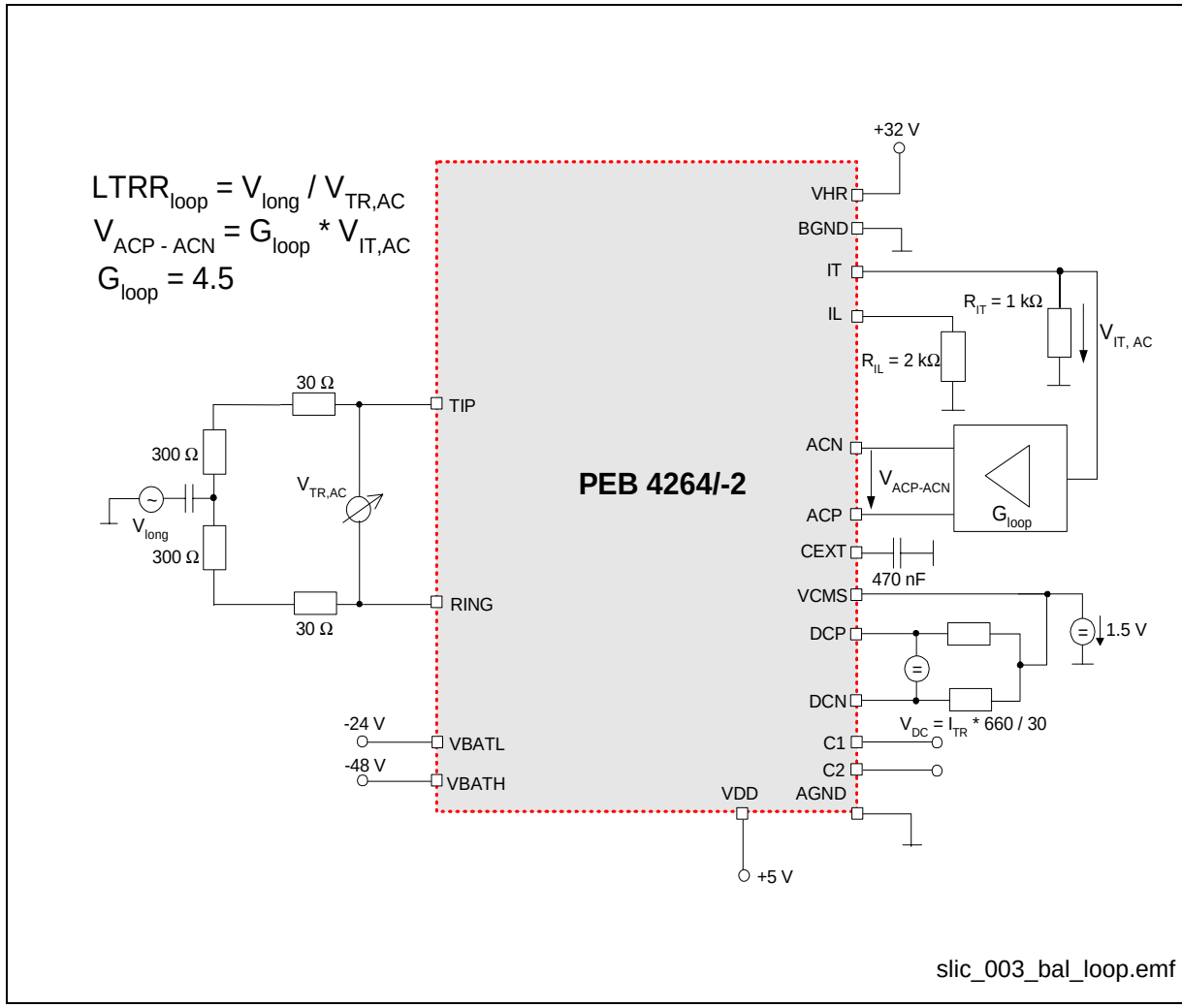



**Figure 12 Longitudinal to Transversal Rejection Loop**

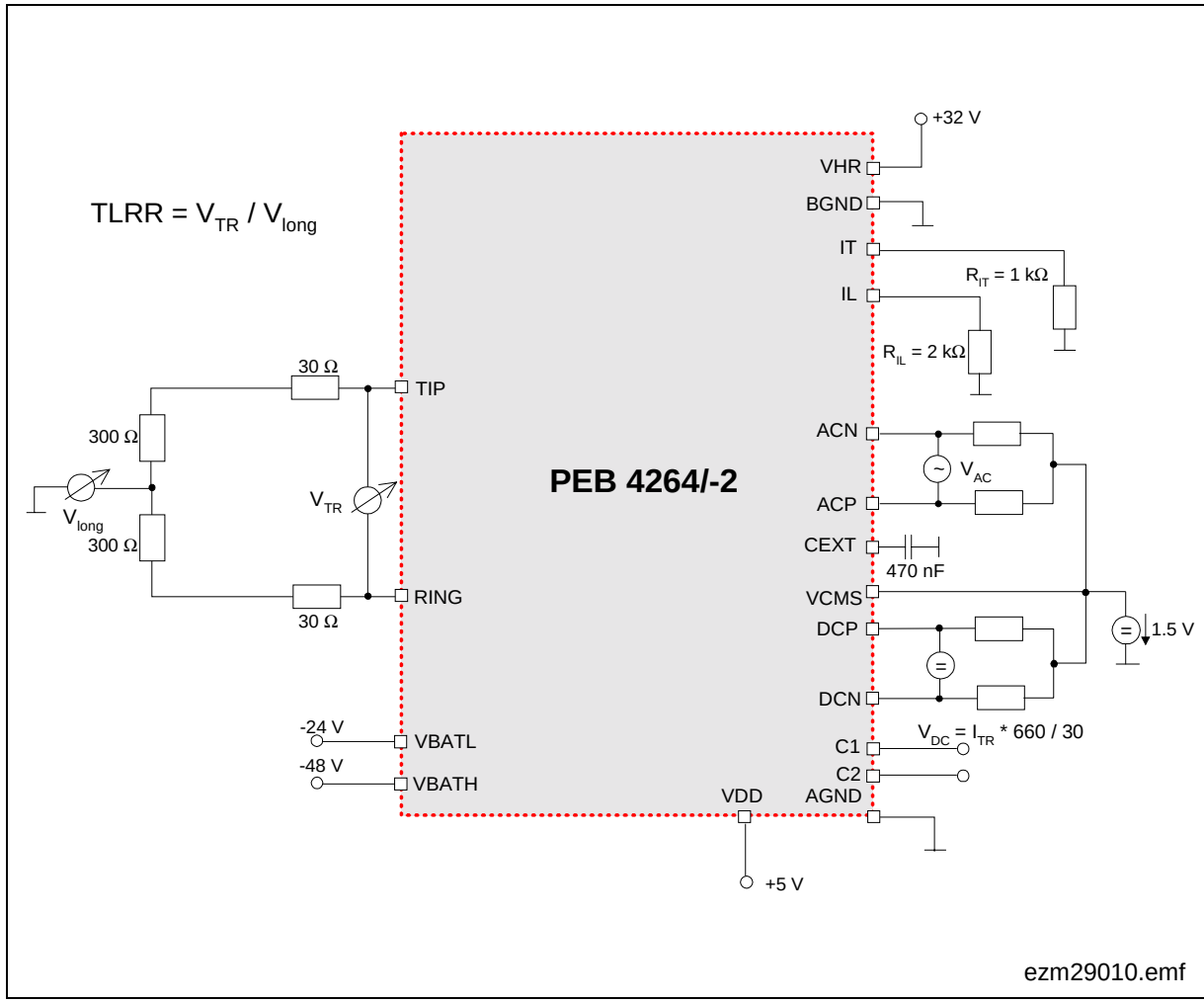



**Figure 13 Transversal to Longitudinal Rejection**

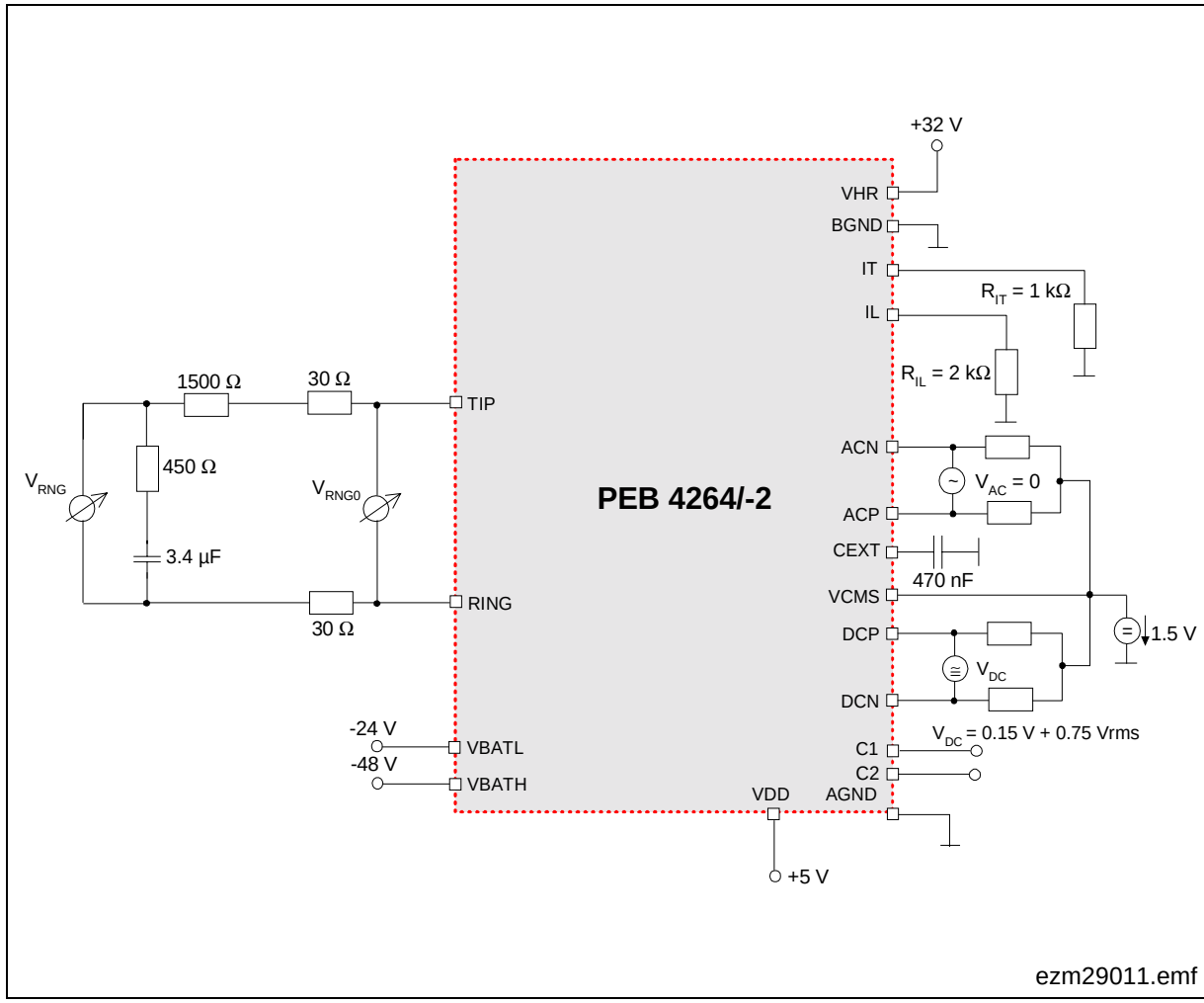
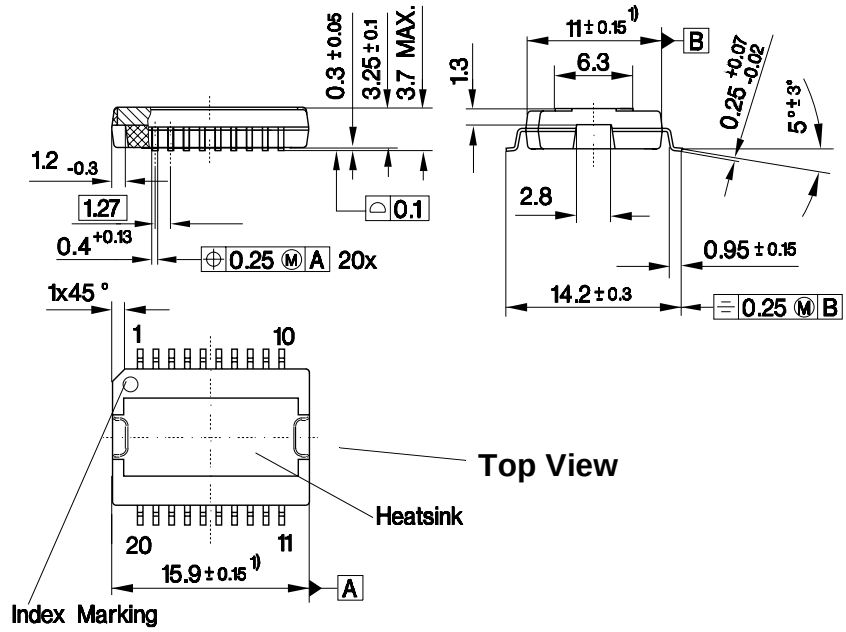



**Figure 14 Ring Amplitude**

# 5 Package Outlines

**P-DSO-20-5 (SLIC-S/-S2)**
(Plastic Dual Small Outline)




1) Does not include plastic or metal protrusion of 0.15 max. per side

gps05755.eps

*Note: The SLIC is only available in a P-DSO-20-5 package with heatsink on top. Please note that the pin counting for the P-DSO-20-5 package is clockwise (top view) in contrast to similar type packages which mostly count counterclockwise.*

**Sorts of Packing**
Package outlines for tubes, trays etc. are contained in our data book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

# Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

Published by Infineon Technologies AG