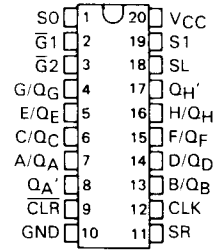
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

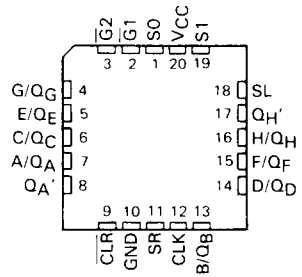
D2661, DECEMBER 1982—REVISED MAY 1986

- Multiplexed I/O Ports Provides Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS299 and AS299 Have Direct Overriding Clear
- 'ALS323 and AS323 Have Synchronous Clear
- Application:
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously on 'ALS299, 'AS299 and synchronously on 'ALS323, 'AS323 when $\overline{CLR}$ is low. Taking either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54' family is characterized for operation over the full military range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

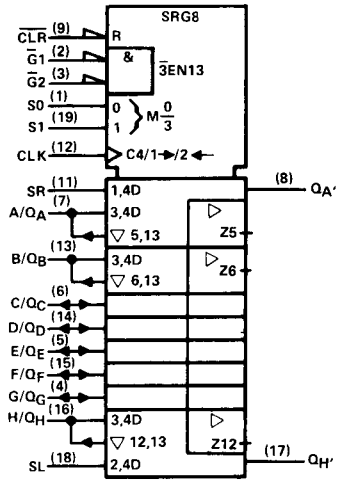
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	OUTPUT CONTROL $\overline{G1}$	OUTPUT CONTROL $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('ALS299)	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('AS299)	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('ALS323)	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('AS323)	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

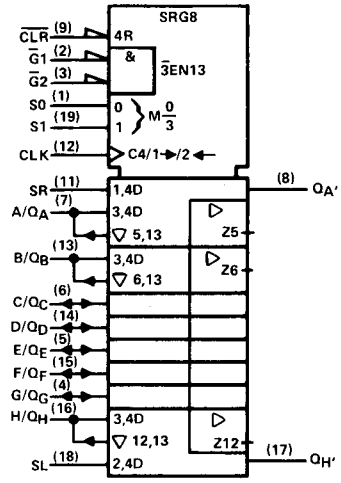
When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbols†

'ALS299, 'AS299



'ALS323, 'AS323



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

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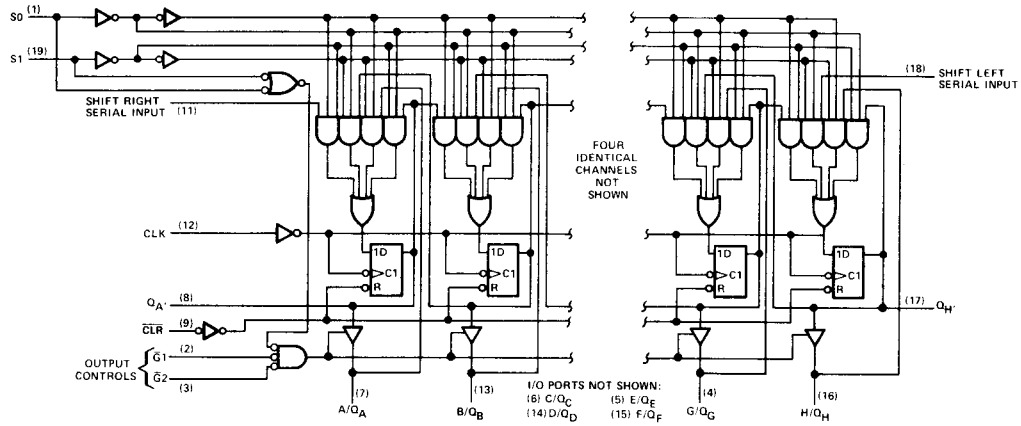
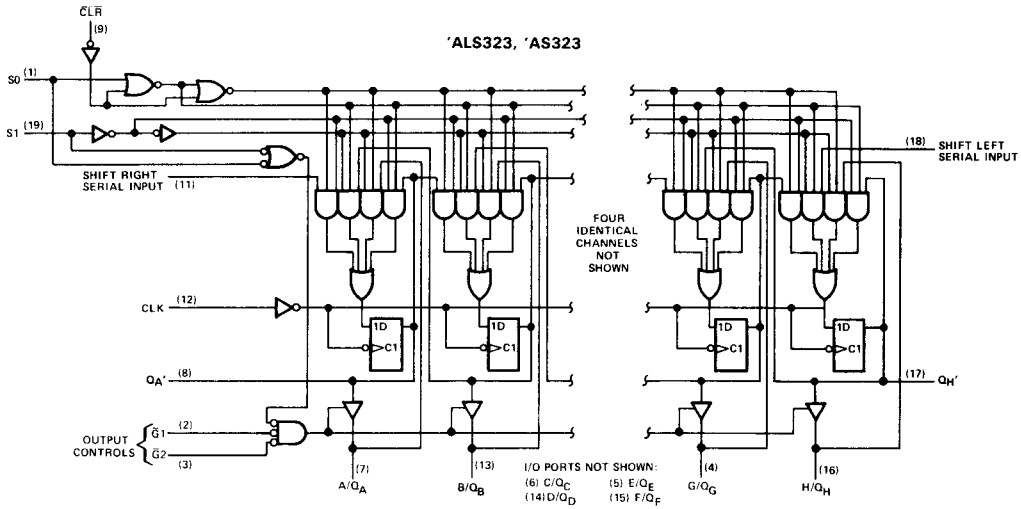
logic diagrams (positive logic)

'ALS299, 'AS299



'ALS323, 'AS323



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$				−0.4			−0.4	mA
		Q_A thru Q_H				−1			−2.6	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$				4			8	mA
		Q_A thru Q_H				12			24	
f_{clock}	Clock frequency (at 50% duty cycle)			0		17	0		30	MHz
t_w	Pulse duration	CLK high or low		22			16.5			ns
		$\overline{CLR}$ low ('ALS299)		12			10			
t_{su}	Setup time before CLK↑	Select		25			20			ns
		Serial or Parallel data	High level	18			16			
			Low level	15			6			
		$\overline{CLR}$ inactive ('ALS299)		15			15			
		$\overline{CLR}$ active ('ALS323)		25			20			
		$\overline{CLR}$ inactive ('ALS323)		18			16			
t_h	Hold time after CLK↑	Select		0			0			ns
		Serial or parallel data		0			0			
T_A	Operating free-air temperature			−55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}‡	S0, S1, SR, SL	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§	$Q_{A'}$, $Q_{H'}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q_A thru Q_H			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	28		15	28	mA
			Outputs low		22	38		22	38	
			Outputs disabled		23	40		23	40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS299 SN54ALS323		SN74ALS299 SN74ALS323		
			MIN	MAX	MIN	MAX	
f_{max}			17		30		MHz
t_{PLH}	CLK	Q_A thru Q_H	2	19	4	13	ns
t_{PHL}			4	25	7	19	
t_{PLH}	CLK	Q_A' or Q_H'	2	21	5	15	ns
t_{PHL}			4	22	8	18	
t_{PHL}	$\overline{CLR}$ ('ALS299 only)	Q_A thru Q_H	6	29	6	22	ns
		Q_A' or Q_H'	6	29	6	22	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	5	22	6	16	ns
t_{PZL}			6	26	8	22	
t_{PZH}	S0, S1	Q_A thru Q_H	5	21	7	17	ns
t_{PZL}			6	26	8	22	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	1	15	1	8	ns
t_{PLZ}			5	38	5	15	
t_{PHZ}	S0, S1	Q_A thru Q_H	1	16	1	12	ns
t_{PLZ}			8	34	8	25	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

				SN54AS299 SN54AS323			SN74AS299 SN74AS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current	Q_A' or Q_H'				−2			−2	mA
		Q_A thru Q_H				−12			−15	
I_{OL}	Low-level output current	Q_A' or Q_H'				20			20	mA
		Q_A thru Q_H				32			48	
f_{clock}	Clock frequency (at 50% duty cycle)									MHz
t_w	Pulse duration	CLK high or low								ns
		$\overline{CLR}$ low ('AS299)								
t_{su}	Setup time before CLK↑	Select								ns
		Serial or Parallel data	High level							
			Low level							
		$\overline{CLR}$ inactive ('AS299)								
		$\overline{CLR}$ active ('AS323)								
		$\overline{CLR}$ inactive ('AS323)								
t_h	Hold time after CLK↑	Select								ns
		Serial or parallel data								
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS299 SN54AS323			SN74AS299 SN74AS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}	Q_A' or Q_H'	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V							mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V							
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		95			95		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS299 SN54AS323			SN74AS299 SN74AS323			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CLK	Q_A thru Q_H		10			10		ns
t_{PHL}				10			10		
t_{PLH}	CLK	Q_A' or Q_H'		10			10		ns
t_{PHL}				10			10		
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H		12			12		ns
		Q_A' or Q_H'		12			12		
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H		10			10		ns
t_{PZL}				10			10		
t_{PZH}	S0, S1	Q_A thru Q_H		10			10		ns
t_{PZL}				10			10		
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H		7			7		ns
t_{PLZ}				7			7		
t_{PHZ}	S0, S1	Q_A thru Q_H		7			7		ns
t_{PLZ}				7			7		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits

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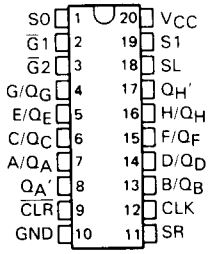
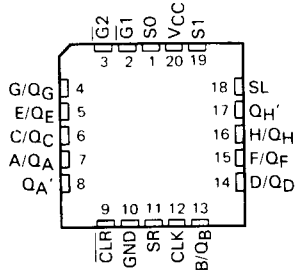


SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



For complete information on the SN54ALS323, SN54AS323, SN74ALS323, SN74AS323, see page 2-343.

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