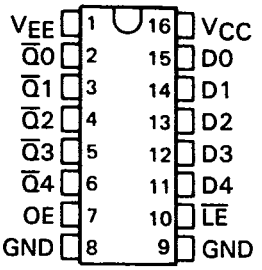
DP8481
TTL-TO-ECL (10K) LEVEL TRANSLATOR WITH LATCH

T-52-11

D3059, NOVEMBER 1987—REVISED APRIL 1988

- ECL Control Inputs
- 10K ECL Compatible
- Propagation Delay . . . 4 ns Typ
- Package Options Include Plastic "Small Outline" Package and Standard Plastic 300-mil DIPs
- Direct Replacement for National Semiconductor DP8481

D OR N PACKAGE
(TOP VIEW)



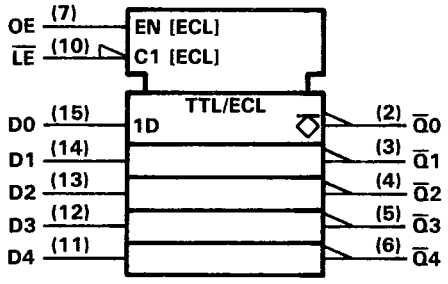
description

This circuit translates TTL input levels to ECL output levels and provides a 5-bit transparent latch. The outputs are gated by Output Enable (OE) and can be wire-OR connected. The Latch Enable ($\overline{LE}$) and OE inputs are ECL.

If Latch Enable ($\overline{LE}$) is low, the latches are transparent and the $\overline{Q}$ outputs follow the complement of the D inputs. If $\overline{LE}$ is high, the outputs are latched. If Output Enable (OE) is low, the outputs are forced to the low level.

The DP8481 is characterized for operation from 0°C to 75°C.

logic symbol†

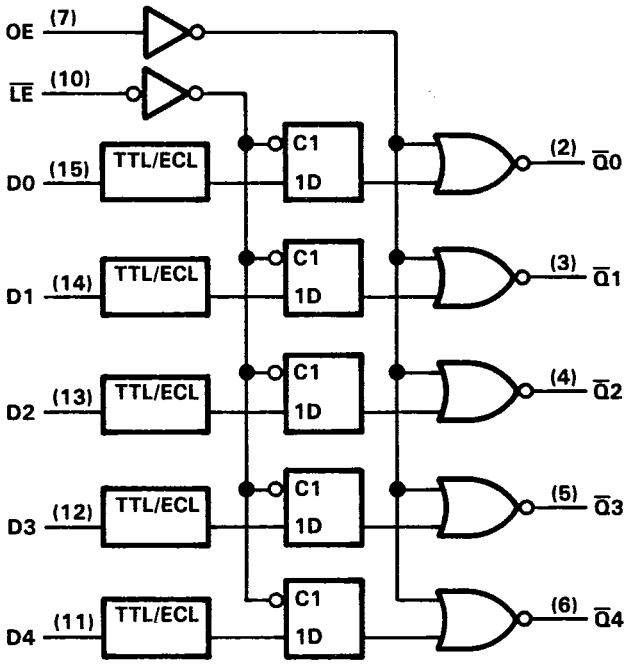


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH LATCH/TRANSLATOR)

OE	$\overline{LE}$	D	$\overline{Q}$
H	L	H	L
H	L	L	H
H	H	X	Q_0
L	X	X	L

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Supply voltage, V_{EE} . . . . . −8 V
Input voltage, V_I: OE or $\overline{LE}$ input . . . . . 0 V to V_{EE}
D inputs . . . . . −1 V to 5.5 V
Output current, I_O . . . . . −50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 75°C$ POWER RATING
D	950 mW	7.6 mW/°C	570 mW
N	1150 mW	9.2 mW/°C	690 mW

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{EE}		−4.68	−5.20	−5.72	V
High-level input voltage, V_{IH} (TTL-level D inputs)		2			V
Low-level input voltage, V_{IL} (TTL-level D inputs)				0.8	V
High-level input voltage, V_{IH} (ECL-level OE and $\overline{LE}$ inputs) (see Note 1)	T_A = 0°C	−1145		−840	mV
	T_A = 25°C	−1105		−810	
	T_A = 75°C	−1045		−720	
Low-level input voltage, V_{IL} (ECL-level OE and $\overline{LE}$ Inputs) (see Note 1)	T_A = 0°C	−1870		−1490	mV
	T_A = 25°C	−1850		−1475	
	T_A = 75°C	−1830		−1450	
Pulse duration, $\overline{LE}$ low, t_w		5			ns
Setup time, t_{su}	Data before $\overline{LE}$↓	5			ns
	Data before OE↓ (see Note 2)	5.5			
Hold time, data after $\overline{LE}$↓, t_h		1			ns
Operating free-air temperature, T_A		0		75	°C

NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.
2. This setup time applies when operating in the transparent mode ($\overline{LE}$ is low) and it is necessary that valid data be available at the output immediately after the outputs are enabled.

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electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D0-D4	I_I = −12 mA		−0.8	−1.2	V
I_{IH}	High-level input current	D0-D4	V_I = 2.5 V		1	40	μA
		OE, $\overline{LE}$	V_I = −0.8 V			200	
I_{IL}	Low-level input current	D0-D4	V_I = 0.5 V		−50	−200	μA
		OE,$\overline{LE}$	V_I = −1.8 V			150	
V_{OH}	High-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C	−1000		−840	mV
			V_{EE} = −5.2 V, T_A = 25°C	−960		−810	
			V_{EE} = −5.2 V, T_A = 75°C	−900		−720	
V_{OHC}	Critical high-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C	−1020			mV
			V_{EE} = −5.2 V, T_A = 25°C	−980			
			V_{EE} = −5.2 V, T_A = 75°C	−920			
V_{OL}	Low-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C	−1870		−1665	mV
			V_{EE} = −5.2 V, T_A = 25°C	−1850		−1650	
			V_{EE} = −5.2 V, T_A = 75°C	−1830		−1625	
V_{OLC}	Critical low-level output voltage (see Notes 1 and 3)		V_{EE} = −5.2 V, T_A = 0°C			−1645	mV
			V_{EE} = −5.2 V, T_A = 25°C			−1630	
			V_{EE} = −5.2 V, T_A = 75°C			−1605	
I_{CC}	Supply current from V_{CC}		V_{CC} = 5.5 V			20	mA
I_{EE}	Supply current from V_{EE}		V_{EE} = −5.7 V			−90	mA

†Typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated one minimum, is used in this data sheet for logic levels only.

3. V_{OH} and V_{OL} are tested using the "outer-limit" values V_{IH} max and V_{IL} min. The "critical" values V_{OHC} and V_{OLC} are tested using the "inner-limit" values V_{IH} min and V_{IL} max. The latter values ensure the noise margins of 155 mV high and 125 mV low associated with 10K ECL.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output from $\overline{LE}$ input	R_L = 50 Ω to −2 V	1.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{LE}$ input		1.5	4	6	ns
t_{PLH}	Propagation delay time, low-to-high-level output from D input		2.5	4	7.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output from D input		2.5	4	7.5	ns
t_{en}	Output enable time from OE input		1	3	4	ns
t_{dis}	Output disable time from OE input		1	3	4	ns

†Typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

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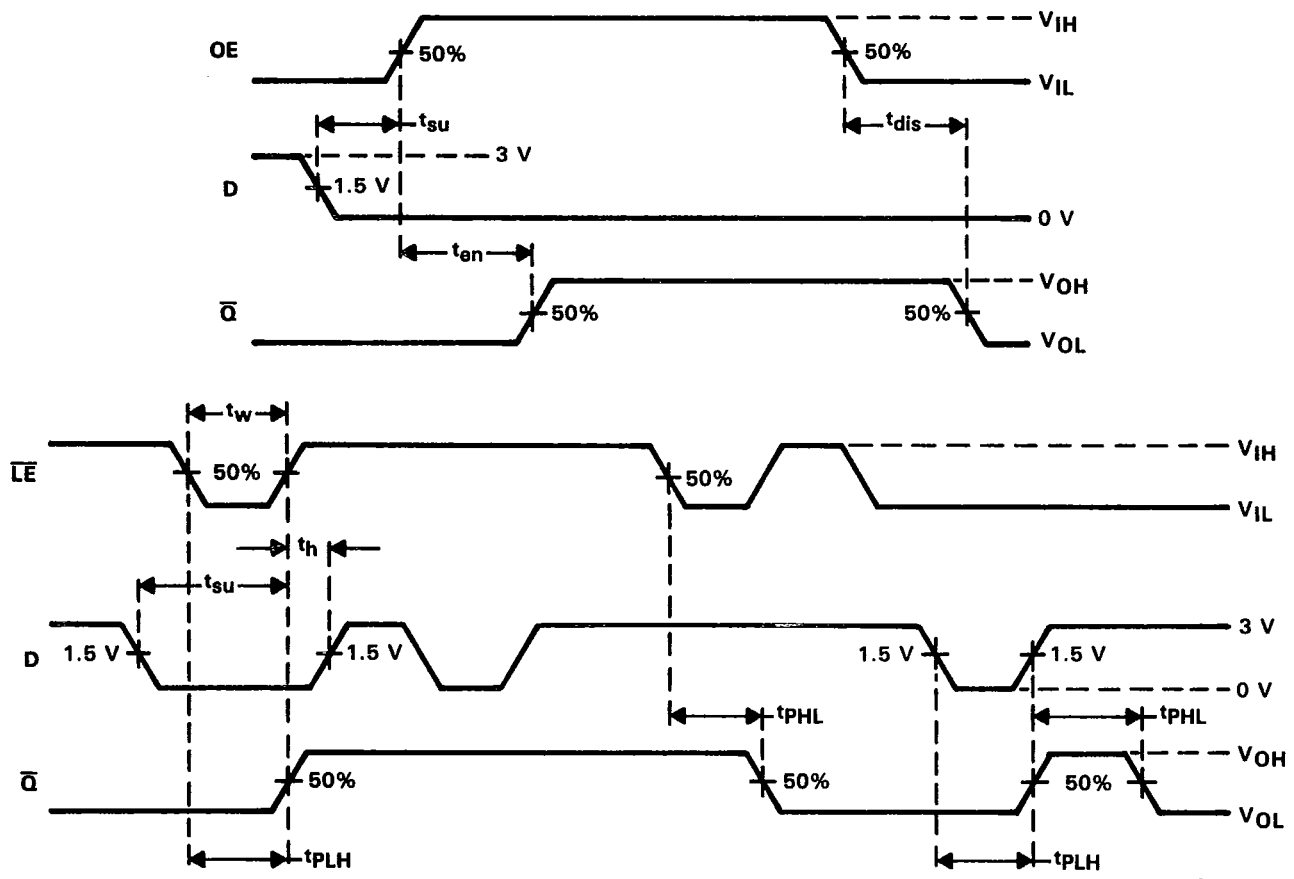
PARAMETER MEASUREMENT INFORMATION



NOTE A: ECL input rise and fall times at OE and $\overline{LE}$ are 2 ns ±0.2 ns from 20% to 80%. TTL input rise and fall times at D inputs are 3 ns maximum measured between 10% and 90%.

FIGURE 1. SWITCHING TIME WAVEFORMS

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