4582B
CARRY LOOKAHEAD GENERATOR

OBSOLETE

DESCRIPTION — The 4582B is a Carry Lookahead Generator which provides high speed lookahead over word lengths of more than four bits. The device has a Carry Input ($\overline{C_n}$), four active LOW Carry Generate Inputs ($\overline{G_0}$-$\overline{G_3}$), four active LOW Carry Propagate Inputs ($\overline{P_0}$-$\overline{P_3}$), three Carry Outputs (C_{n+x},C_{n+y},C_{n+z}), an active LOW Carry Propagate Output ($\overline{P}$) and an active LOW Carry Generate Output ($\overline{G}$). The logic equations for all outputs are shown below.

- **EXPANDABLE TO ANY NUMBER OF BITS**
- **HIGH SPEED LOOKAHEAD OVER WORD LENGTHS OF MORE THAN FOUR BITS**

PIN NAMES

$\overline{C_n}$	Carry Input
$\overline{G_0}$-$\overline{G_3}$	Carry Generate Inputs (Active LOW)
$\overline{P_0}$-$\overline{P_3}$	Carry Propagate Inputs (Active LOW)
C_{n+x},C_{n+y},C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

LOGIC EQUATIONS

$$C_{n+x} = G_0 + P_0 \cdot C_n$$

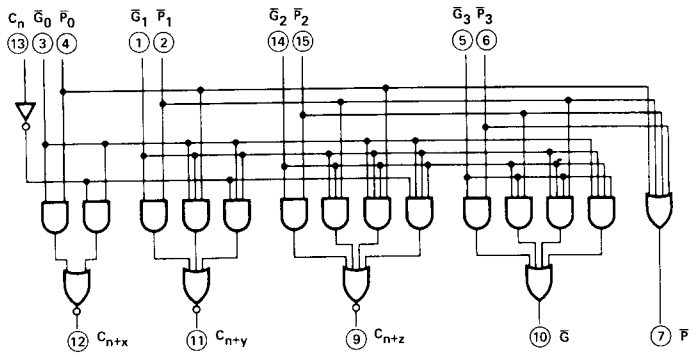
$$C_{n+y} = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_n$$

$$C_{n+z} = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_n$$

$$\overline{G} = \overline{G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0}$$

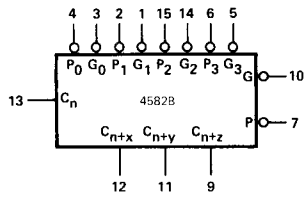
$$\overline{P} = \overline{P_3 \cdot P_2 \cdot P_1 \cdot P_0}$$

LOGIC DIAGRAM



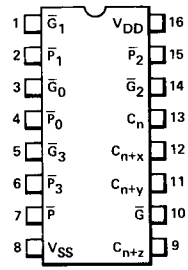
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

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TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, C_n to C_{n+x},		160			75			55		ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}	C_{n+y} or C_{n+z}		160			75			55			
t_{PLH}	Propagation Delay, $\overline{P}_n$ to C_{n+x}		160			75			55		ns	
t_{PHL}	C_{n+y} or C_{n+z}		160			75			55			
t_{PLH}	Propagation Delay, $\overline{G}_n$ to C_{n+x},		160			75			55		ns	
t_{PHL}	C_{n+y} or C_{n+z}		160			75			55			
t_{PLH}	Propagation Delay, $\overline{P}_n$ to $\overline{G}$		160			75			55		ns	
t_{PHL}	to $\overline{G}$		160			75			55			
t_{PLH}	Propagation Delay, $\overline{G}_n$ to $\overline{G}$		160			75			55		ns	
t_{PHL}			160			75			55			
t_{PLH}	Propagation Delay, $\overline{P}_n$ to $\overline{P}$		160			75			55		ns	
t_{PHL}			160			75			55			
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20			

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

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