ECL to TTL Translator (+ 5.0 Vdc Power Supply)

ELECTRICALLY TESTED PER:
MPG 10H750

The 10H750 is a member of Motorola's 10H family of high performance ECL logic. It consists of 4 translator with differential inputs and TTL outputs. The 3-state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

The 10H750 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the 10H750 to be used as an inverting or non-inverting translator, a differential line receiver or as a high performance comparator.

- Propagation Delay, 3.5 ns Typical
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
ECL V_{CC}	1	5	2	V_{CC}
A_{OUT}	2	6	3	GND
A_{IN}	3	7	4	V_{CC}
$\overline{A_{IN}}$	4	8	5	GND
$\overline{B_{IN}}$	5	9	7	GND
B_{IN}	6	10	8	V_{CC}
B_{OUT}	7	11	9	GND
GND	8	12	10	GND
$\overline{OE}$	9	13	12	GND
D_{OUT}	10	14	13	GND
D_{IN}	11	15	14	V_{CC}
$\overline{D_{IN}}$	12	16	15	GND
$\overline{C_{IN}}$	13	1	17	GND
C_{IN}	14	2	18	V_{CC}
C_{OUT}	15	3	19	GND
TTL V_{CC}	16	4	20	V_{CC}

BURN - IN CONDITIONS:
V_{CC} = + 6.0 V MAX/ + 5.0 V MIN

Military 10H750

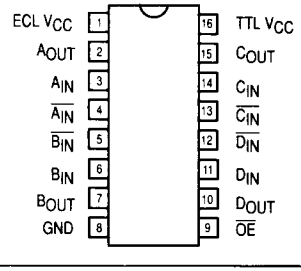
2

AVAILABLE AS

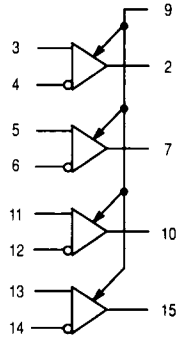
1) JAN: N/A
2) SMD: N/A
3) 883: 10H750/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



V_{CC} (+ 5.0 V) = Pins 1, and 16
GND = Pin 8

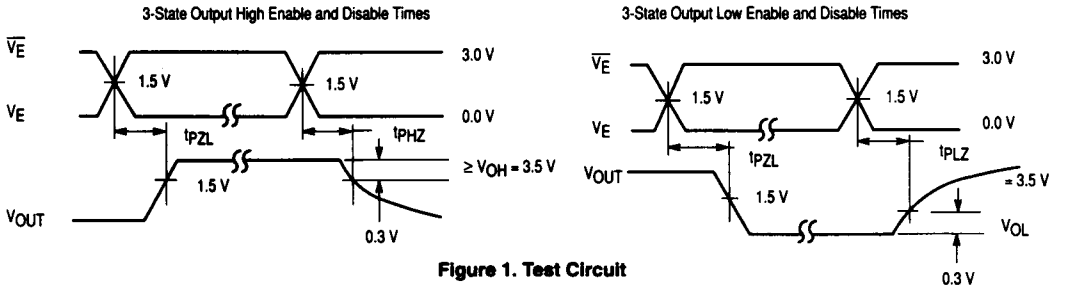


Figure 1. Test Circuit

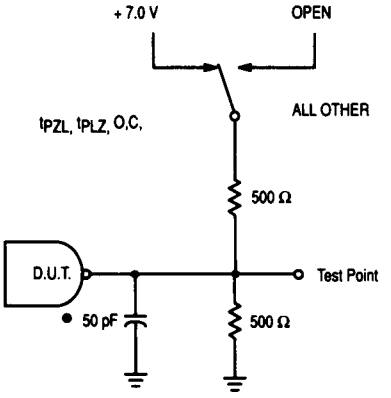


Figure 2. Test Load

• INCLUDES JIG AND PROBE CAPACITANCE
Application Note: Pin 9 is an $\overline{OE}$ and the 10H750 is disabled when $\overline{OE}$ is at V_{IH} or higher

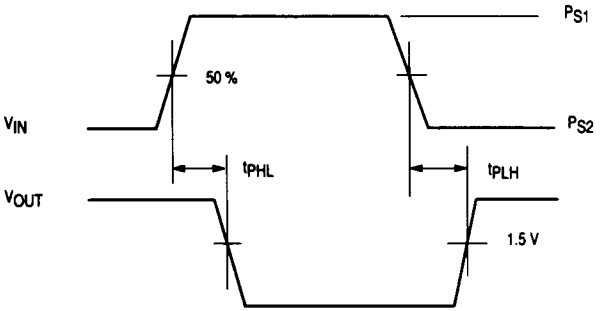


Figure 3. Inverting Waveform Functions

10H750
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts) (V_{DIFF} in millivolts)															Test Current (milliAmps)	
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{CC1}	V_{CC2}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_R	$V_{comm.mode}$	V_{DIFF}	I_{OH}	I_{OL}
T_A = 25 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.11	+3.31	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.71	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20
T_A = 125 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.22	+3.345	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.82	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20
T_A = 55 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.03	+3.285	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.63	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments $V_{CC1\ \&\ 2}$ = (Pin 1, 16), GND = (Pin 8), Output Load = See Figure 1.									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IHH}	V_{IHL}	V_{IL}	V_{ILL}	V_{ILH}	V_{CC2}	V_{CC1}	$I_{OH/L}$	P. U. T.
V_{OH}	High Output Voltage	2.5		2.5		2.5		V	3, 6 11, 14	3, 6 11, 14	3, 6 11, 14	4, 5 12, 13	4, 5 12, 13	4, 5 12, 13	1, 16	1, 16	2, 7 10, 15	2, 7 10, 15
V_{OL}	Low Output Voltage		0.5		0.5		0.5	V	2, 3	2	2	3		3	3	8	4	4, 5 12, 13
I_{OZH} I_{OZL}	Output Disable Current (High/ Low)	+ 50 –50		+ 50 –50		+ 50 –50		mA mA	2, 7 10, 15			2, 7 10, 15				1, 16		2, 7 10, 15
I_{CC1} I_{CC2}	Power Supply Current (TTL/ ECL)		20 12		20 12		20 12	mA mA		4, 5 12, 13		9		3, 6 11, 14		1, 16		1, 16
I_{CC}	Input Leakage Current		32		32		32	mA		4, 5 12, 13		9		3, 6 11, 14		1, 16		1, 16
I_{OS}	Short Circuit (**) Current	–60	–150	–60	–150	–60	–150	mA	3, 6 11, 14			4, 5, 9 12, 13				1, 16		2, 7 10, 15
I_{IH}	Input Current		20		20		20	µA	9							1, 16		9
I_{INH}	Input Current		50		50		50	µA		3 – 6 11 – 14				3, 6 11, 14		1, 16		3 – 6 11 – 14
I_{IL}	Input Current		– 0.6		– 0.6		– 0.6	µA				9				1, 16		9
I_{INL}	Input Current		50		50		50	µA		3 – 6 11 – 14				3, 6 11, 14		1, 16		3 – 6 11 – 14

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts. ** For I_{OS}: Pins 2, 7, 10, 15 = GND

10H750
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T_A = 125 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.22	+3.345	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.82	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20
T_A = – 55 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.03	+3.285	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.63	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{out}	V_{CC}	V_R	P_{S1}	P_{S2}	P.U.T.
t_{pd}	Propagation Delay Data	1.5	5.0	1.5	5.2	1.5	5.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdHZ}	Outside Disable Time	2.0	6.0	2.0	6.2	2.0	6.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdHZ}	Outside Disable Time	2.0	6.0	2.0	6.2	2.0	6.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdZL}	Output Enable Time	2.0	8.0	2.0	8.2	2.0	8.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdZH}	Output Enable Time	2.0	8.0	2.0	8.2	2.0	8.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15

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Note

Subgroups A10 and A11, (AC testing) at –55°C and +125°C guaranteed, but not tested.