

T7035 Clock Recovery and Data Retiming Circuit

Features

- Clock recovery and data retiming
- Pin-programmable for 50.5 MHz to 237 MHz operation
- 100K ECL compatible I/O
- Fiber and wire applications
- Nonpeaking jitter transfer
- Single 5 V supply
- Extended temperature range available: -40 °C to +85 °C
- Single external component required: 3.579545 MHz crystal

Description

The AT&T T7035 Clock Recovery Circuit operates over a 50.5 MHz to 237 MHz frequency range. Using a single plus or minus 5 V supply, the circuit provides clock recovery and data retiming. The device accepts NRZ data, recovers the clock, and retimes the data to the recovered clock. The differential input and outputs are 100K ECL compatible. The T7035 Clock Recovery Circuit is manufactured by using 0.9 μm CMOS technology and is available in a 44-pin, plastic, leaded chip carrier (PLCC) package.

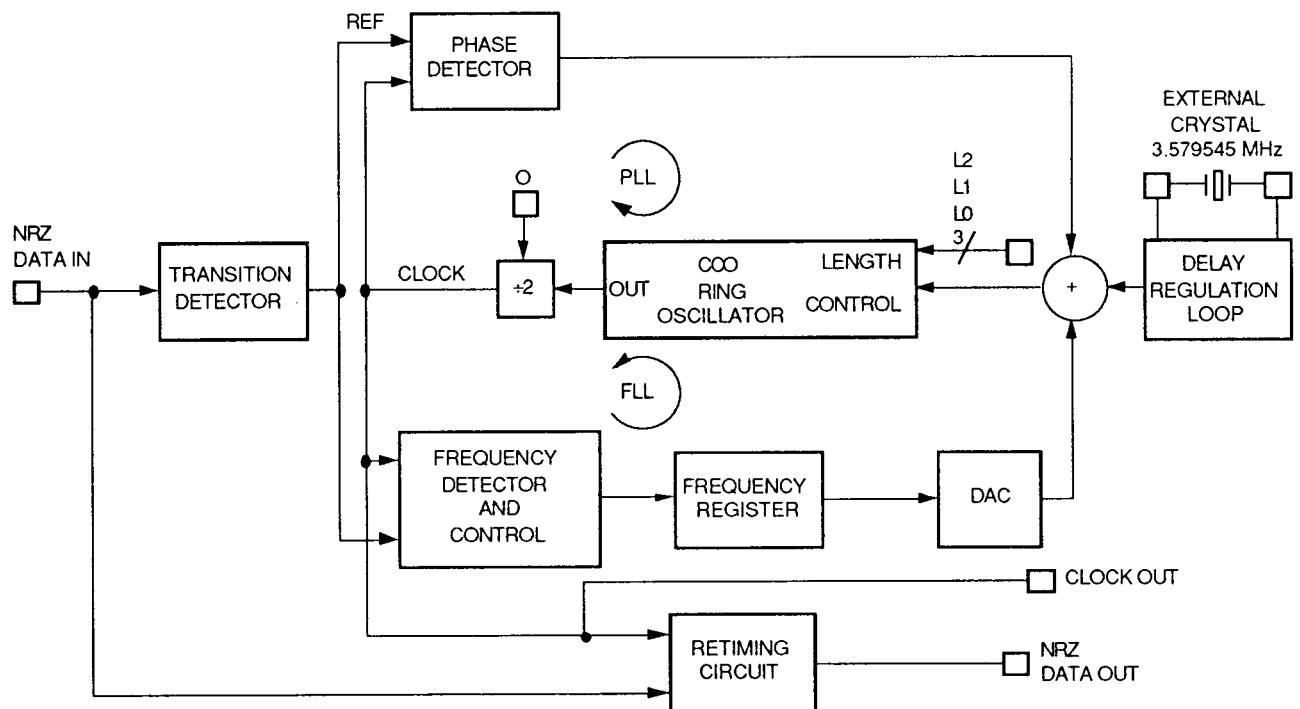


Figure 1. Block Diagram

T7035 Clock Recovery and Data Retiming Circuit

Description (continued)

The overall circuit architecture includes a phase- and frequency-locked loop to extract the clock from the input data, a regulation circuit to control the effects of variations in operating conditions and silicon processing, and a retiming circuit to synchronize clock and data outputs. At the core is a low-gain, phase-locked loop (PLL) that is composed of a phase detector, a variable length current-controlled oscillator (CCO), and a frequency divider circuit. The CCO can be changed by varying the number of stages and the current drive per stage.

The delay regulation loop (DRL) tracks a reference frequency of 3.579545 MHz (unrelated to the bit rate of the input data) to compensate and stabilize all on-chip oscillators and delay chains against variations in temperature, power supply, and silicon manufacturing. The low-gain PLL by itself can capture and lock only within a narrow range of the free-running frequency of the

CCO. To accommodate this, several frequency setting techniques are used to allow the PLL to lock on to any frequency from 50.5 MHz to 237 MHz. For fast frequency convergence, a frequency-locked loop (FLL) composed of a frequency detector and control circuit, a frequency register, and a digital-to-analog converter (DAC) is used to extend the capture range to 10%. The range of the clock recovery is extended beyond that achievable with the FLL alone by programming (setting pins high or low) five parameters: L0, L1, L2, O, and N. The L parameters set the length of the ring oscillator CCO, N controls the multiple of 3.579545 MHz to which the DRL frequency is divided, and O selects the high or low octave. Finally, the retiming circuit ensures that the clock strobe appears in the center of the data eye.

Pin Information

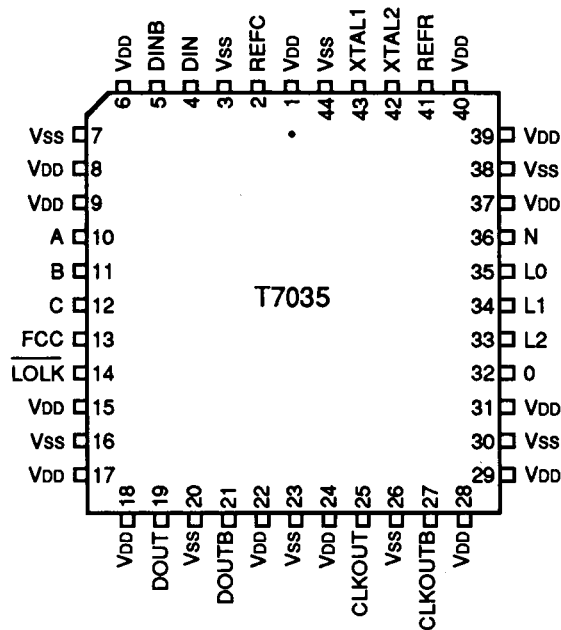


Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Description
1, 6, 8, 9, 15, 17, 18, 22, 24, 28, 29, 31, 37, 39, 40	V _{DD}	PWR	High Power Supply*.
3, 7, 16, 20, 23, 26, 30, 38, 44	V _{SS}	PWR	Low Power Supply*.
2	REFC	I	Reference Clock Input (LSTTL). When using the REFC input as the frequency reference, tie XTAL1 to V _{SS} and leave XTAL2 unconnected. REFC can be used when several T7035 devices are driven from a single frequency reference source. When a crystal is used, REFC should be tied to V _{SS} .
4	DIN	I	Data Input (ECL).
5	DINB	I	Data Input Complement (ECL).
10, 11, 12	A, B, C	I	A, B, and C. These pins must be tied to V _{SS} for normal operation.
13	FFC	I	Freeze Frequency Control (LSTTL). FFC should be tied low for normal operation. When this pin is high, the operating frequency of the output clock is held constant.
14	LOLK	O	Loss of Lock Output Pin (LSTTL). The LOLK pin is low when the clock recovery circuit has attained phase/frequency lock.
19	DOUT	O	Data Output (ECL). For optimum performance, the differential outputs DOUT and DOUTB must have equal loading.
21	DOUTB	O	Data Output Complement (ECL). For optimum performance, the differential outputs DOUT and DOUTB must have equal loading.
25	CLKOUT	O	Clock Output (ECL). For optimum performance, the differential outputs CLKOUT and CLKOUTB must have equal loading.
27	CLKOUTB	O	Clock Output Complement (ECL). For optimum performance, the differential outputs CLKOUT and CLKOUTB must have equal loading.
32	O	I	Frequency Select Pin (LSTTL). Frequency select pin sets the operating frequency range. See Table 2.
33, 34, 35	L2, L1, L0	I	Frequency Select Pins (LSTTL). Frequency select pins set the operating frequency range. See Table 2.
36	N	I	Frequency Select Pin (LSTTL). Frequency select pin sets the operating frequency range. See Table 2.
41	REFR	O	ECL Reference Resistor. The ECL reference resistor REFR should be tied to the ECL termination voltage ($V_{TT} = V_{DD} - 2\text{ V}$) through a resistor which has a value $10(R_{TT})$, where R_{TT} is the terminating impedance of the ECL outputs (e.g., if $R_{TT} = 50\ \Omega$, REFR should be tied to V_{TT} through a 500 Ω resistor). Both R_{TT} and REFR resistors should not exceed 5.0% tolerance.
42	XTAL2	I	Reference Crystal Input (XTAL). When using the on-chip crystal oscillator as the frequency reference, connect a 3.579545 MHz crystal between XTAL1 and XTAL2. Tie REFC to V _{SS} . If an external reference clock is applied to REFC, leave XTAL2 unconnected. An example XTAL is Digikey X079 3.579545 MHz.
43	XTAL1	I	Reference Crystal Input (XTAL). When using the on-chip crystal oscillator as the frequency reference, connect a 3.579545 MHz crystal between XTAL1 and XTAL2. Tie REFC to V _{SS} . If an external reference clock is applied to REFC, tie XTAL1 to V _{SS} .

* A circuit board ground plane is required for optimum performance. If high power supply is +5 V, then the high power supply should be bypassed to the low supply (ground) with low-inductance 0.01 μF and 0.1 μF capacitors (see Figure 8B). If low power supply is -5 V, then the low power supply should be bypassed to the high supply (ground) with low-inductance 0.01 μF and 0.1 μF capacitors (see Figure 8A).

T7035 Clock Recovery and Data Retiming Circuit

Overview

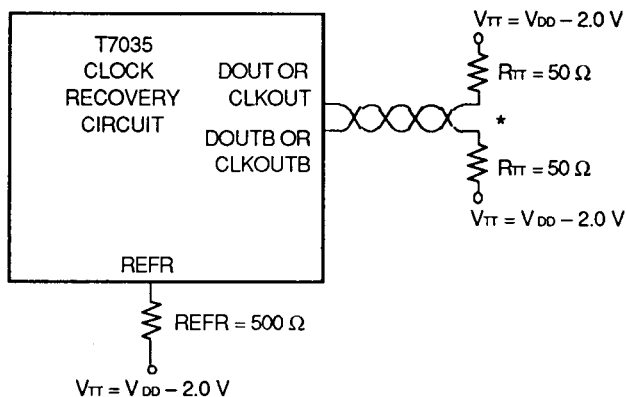
The on-chip clock recovery circuit consists of a phase-locked loop and a digital frequency-locked loop that determine the clock phase and frequency using the positive-going edges of the input data. This recovered clock is used with the input data in the retimer section to synchronize the output data with the positive edge of the clock output.

To ensure accurate frequency selection, the T7035 Clock Recovery Circuit uses a 3.579545 MHz crystal in the delay regulation loop. An external clock reference signal input is also provided if a local clock signal is available. The operating frequency of the device is determined by the circuit's five LSTTL frequency select pins, which are set according to Table 2. The T7035 device can lock to a frequency above and below the specified band edges in Table 2 by a small amount (± 1000 ppm) for applications near the band edges.

The ECL reference resistor connected to the REFR output is necessary to produce the 100K ECL output levels (see Figure 3).

Table 2. Frequency Pin Truth Table

O	L2	L1	L0	N	Frequency	
					Min	Max
1	1	0	1	1	50.5	55
1	1	0	1	0	55	58
1	1	0	0	1	58	61
1	1	0	0	0	61	65
1	0	1	1	1	65	69
1	0	1	1	0	69	74
1	0	1	0	1	74	78
1	0	1	0	0	78	86
1	0	0	1	1	86	94
1	0	0	1	0	94	102
1	0	0	0	1	102	110
0	1	0	1	0	110	119
0	1	0	0	0	119	129
0	0	1	1	1	129	138
0	0	1	1	0	138	147
0	0	1	0	1	147	157
0	0	1	0	0	157	172
0	0	0	1	1	172	188
0	0	0	1	0	188	204
0	0	0	0	1	204	220
0	0	0	0	0	220	237



* See alternate termination description.

Figure 3. T7035 ECL Output Termination Example

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability. External leads can be safely soldered or bonded at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	55	125	°C
Power Supply Voltage	V_{SS}	0.5	6.5	V
Power Dissipation	P_{DISS}	—	800	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω , capacitance = 100 pF) is widely accepted and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold Voltage	
Device	Voltage
T7035	1000 V

Electrical Characteristics

$T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ (see Ordering Information) except as noted, $V_{DD} - V_{SS} = 5\text{ V} \pm 10\%$.

Table 3. Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Using a Negative Supply	V_{SS}	-4.5	-5.5	V
	V_{DD}	0.0	0.0	V
Using a Positive Supply	V_{SS}	0.0	0.0	V
	V_{DD}	4.5	5.5	V
Supply Current*				
235 MHz	I_{SS}	60	140	mA
155 MHz	I_{SS}	50	115	mA
52 MHz	I_{SS}	30	80	mA
Operating Frequency	F_O	50.5	237	MHz
Termination Voltage	V_{TT}	$V_{DD} - 2.1$	$V_{DD} - 1.9$	V
ECL Input Voltage†:				
Low	V_{IL}	$V_{DD} - 1.81$	$V_{DD} - 1.47$	V
High	V_{IH}	$V_{DD} - 1.16$	$V_{DD} - 0.88$	V
ECL Output Voltage:				
Low	V_{OL}	$V_{DD} - 1.81$	$V_{DD} - 1.62$	V
High	V_{OH}	$V_{DD} - 1.02$	$V_{DD} - 0.88$	V
ECL Reference Resistor Tolerance	REFRTOL	-5	5	%
Load Resistor Tolerance	RTTOL	-5	5	%
LSTTL Input Current ‡	I_{IH}	-10	10	A
LSTTL Output Current	I_{OL}	-4		mA
LSTTL Input Voltage‡:				
Low	V_{IL}	—	0.8	V
High	V_{IH}	2.0	$V_{DD} + 0.5$	V
LSTTL Output Voltage‡:				
Low ($I_{OL} = 4\text{ mA}$)	V_{OL}	—	0.4	V
High ($I_{OH} = -400\text{ }\mu\text{A}$)	V_{OH}	2.7		V
LSTTL Input/Output Capacitance	C_I		5.5	pF

* ECL load current not included since this current varies with choice of REFR and RTT.

† All ECL inputs are internally biased to $\sim V_{DD} - 1.32\text{ V}$ through $\sim 30\text{ k}$ pull-up resistors.

‡ All LSTTL input and output voltages are referenced to V_{SS} .

T7035 Clock Recovery and Data Retiming Circuit

Electrical Characteristics (continued)

Table 4. ac Characteristics

The minimum values of this table are measured with $V_{DD} - V_{SS} = 4.5$ V. The maximum values are measured with $V_{DD} - V_{SS} = 5.5$ V.

Parameter	Test Conditions	Min	Max	Unit
LSTTL Output Rise Time	CLOAD = 20 pF*	2.0	6.0	ns
LSTTL Output Fall Time	CLOAD = 20 pF*	2.0	6.0	ns
ECL Output Rise Time	CLOAD = 20 pF†	0.5	2.0	ns
ECL Output Fall Time	CLOAD = 20 pF†	0.5	1.5	ns
Data Skew (relative to clock output)‡ (See Figure 4).	—	-0.5	0.5	ns

* Transition time is measured between the 10% to 90% values.

† Transition time is measured between the 20% to 80% values.

‡ Measured at 50% of pulse amplitudes.

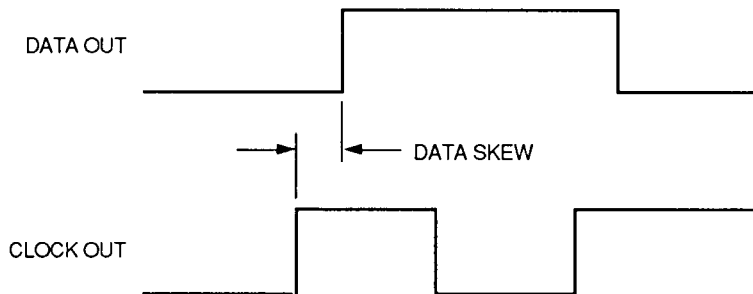


Figure 4. Data Skew

External Reference Crystal Requirements

Parameter	Value	Comments
Frequency	3.579545 MHz \pm 0.05 MHz	MHz*
Series Resistance	185 Ω	Maximum Value

* Example: Digikey X079 3.579545 MHz.

Jitter Characteristics

The jitter characteristics of T7035 are specified in three ways (using a PRBS of $2^7 - 1$):

- Output jitter with a specific jitter-free input pattern
- Jitter transfer for small amplitude input jitter over a range of jitter frequencies
- Jitter accommodation or tolerance for particular input jitter amplitudes and frequencies

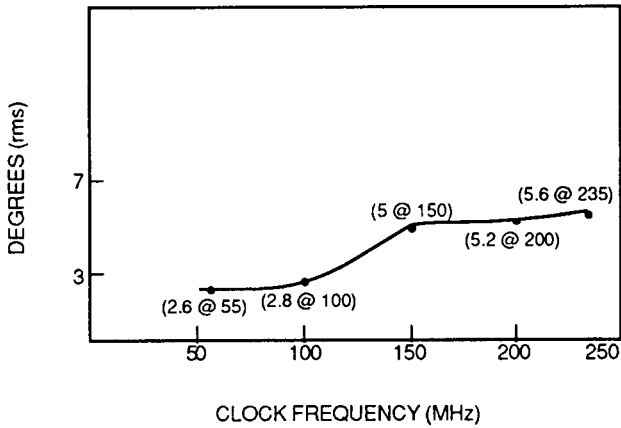


Figure 5. Typical Output Jitter vs. Clock Frequency

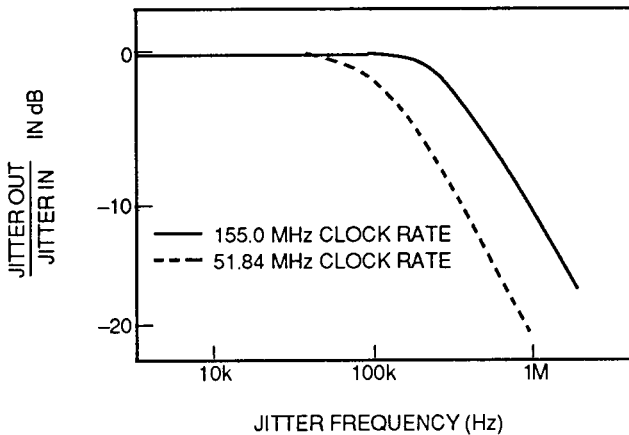


Figure 6. Typical Jitter Transfer

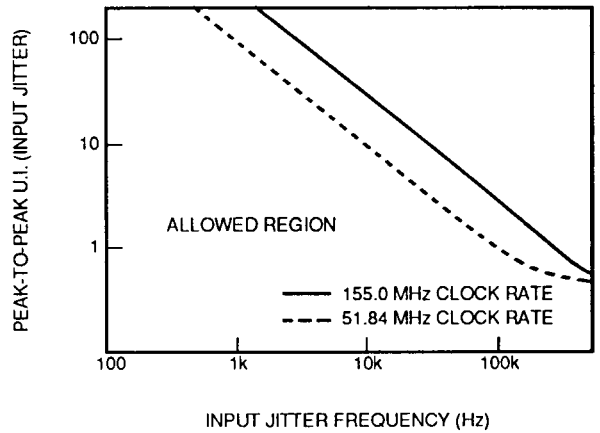


Figure 7. Typical Jitter Accommodation

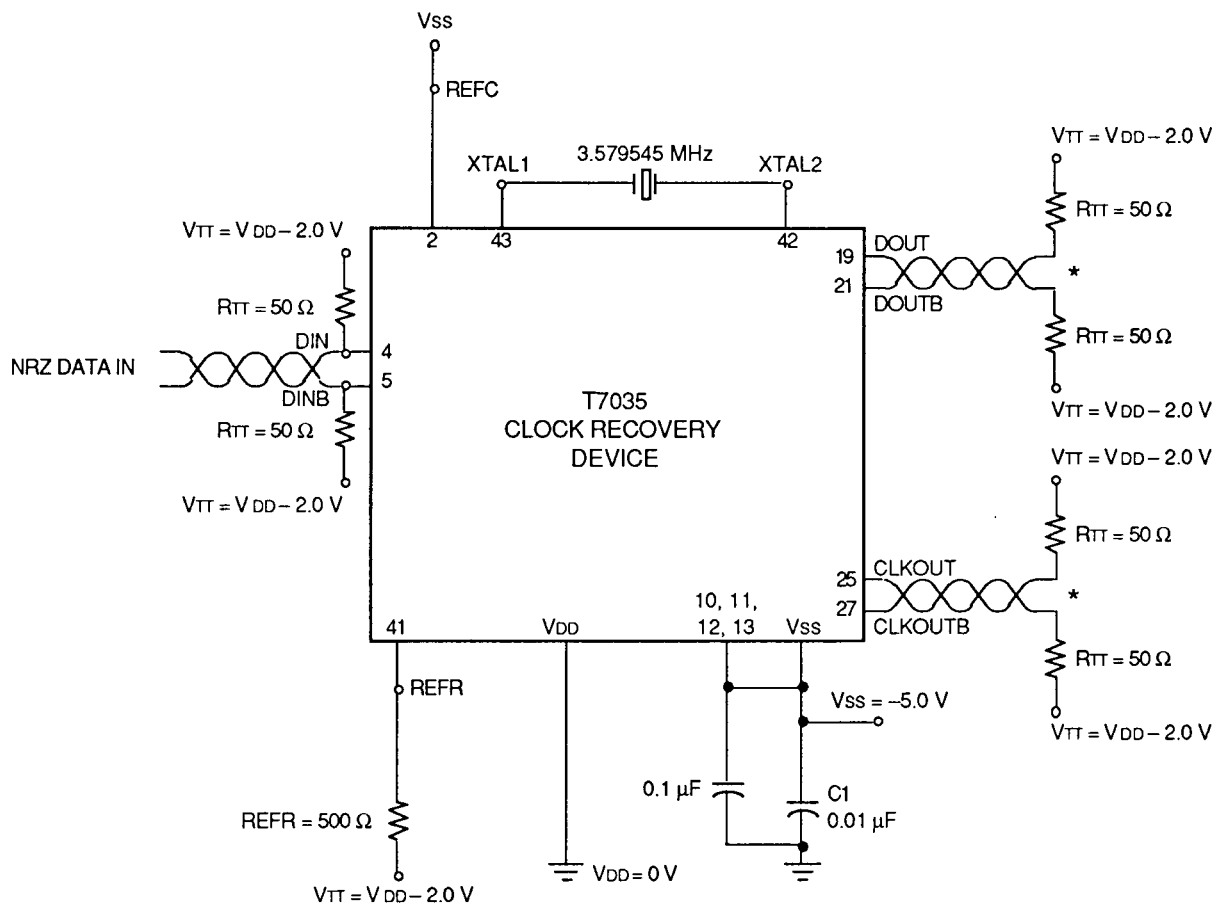
Noise Properties

Closely related to the jitter characteristics is the response of the T7035 to time domain input noise. This noise can arise when the T7035 is used in an optical system operated at low signal power. The performance of the T7035 with this type of noisy input is characterized by a noise factor (in dB). Simply stated, the noise factor is the increase in optical power necessary to overcome the imperfections of T7035's internal strobe position and jitter. Compared to an ideal clock recovery circuit, where the internal strobe is positioned exactly in the middle of the data eye (at 1/2 the data period) and has no jitter, the T7035 requires, at most, 1 dB (typically, much less than 1 dB) more optical power to achieve the same bit error rate as the ideal circuit.

Applications

Power Supply Configurations

Figure 8 shows the two basic power arrangement applications for the T7035.



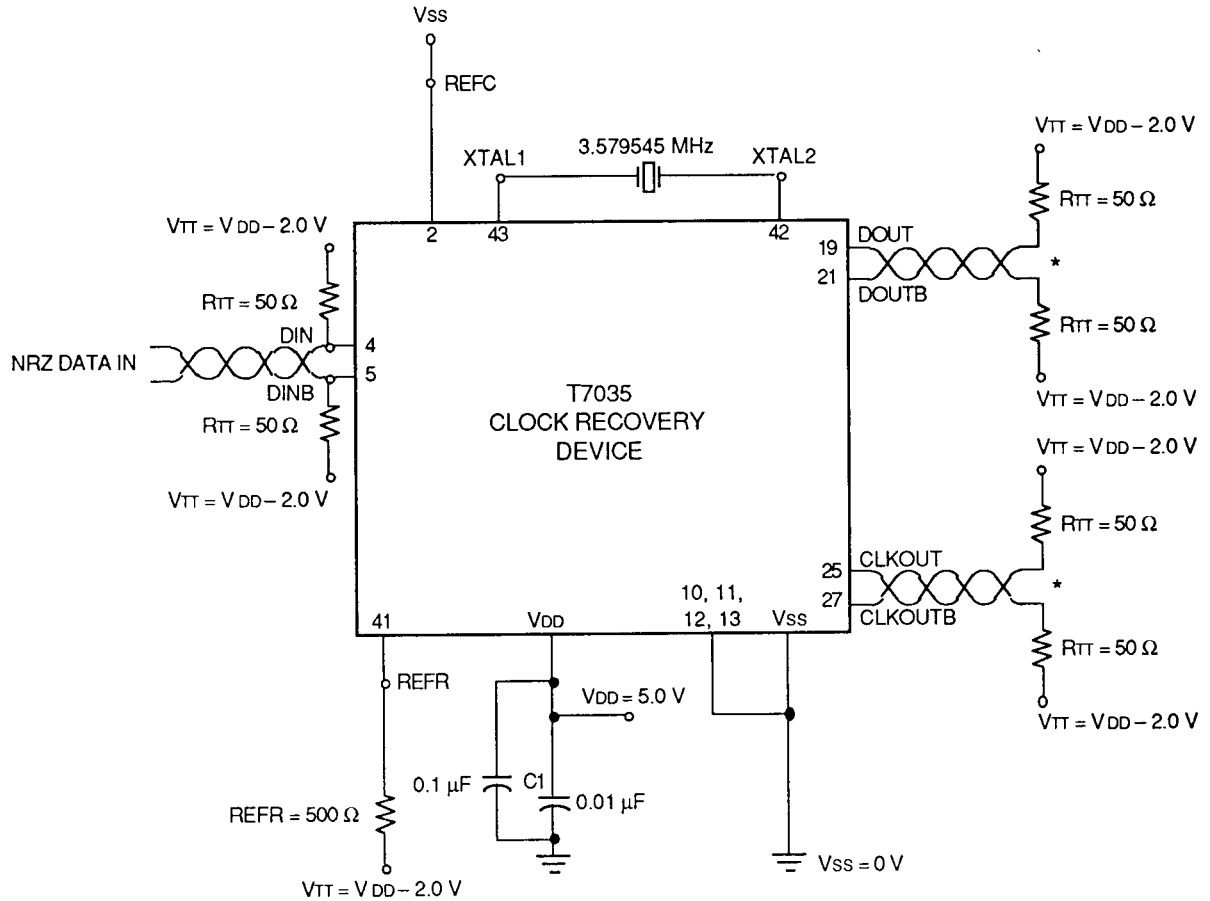
A. Typical Configuration for $V_{DD} = 0$, $V_{SS} = -5.0$ V

* See alternate termination description.

Figure 8. ECL Input Configuration

Applications (continued)

Power Supply Configurations (continued)



B. Typical Configuration for VDD = 5.0 V, VSS = 0

* See alternate termination description.

Figure 8. ECL Input Configuration (continued)

Applications (continued)

Using the Frequency Freeze Control (FFC) with an Optical Receiver

When optical receivers do not receive any optical input, they usually output large amounts of random noise which can have harmful effects on subsequent circuits like the T7035. The T7035 has the capability to freeze its operation for this condition by asserting the FFC (pin 13) high. This mode can be automated easily by utilizing the carrier detect or flag signals provided by most optical receivers. If the flag signal is an ECL level in a single-power-supply system (either +5 V or -5 V), a translator, such as the AT&T 41LF, can be used to provide the TTL level required for pin 13.

Alternate ECL Output Terminations

Thevenin Equivalent ECL Loads

Many systems do not have the required -2 V supply necessary to terminate the outputs of the T7035. In this case, a Thevenin equivalent load can be easily synthesized. For a single +5 V or -5 V supply, an 82 Ω resistor connected to the most positive supply joined to a 130 Ω resistor connected to the most negative supply will provide a 50 Ω load terminated 2 V below the most positive supply. For a 5.2 V supply, the resistor values for a 50 Ω load should be 82 Ω and 120 Ω , respectively. The resistor tolerance should be $\pm 5\%$ in all cases, and the resistors connected to REFR (pin 41) should be multiplied in value by 10. For values higher than 50 Ω (50 Ω is the minimum load allowed for the T7035), simply scale each resistor value proportionately; for 100 Ω , multiply each resistor by 2. It may be necessary to bypass the power and ground connections of each resistor.

Alternate ECL Output Termination for Low-Power Applications

The network in Figure 9 can be utilized as an alternate termination for the ECL output pairs DOUT/DOUTB and CLKOUT/CLKOUTB.

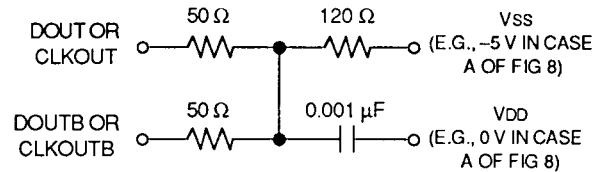


Figure 9. ECL Output Termination Network for Low-Power Applications

Data-In to Data-Out Delay

The delay from data input to data output is not a controlled parameter. This delay varies significantly with silicon manufacturing variations, temperature, and power supply variations. It is recommended that signals synchronous with the input data should not be clocked with the recovered clock output since clock output is precisely aligned only to the data output, but has an uncontrolled timing relationship with respect to the input of the T7035.

T7035 Clock Recovery and Data Retiming Circuit

Ordering Information

Device Code	Package	Temperature	Comcode
T7035-MC	44-pin PLCC	0 °C to 70 °C	105524482
T7035-ML	44-pin PLCC	-40 °C to +85 °C	106419369

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