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A TDK Group Company

SSI 32C9600
ATA-2 Storage Controller
160 Mbit/s, 8-Bit NRZ Interface

Advance Information

November 1994

DESCRIPTION

The SSI 32C9600 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The SSI 32C9600 has an eight bit wide NRZ channel interface with disk transfers rates up to 160 Megabits per second, an advanced ATA interface which supports host transfer rates up to 20 megabytes per second, and a sixteen bit wide data buffer interface capable of supporting concurrent full speed transfers on both disk and host interfaces. The circuitry of the SSI 32C9600 includes: a complete, highly automated ATA interface; an advanced, fully integrated Buffer Manager; a high performance Disk Formatter; and two fast Reed-Solomon ECC's, one for the header field and a second for the data field, both with on-the-fly hardware correction. The SSI 32C9600 maximizes performance while minimizing microcontroller intervention.

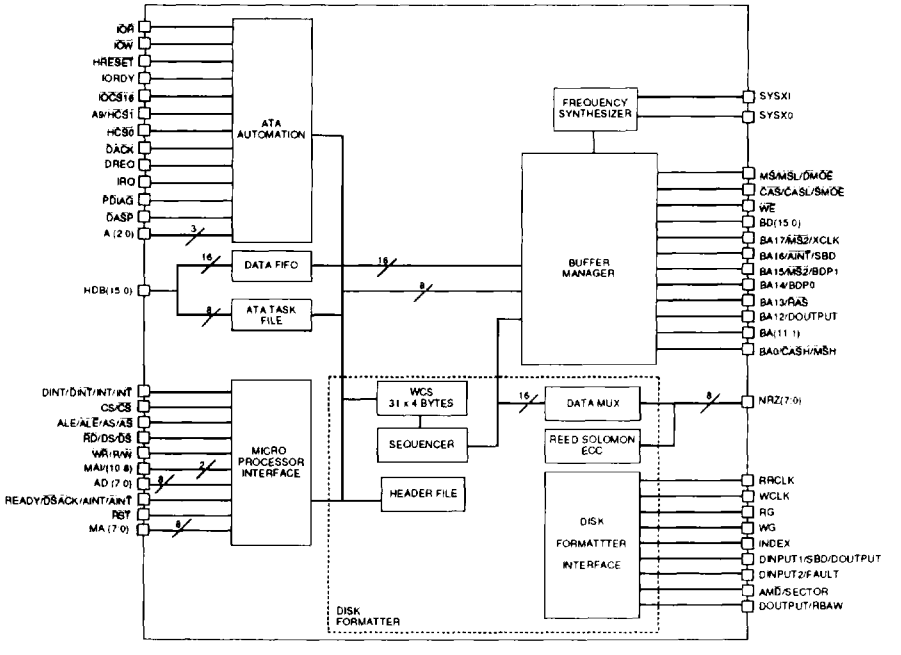
(continued)

FEATURES

- **ATA Interface**
  - **Single chip PC AT controller (IDE)**
  - **Full ANSI ATA-1 and ATA-2 compliance**
  - **Direct PC bus connection with on-board 12 mA drivers**
  - **PC transfers to 10 megawords (20 megabytes) per second**
  - **Supports PIO, DMA and Multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operates as Master, Slave or both**
  - **Automatic command decoding of Write, Write Long, Write Multiple, Write DMA, Write Buffer and Format commands.**

(continued)

BLOCK DIAGRAM



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SSI 32C9600
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DESCRIPTION (continued)

The SSI 32C9600 also supports dual bit NRZ interfaces. In dual bit mode, transfer rates up to 100 megabits per second on the disk interface are supported.

The highly automated Header ECC logic performs corrections on the header within one or two byte times, and Data ECC is capable of performing corrections in real time, allowing the SSI 32C9600 to read every sector on the disk in a single revolution even if every sector contained a correctable error.

The SSI 32C9600 is the latest in a line of sophisticated disk storage controllers. Other Silicon Systems' disk storage controllers include: the SSI 32C9800 SCSI-3 controller, with host transfer rates up to 20 megabytes per second and disk data rates of up to 160 megabits per second. The SSI 32C9001, SSI 32C9301, SSI 32C9302 and SSI 32C9003 ATA controllers provide dual and serial NRZ data rates to 80 Megabits per second and ATA speeds to 13.3 megabytes per second. The SSI 32C9020, SSI 32C9022, SSI 32C9023 and SSI 32C9024 family members are SCSI disk controllers supporting fast, 8-bit wide SCSI interface, with disk data rates to 80 Megabits per second. The SSI 32C9340 disk controller completes the family providing PCMCIA/ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9600 represents a major reduction in parts count. When the SSI 32C9600 ATA Controller is combined with the SSI 32R1510BR or SSI 32R2110R Read/Write device, the SSI 32P4782 Read Channel (1,7) or SSI 32P4910 PRML Read Channel (8/9), the 32H6826 Servo/Spindle Controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Hardware support for Read Multiple and Write Multiple commands
- Hardware support for Cyl/Hd/Sec and LBA addressing modes, including automatic updates of the host task file registers in both modes
- Automatic Multi-Sector data transfers without microprocessor intervention
- Automatic Host Interrupt and Busy for multiple sector transfers
- 32 byte FIFO to improve performance
- Extensive Power Down modes

• Buffer Manager
- Direct support of DRAM or SRAM
  - SRAM: up to 256k bytes of memory with throughput to 40 megabytes per second
  - DRAM: up to 8 megabyte of memory with throughput to 36 megabytes per second
- Buffer CRC and/or buffer parity for increased data integrity
- Programmable memory timing
- Flexible buffer RAM segmentation
- Dedicated host, disk and microprocessor address pointers
- Buffer streaming with internal buffer protection circuit providing buffer integrity

• Disk Formatter
- 8-Bit or 4-Bit NRZ interface supporting data rates to 160 megabits per second, or
- 2-Bit NRZ interface supporting data rates to 100 megabits per second
- Automatic multi-sector transfers
- Error tolerant sync detection
- Header based split data field support
- Advanced sequencer organized in 31 x 4 bytes
- Timeouts for sync detection, sector or index pulse detection, and retry limiting
- 144-bit Reed Solomon ECC for the data field, with "on-the-fly" fast hardware correction circuitry

  - Capable of correcting up to six 8-bit symbols in error
  - Guaranteed to correct a single 41-bit error burst, or two 17-bit error bursts
  - Fast hardware on-the-fly correction assures continuous data transfers even if consecutive sectors are in error
- 40-bit Reed Solomon ECC for the header field, with "on-the-fly" hardware correction circuitry which completes within 1 or 2 byte times
  - Guaranteed to correct a single 9-bit error burst

- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate host and disk interrupts
  - 1024 byte buffer window with wait stated or polled access
- Other Features
  - Frequency synthesizers for buffer clock
  - Internal Power Down mode
  - Available in 128-pin QFP or TQFP

FUNCTIONAL DESCRIPTION

The SSI 32C9600 contains the following four major functional blocks:

Microprocessor Interface
ATA Interface
Disk Formatter
Buffer Manager

The microprocessor interface allows the local microprocessor access to all of the SSI 32C9600 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9600. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9600 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 12 mA drivers allowing for direct connection of the SSI 32C9600 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro-controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching

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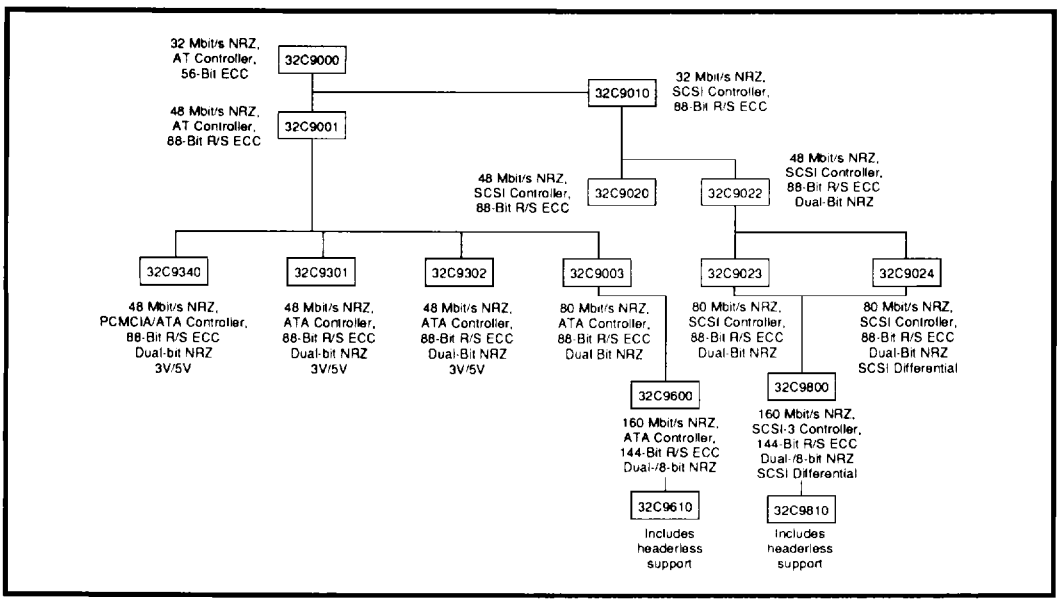

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION (continued)

FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The disk formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the disk formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 4 bytes (32 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities.

This allows the SSI 32C9600 to interface with many different read/write channels and allows the user of the SSI 32C9600 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9600 controller and the SSI 32P4910 PRML read channel (8/9), you are guaranteed a problem free interface.

Within the disk formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 40-bit Reed-Solomon ECC for headers and a 144-bit Reed-Solomon code for data. The header ECC circuitry performs correction of the header bytes within one or two byte times, minimizing delays. The data ECC correction circuitry performs data corrections rapidly. The data ECC circuitry guarantees that the correction logic will always be available to correct the next sector if necessary.

The disk formatter provides additional reliability by use of error tolerant sync detection. This feature allows the creation of a multi-byte sync field and the detection of data synchronization even in the event of errors within the sync field.

The buffer manager manages the data buffer of the controller. The buffer manager can support either SRAM or DRAM. When configured to operate with DRAM, the buffer manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the buffer manager interfaces with the ATA Interface block, the disk formatter block, the ECC corrector and the microprocessor. If more than one of these blocks requires access to the buffer memory, the buffer manager arbitrates the requests automatically. The buffer manager of the SSI 32C9600 can sustain ATA operations at the rate of 10 megawords (20 megabytes) per second, disk formatter operations at 160 megabits per second and still has sufficient band-width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

Besides the ability to generate and check data parity, the ATA interface also includes a CRC generation and checking capability. During writes, a CRC can be generated on data received from the host and checked when the data is transferred to the Disk Formatter. The CRC is part of the data ECC and is always written by the Disk Formatter. If the ATA interface generates the CRC, then the Disk formatter writes the CRC field that was generated by the ATA interface to the media, or the Disk Formatter generates the CRC itself. During reads the CRC is read from the media by the Disk Formatter. If buffer CRC is enabled, the Disk Formatter writes the CRC to the buffer and the CRC is re-checked by the ATA interface when the data is transferred to the host, or the Disk Formatter checks the CRC that is read from the media. The addition of CRC to the ATA interface adds a high degree of integrity, and detects most memory errors that may occur in the buffer memory.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(I/O) denotes a bidirectional signal
(Z) denotes a tri-state output
(OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{HCS1}$.

GENERAL

NAME	TYPE	DESCRIPTION
VDD	-	POWER SUPPLY PIN
GND	-	GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various host control, status, and data registers.
A9/$\overline{HCS1}$	I	HOST CHIP SELECT 1. This pin selects access to the control block task file registers.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin selects access to the command block task file registers.
$\overline{IOCS16}$	OD	16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
IRQ	Z	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	Z	I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin will be tristated when a read or write is not in progress.
DREQ	Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA transfer between the host and the controller.
$\overline{IOR}$	I	I/O READ. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the device is enabled onto the host data bus if the device is currently selected.
$\overline{IOW}$	I	I/O WRITE. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the host data bus is strobed into the device.

PIN DESCRIPTION (continued)

HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — This signal can also "wake up" the device while it is in power down mode.
HDB(15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.
$\overline{\text{DASP}}$	I,OD	DRIVE ACTIVE/DRIVE 1 PRESENT. This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present.
$\overline{\text{PDIAG}}$	I,OD	PASSED DIAGNOSTICS. This signal is an output when configured as Drive 1 and an input when configured as Drive 0.

DISK INTERFACE

INDEX	I	INDEX. This pin serves as the index function for the disk sequencer. When the INPUT function is not available on the BA16 pin, this pin can function as input or index.
DOUTPUT/RBAW	O	DISK SEQUENCER OUTPUT/READ BIAS ACTIVE WHILE WRITING. This pin is controlled by bit 2 of the disk sequencer's control field when configured as DOUTPUT. It performs the read bias active while writing function when configured as RBAW.
DINPUT1/SBD/ DOUTPUT	I/O	DISK SEQUENCER INPUT 1: This pin may be used to synchronize the sequencer to an external event.
DINPUT2/FAULT	I	DISK SEQUENCER INPUT 2: This pin may be used to synchronize the sequencer to an external event, or as a write fault signal.
$\overline{\text{AMD}}$/SECTOR	I	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer.
RRCLK	I	READ REFERENCE CLOCK. This pin is used in conjunction with the NRZs pin to clock data in. It is also used as a clock for the disk sequencer and is used to generate WCLK.
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out.
NRZ (7:0)	I/O	NON RETURN TO ZERO. These signals are the read data input 0 through 7 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. NRZ7 is the most significant bit.

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the controller at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/$\overline{ALE}$/AS/$\overline{AS}$	I	ADDRESS LATCH ENABLE/ADDRESS STROBE: This pin functions as the address latch enable or address strobe. This pin is only used when the microprocessor interface is programmed for multiplexed address and data mode. The address bits on AD(7:0) and MAI(10:8) are applied to a transparent latch which is gated by this signal. The lower 8 bits of latched address are output on the MA (7:0) pins.
CS/$\overline{CS}$	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the Write strobe signal is asserted low and the CS signal is asserted high, the data on the AD lines will be written to the register. When the Motorola bus control interface is selected, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the DS signal and the CS signal asserted indicates a read operation. A low on this input along with the DS signal asserted and the CS signal deasserted indicates a write operation.
$\overline{RD}$/DS/$\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD signals. When the Motorola bus control interface is selected, this signal acts as the DS/$\overline{DS}$ signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation.
DINT/$\overline{DINT}$/INT/$\overline{INT}$	O, OD	DISK INTERRUPT/INTERRUPT. This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin READY/$\overline{AINT}$ is programmed as Ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-multiplexed mode, these lines are bidirectional data lines.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a Multiplexed type microprocessor cycle. These signals are non-multiplexed address inputs when used with a Non-multiplexed microprocessor.
MAI (10:8)	I	MICROPROCESSOR ADDRESS INPUTS: These signals are address input lines for the high bits of the address. They are inputs regardless of whether multiplexed or non-multiplexed data and address busses are used. In the multiplexed mode, these bits are latched internally with the ALE/$\overline{\text{ALE}}$/AS/$\overline{\text{AS}}$ signal; in the non-multiplexed mode, they are not latched.
READY/$\overline{\text{DSACK}}$/ AINT/$\overline{\text{AINT}}$	O, OD	READY/DATA STROBE ACKNOWLEDGE/AT INTERRUPT: This pin may be configured as the Ready function or the data strobe acknowledge function for adding wait states to local microprocessor accesses, or as a separate local microprocessor interrupt for the host interface. This pin may be configured as push-pull or open-drain. After $\overline{\text{RST}}$ is asserted, this signal is configured as open-drain, and as Ready or $\overline{\text{DSACK}}$, depending upon the value latched at the BD (3) pin.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
SYSXI	I	CRYSTAL INPUT/SYSTEM CLOCK: This is the crystal input to the buffer manager frequency synthesizer, or the clock input that is used to generate buffer memory access cycles when the frequency synthesizer is bypassed.
SYSXO	O	CRYSTAL OUTPUT.
$\overline{\text{CAS}}$/$\overline{\text{CASL}}$/$\overline{\text{SMOE}}$	O	COLUMN ADDRESS STROBE/COLUMN ADDRESS STROBE LOW BYTE: SRAM Memory output enable: This signal is used as the column address strobe in DRAM mode when using 8-bit data buffer bus. This signal is used as the column address strobe for the low data byte in DRAM mode when using 16-bit data buffer bus. This signal is used as the memory output enable in SRAM mode. After RST is asserted, this signal will be high and function as CAS.
$\overline{\text{WE}}$	O	WRITE ENABLE: This signal is asserted low when a buffer memory write operation is active.
BD(15:0)	I/O	BUFFER MEMORY DATA BUS: These signals are bits 15-0 of the 16-bit parallel data lines to/from the buffer memory.
BA17/$\overline{\text{MS2}}$/XCLK	O	BUFFER ADDRESS 17: MEMORY SELECT 2/ SYNTHESIZER OUTPUT CLOCK: This signal is either the output of the frequency synthesizer, memory select 2, or buffer address 17. This pin may be programmed as a second memory select when two 128 kilobyte SRAMs are used in an 8-bit wide buffer configuration.
BA16/$\overline{\text{AINT}}$/SBD	I/O	BUFFER ADDRESS 16/AT INTERRUPT/SYNC BYTE DETECT: This signal may be used for addressing the buffer memory in SRAM mode, or as separate local microprocessor interrupt for the host interface, or as a sync byte detect signal input for the disk formatter.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BA15/$\overline{MS2}$/BDP1	I/O	BUFFER ADDRESS 15/MEMORY SELECT 2/BUFFER DATA PARITY 1: This signal may be used as buffer address 15 or memory select 2 in SRAM mode, or as the parity bit for BD (15:8) in DRAM mode.
BA14/BDP0	I/O	BUFFER MEMORY ADDRESS 14/BUFFER DATA PARITY 0: This signal is used for addressing the buffer memory in SRAM mode, or as the parity bit for BD (7:0) in DRAM mode.
BA13/$\overline{RAS}$	I/O	BUFFER MEMORY ADDRESS 13/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode, or as the row address strobe in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA12/DOUTPUT	O	BUFFER MEMORY ADDRESS 12/DISK SEQUENCER OUTPUT: This signal is used for addressing the buffer memory, or it may be configured as the disk sequencer output pin and be controlled by bit 2 of the disk sequencer's control field. After $\overline{RST}$ is asserted, this signal will be buffer memory address 12.
BA (11:1)	O	BUFFER MEMORY ADDRESS LINES: These are bits 11-1 for addressing the buffer memory.
BA0/$\overline{CASH}$/$\overline{MSH}$	O	BUFFER MEMORY ADDRESS 0/COLUMN ADDRESS STROBE HIGH BYTE/MEMORY SELECT HIGH BYTE: When an 8-bit wide buffer is used, this signal is buffer memory address 0. When a 16-bit wide buffer is used, this signal is the column address strobe for the high data byte in DRAM mode, or the memory select for the high data byte in SRAM mode.
$\overline{MS}$/$\overline{MSL}$/$\overline{DMOE}$	O	MEMORY SELECT/MEMORY SELECT LOW BYTE/DRAM MEMORY OUTPUT ENABLE: This pin is configured as memory select in SRAM mode, or as memory output enable in DRAM mode.

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PARAMETER	RATING
Ambient temperature under bias	0 to 70°C
Storage temperature	-65 to 150°C
Voltage on any pin with respect to ground	GND -0.5 TO VCC +0.5V
Power dissipation	750 mW
Power supply voltage	+7V
Maximum current injection	50 mA

D.C. SPECIFICATIONS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply voltage	VDD	3.3V nominal	3		3.6	V
Supply voltage	VDD	5V nominal	4.5		5.5	V
Input low voltage	VIL	All pins at 3.3V or 5V nominal	-0.5		0.8	V
Input high voltage	VIH	All pins at 3.3V or 5V nominal	2		VCC+0.5	V
Output low current	VOL	IOL = 2 mA			0.4	V
Output low current host i/f	VOLA	IOL = 12 mA			0.5	V
Output high voltage	VOH	IOH = 400 µA			2.4	V
Supply current	IDD	VDD = 3.3V nominal			70	mA
Supply current	IDD	VDD = 5V nominal			100	mA
Standby current	IDDS	All inputs at GND or VDD	250			µA
Input leakage current	IL	0 < Vin < VDD	-10		10	µA
Input capacitance	CIN				10	pF
Output capacitance	COUT				10	pF

A.C. SPECIFICATIONS

The following timings assume that all output pins will drive one TTL load in parallel with 30 pF. The timings conform to the operating ranges of a power supply voltage of 5V with 10% variance, and an ambient temperature of 0 to 70°C.

MICROPROCESSOR INTERFACE TIMING PARAMETERS

Multiplexed Bus Interface Timings

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
ALE/$\overline{ALE}$ width	Ta		20			ns
Address valid to MA (7:0) valid	Tma				30	ns
Address valid to ALE↓	As		5			ns
ALE↓ to address invalid	Ah		10			ns
CS valid to $\overline{RD}$↓ or $\overline{WR}$↓ or $\overline{DS}$↓	Cs		10			ns
$\overline{RD}$↑ or $\overline{WR}$↑ or $\overline{DS}$↑ to CS↓	Ch		0			ns
Address valid to read data valid	Taa				50	ns
$\overline{RD}$↓ or $\overline{DS}$↓ to read data valid except WCS access	Tda				30	ns
$\overline{RD}$↓ or $\overline{DS}$↓ to read data valid for WCS access	Tdawcs				50	ns
$\overline{WR}$ or $\overline{DS}$ width for write	Tww		40			ns
$\overline{RD}$↑ or $\overline{DS}$↑ to read data invalid	Tdh		0		25	ns
R/$\overline{W}$ valid to $\overline{DS}$↓	Tsrw		20			ns
$\overline{DS}$↑ to R/$\overline{W}$ invalid	Thrw		20			ns
$\overline{RD}$↓ or $\overline{DS}$↓ to READY	Tdrdy				30	ns
Write data valid to $\overline{WR}$↑ or $\overline{DS}$↑	Wds		30			ns
$\overline{WR}$↑ or $\overline{DS}$↑ to write data invalid	Wdh		10			ns

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ELECTRICAL SPECIFICATIONS (continued)

MICROPROCESSOR INTERFACE TIMING PARAMETERS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
MA (7:0) valid $\overline{DS}\downarrow$	Tmas		10			ns
$\overline{DS}\uparrow$ to MA (7:0) invalid	Tmah		5			ns
CS valid to $\overline{DS}\downarrow$	Csn		10			ns
$\overline{DS}\uparrow$ to CS$\downarrow$	Chn		0			ns
Address valid to read data valid	Taan				50	ns
$\overline{DS}\uparrow$ to read data valid	Tdan				30	ns
$\overline{DS}$ width for write	Twwn		40			ns
$\overline{DS}\uparrow$ to read data invalid	Tdh		0		25	ns
R/$\overline{W}$ valid to $\overline{DS}\downarrow$	Tsrwn		20			ns
$\overline{DS}\uparrow$ to R/$\overline{W}$ invalid	Thrwn		20			ns
$\overline{DS}\downarrow$ to READY$\downarrow$	Tdrdy				30	ns
Write data valid to $\overline{DS}\downarrow$	Wdsn		30			ns
$\overline{DS}\uparrow$ to write data invalid	Wdhn		10			ns

Note: Loading capacitance = 30 pF

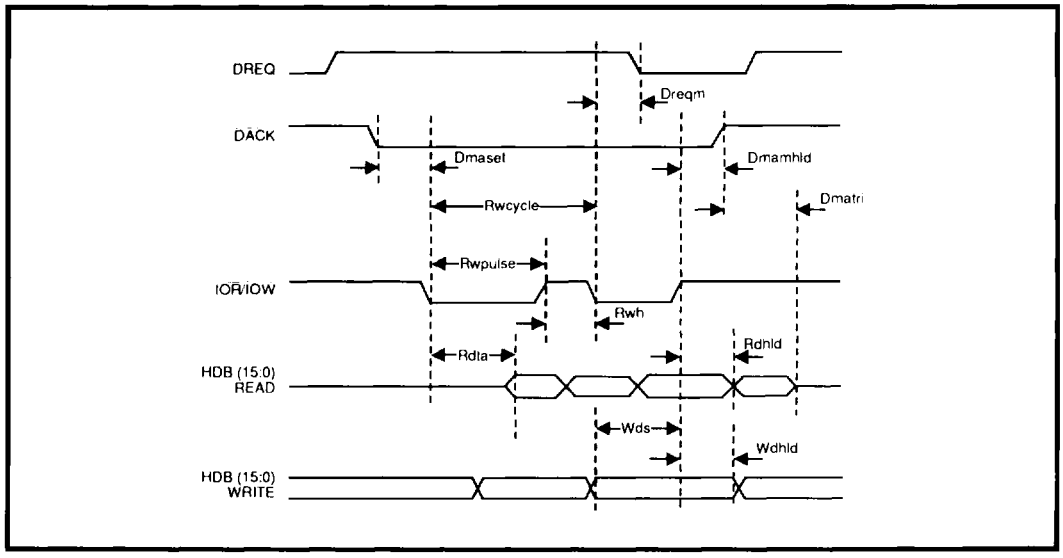

FIGURE 2: Multiword DMA Timing

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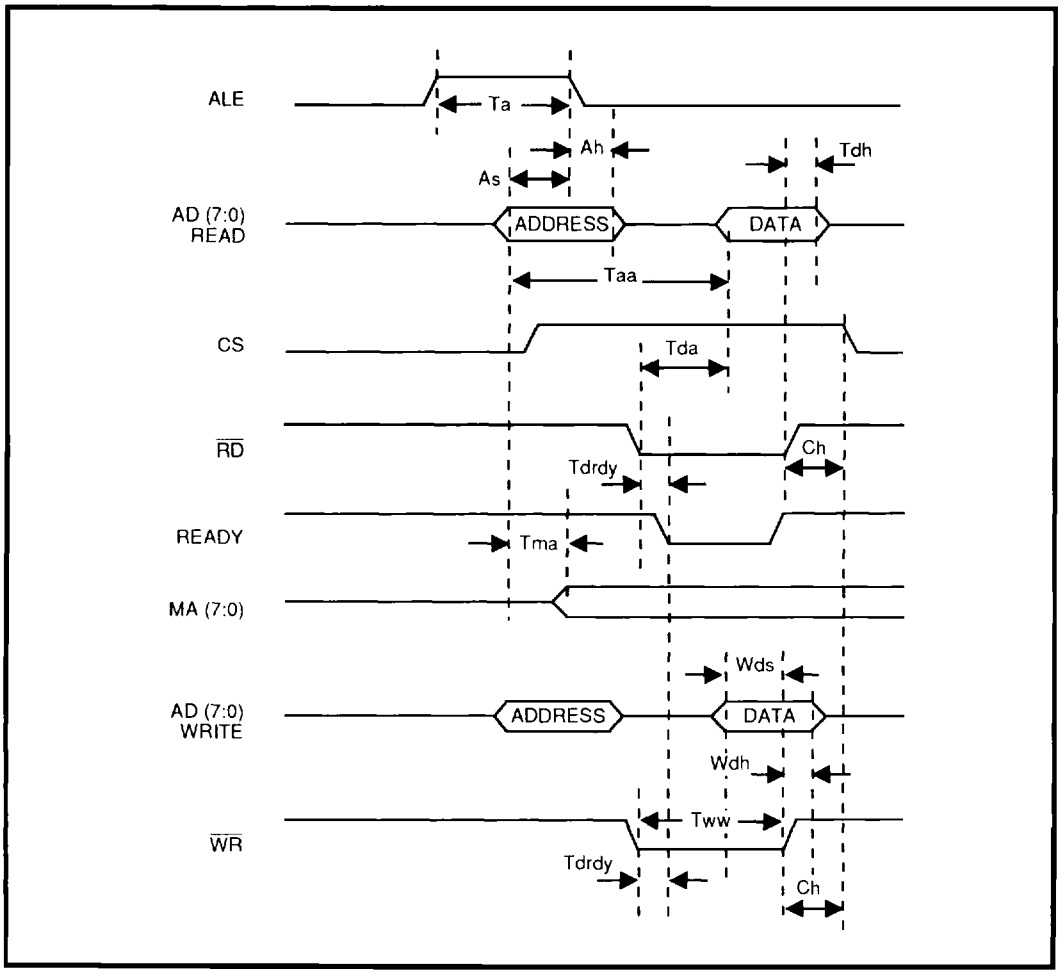

FIGURE 3: Multiplexed Intel Register Timing

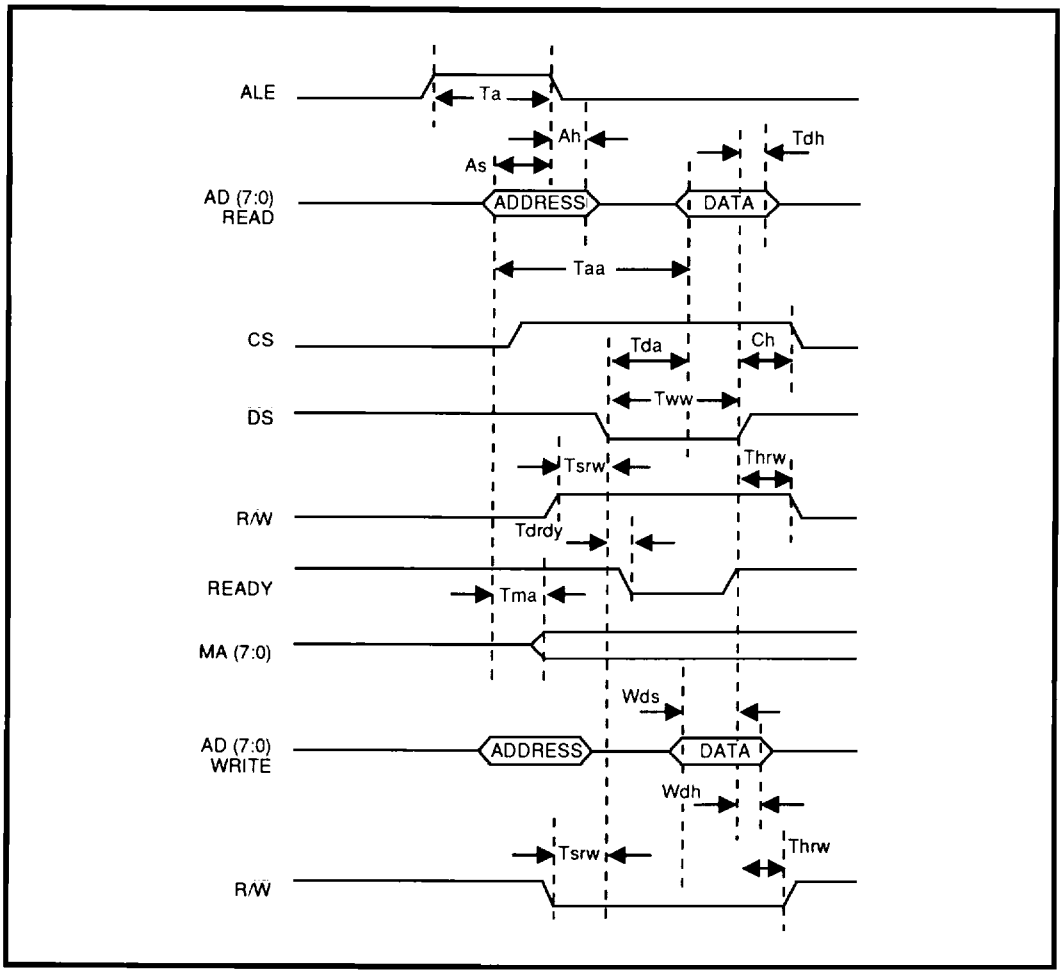

FIGURE 4: Multiplexed Motorola Register Timing

ELECTRICAL SPECIFICATIONS (continued)

DISK INTERFACE TIMING PARAMETERS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
RRCLK period (dual bit) Trrc		20			ns
RRCLK period (byte wide) Trrc		50			ns
RRCLK low time (dual bit) Trrcl		8			ns
RRCLK low time (byte wide) Trrcl		8			ns
RRCLK high time (dual bit) Trrch		20			ns
RRCLK high time (byte wide) Trrch		20			ns
NRZ in valid to RRCLK high Dis		4			ns
RRCLK high to NRZ in invalid Dih		4			ns
RRCLK high to NRZ1 out valid Dv		3		20	ns
WCLK low to NRZ out valid Dvw		-4		+4	ns

Note: Loading capacitance = 30 pF

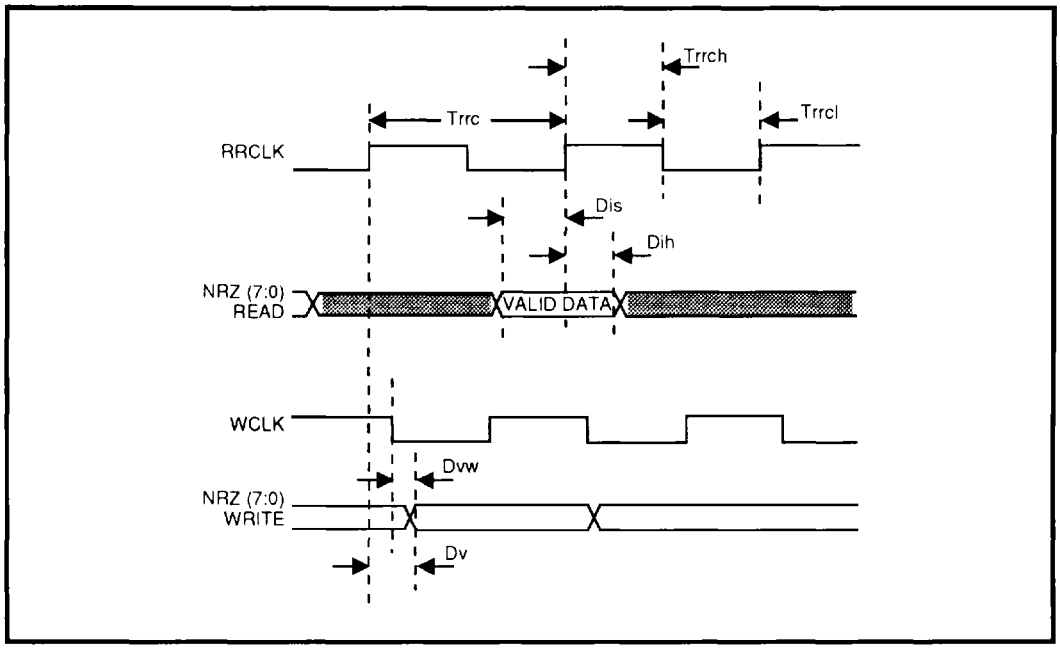

FIGURE 5: Disk Interface Timing Diagram

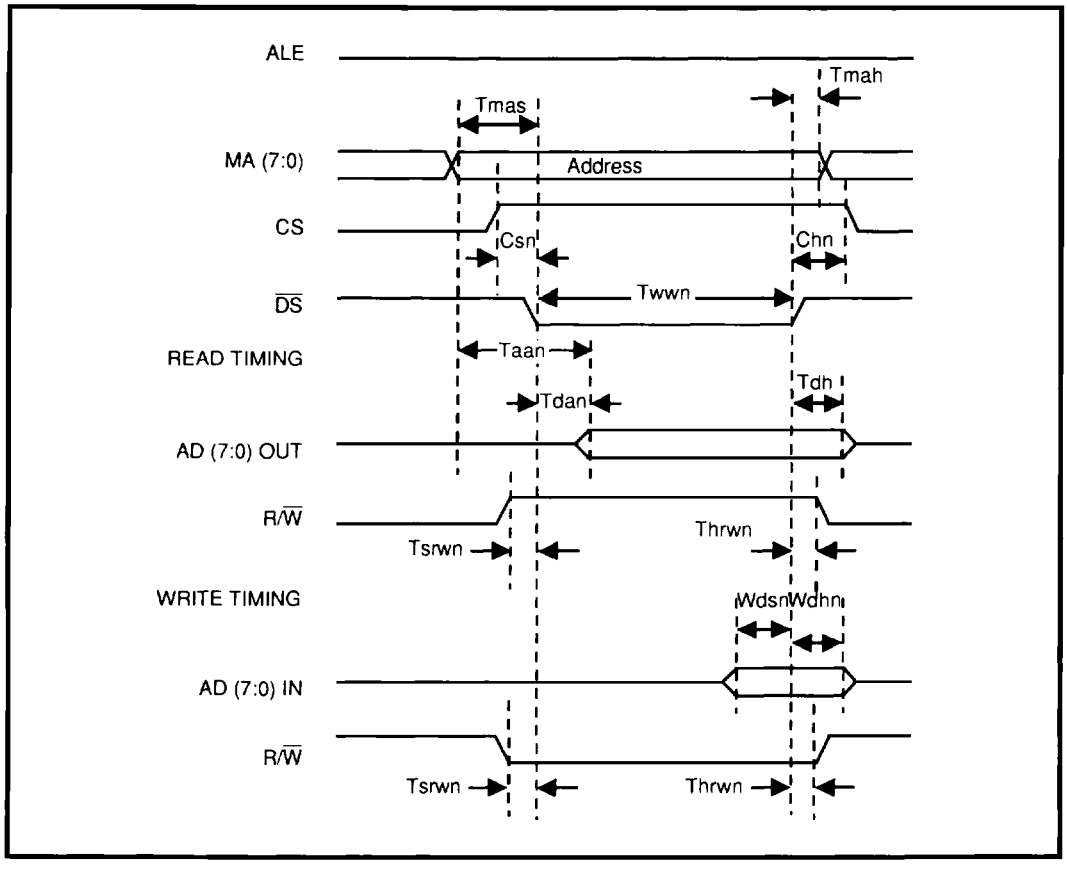

FIGURE 6: Non-Multiplexed Timing

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SYSCLK period	T		25			ns
SYSCLK↑ to address valid	Tav				20	ns
SYSCLK↑ to $\overline{MOE}$↓	Tmv				20	ns
SYSCLK↑ to $\overline{MOE}$↑	Tmh				20	ns
SYSCLK↑ to $\overline{WE}$↓	Twv				20	ns
SYSCLK↑ to $\overline{WE}$↑	Twh				20	ns
SYSCLK↑ to data out valid	Tdov				20	ns
SYSCLK↑ to data out in invalid	Tdoh				20	ns
Data in valid to $\overline{MOE}$↑ (SRAM) Data in valid to $\overline{CAS}$↑ (DRAM)	Tdis		5			ns
$\overline{MOE}$↑ to data in valid (SRAM) $\overline{CAS}$↑ to data in valid (DRAM)	Tdih		0			ns
SYSCLK↑ to $\overline{RAS}$↓	Trv				20	ns
SYSCLK↑ to $\overline{RAS}$↑	Trh				20	ns
SYSCLK↑ to row address valid	Trav				20	ns
SYSCLK↑ to row address invalid	Trah				20	ns
SYSCLK↑ to $\overline{CAS}$↓	Tcv				20	ns
SYSCLK↑ to $\overline{CAS}$↑	Tch				20	ns
SYSCLK↑ to column address valid	Tcav				20	ns
SYSCLK↑ to column address invalid	Tcah		0			ns

Note: Loading capacitance = 30 pF

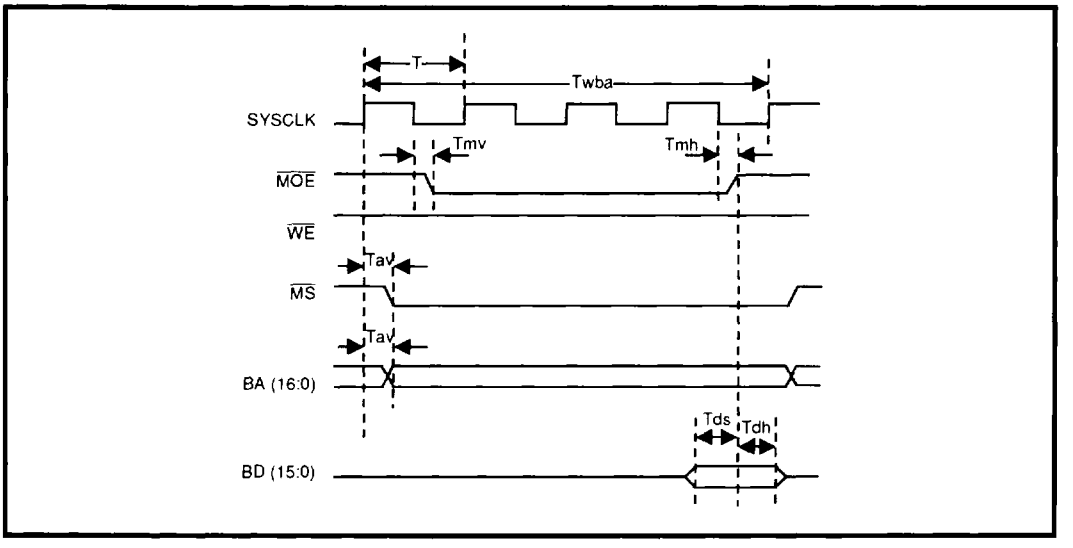

FIGURE 7: SRAM Read Timing

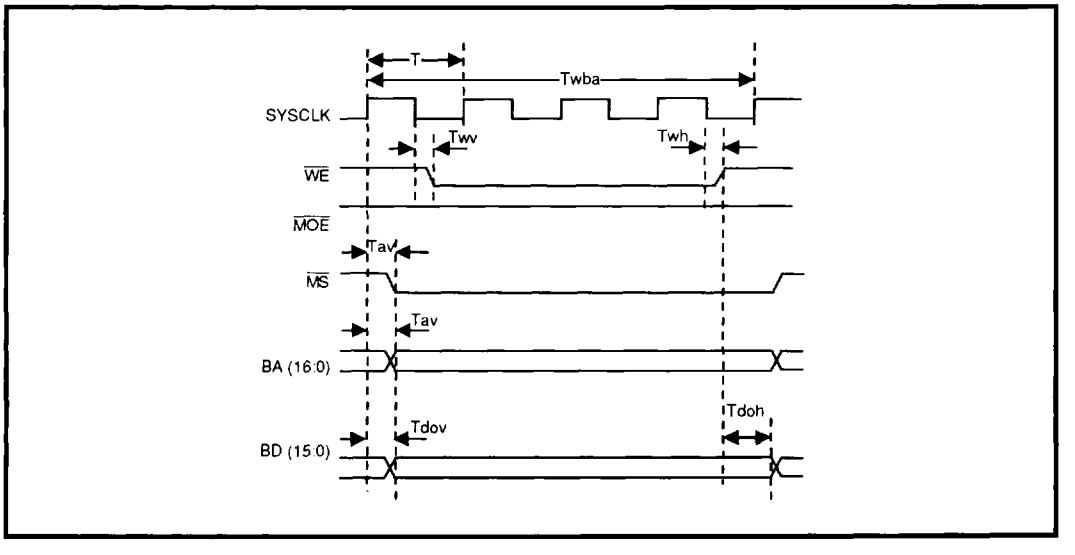

FIGURE 8: SRAM Write Timing

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ELECTRICAL SPECIFICATIONS (continued)

ATA HOST INTERFACE TIMING PARAMETERS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Cycle time	Rwcycle		120			ns
$\overline{IOR}\downarrow$ to HDB (15:0) valid	Rdta				45	ns
$\overline{IOR}\uparrow$ to HDB (15:0) invalid	Rdhld		5			ns
$\overline{IOR}\uparrow$ to HDB (15:0) tristate (PIO and single word DMA)	Rdtri				30	ns
$\overline{DACK}\uparrow$ to HDB (15:0) tristate (multiword DMA)	Dmatri				25	ns
HDB (15:0) setup to $\overline{IOW}\uparrow$	Wdset		25			ns
HDB (15:0) hold from $\overline{IOW}\uparrow$	Wdhld		5			ns
$\overline{IOR}$ or $\overline{IOW}\downarrow$ pulse width	Rwpulse		60			ns
$\overline{HCS0}$ low, A(2:0), or $\overline{HCS1}$, high to $\overline{IOCS16}$ low	Cs161				25	ns
$\overline{IOR}$ or $\overline{IOW}\downarrow$ to IOCHRDY$\downarrow$	Iochl				20	ns
HDB (15:0) valid to IOCHRDY$\downarrow$	Iochh		0			ns
$\overline{HCS0}$, A(2:0), A9$\uparrow\overline{HCS1}$, setup to $\overline{IOR}/\overline{IOW}$ low	Adrset		25			ns
$\overline{HCS0}$, A(2:0), A9$\uparrow\overline{HCS1}$ hold, from $\overline{IOR}/\overline{IOW}$ high	Adrhld		5			ns
$\overline{DACK}\downarrow$ to DREQ$\uparrow$ (single word DMA)	Dreqs				40	ns
$\overline{IOR}$ or $\overline{IOW}\downarrow$ to DREQ$\uparrow$ (multiword DMA)	Dreqm				30	ns
$\overline{DACK}\downarrow$ to $\overline{IOR}$ or $\overline{IOW}\downarrow$	Dmaset		0			ns
$\overline{IOR}$ or $\overline{IOW}\uparrow$ to $\overline{DACK}\uparrow$ (single word DMA)	Dmashld		0			ns
$\overline{IOR}$ or $\overline{IOW}\uparrow$ to $\overline{DACK}\uparrow$ (multiword DMA)	Dmamhld		5			ns
$\overline{IOR}$ or $\overline{IOW}\uparrow$ to $\overline{IOR}$ or $\overline{IOW}\downarrow$	Rwh		25			ns

Note: Loading capacitance = 30 pF

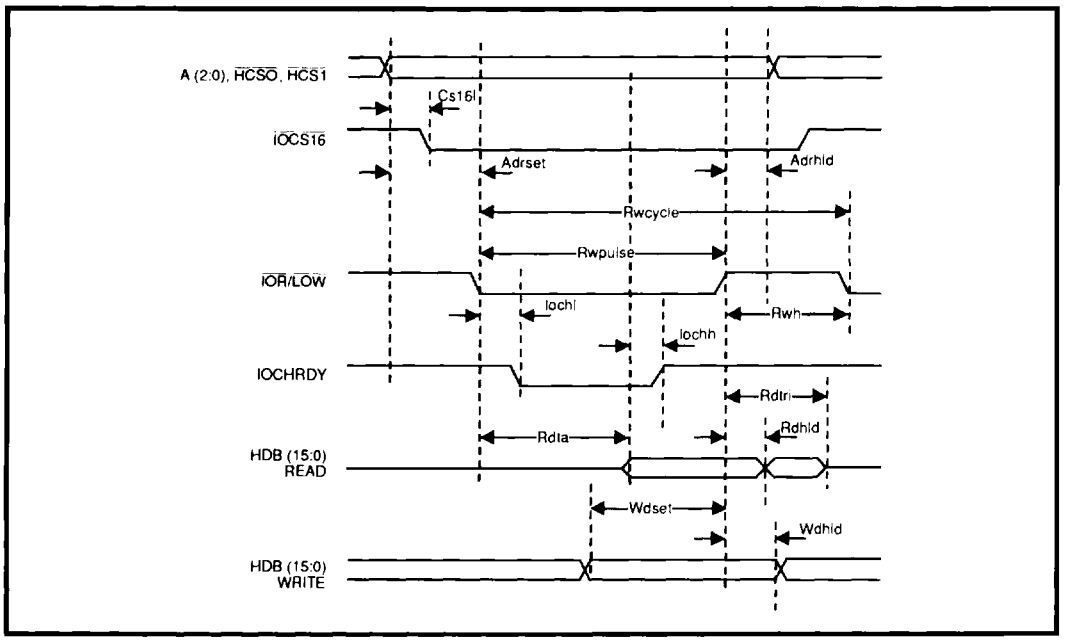

FIGURE 9: PIO Timing

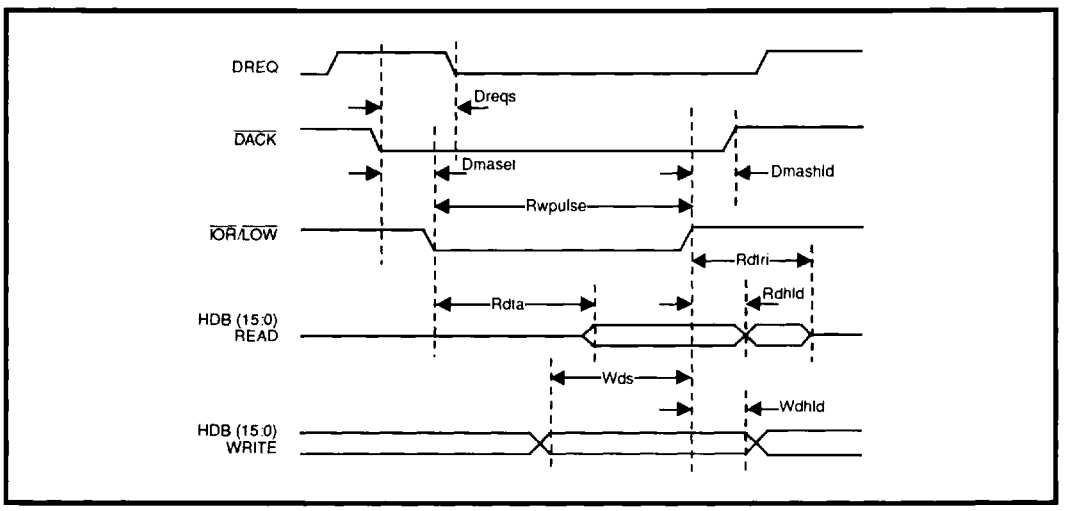

FIGURE 10: Single Word DMA Timing

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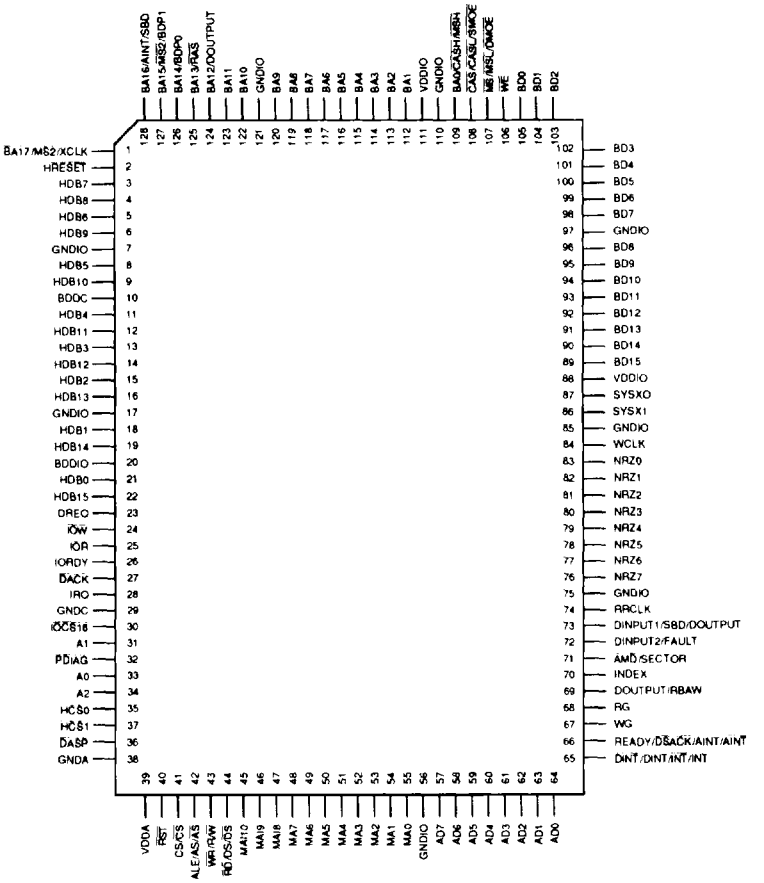
SSI 32C9600
ATA-2 Storage Controller
160 Mbit/s, 8-Bit NRZ Interface

PACKAGE PIN DESIGNATIONS

(Top View)



128-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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