HD66133T

(120-Channel HI-FAS Common Driver for Dot-Matrix Graphic LCD Display)

HITACHI

Rev 0.7
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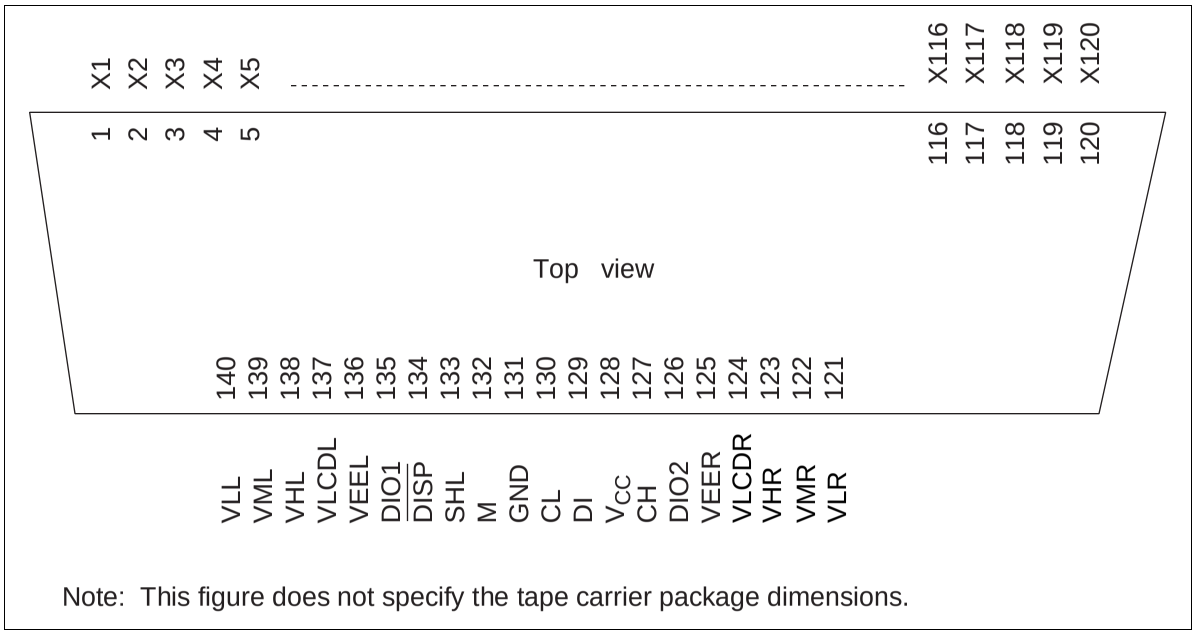
Description

The HD66133T is a 120-channel common driver, which drives a dot matrix liquid crystal graphic system with HI-FAS (high-frequency-amplitude selection). It features 120 channels which can be divided into two groups of 60 channels by selecting data input/output pins. The HD66133T, packaged in a slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area.

Features

- HI-FAS drive method
- Duty cycle: up to 1/300
- 120 LCD drive circuits
- LCD drive voltage: 75V
- Output division function (60 × 2 outputs)
- Display off function
- Operating voltage: 2.7 to 5.5V
- Slim TCP
  - Output load pitch : 190 µm
- Low output impedance: 0.5 kΩ (typ)
- Intermediate voltage I/F

Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

Figure 1 Pin Arrangement

Pin Function

Table 1 Pin Functions

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function
Power supply	VLCDL VLCDR VEEL VEER V_{CC} GND	137 124 136 125 128 131	VLCDL VLCDR VEEL VEER V_{CC} GND	—	VLCDL, VLCDR–VEEL, VEER: LCD drive power supply V_{CC}–GND: Logic power supply
	VHL VHR VLL VLR VML VMR	138 123 140 121 139 122	VHL, R VLL, R VML, R	Input	LCD drive level voltage VHL, VHR: Selection level (equivalent to VLCDL and VLCDR levels) VLL, VLR: Selection level (equivalent to VEEL and VEER levels) VML, VMR: Non-selection level
Control signal	CL	130	Clock	Input	Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input.
	M	132	M	Input	Changes the LCD drive outputs to AC.
	CH	127	CH	Input	Selects the data shift mode. (CH = low: 120-output mode, CH = high: 2 × 60-output mode)
	SHL	133	Shift left	Input	Selects the data shift direction as shown in Table 2.
	DIO1	135	Data	Input/ output	Serial input/output (shift register data input/output). This pin is used for serial input when SHL is high, and as serial output when SHL is low.
	DIO2	126	Data	Input/ output	Serial input/output (shift register data input/output). This pin is used for serial input when SHL is low, and as serial output when SHL is high.
	DI	129	Data	Input	Serial input (shift register data input). In 2 × 60-output mode, shift register data is input to pins X61 to X120 in serial when SHL is low, and to pins X1 to X60 in serial when SHL is high. This pin must be connected to GND when not used.
	$\overline{DISP}$	134	Disp off	Input	Pins X1 to X120 are set at VM levels by connecting this pin to GND.
LCD drive output	X1 to X120	1 to 120	X1 to X120	Output	One of three levels VH, VL, or VM is output according to the combination of the M signal and display data when the $\overline{DISP}$ pin is connected to V_{CC}. See Figure 2.

Table 2 Shift Register Shift Direction

SHL	Data Shift Direction
Low	Shift to right
	DIO2 → SR120 → SR119.....SR1 → DIO1
High	Shift to right
	DIO1 → SR1 → SR2 → SR2.....SR120 → DIO2

Note: SR1 to SR120 correspond to the outputs of X1 to X120, respectively.

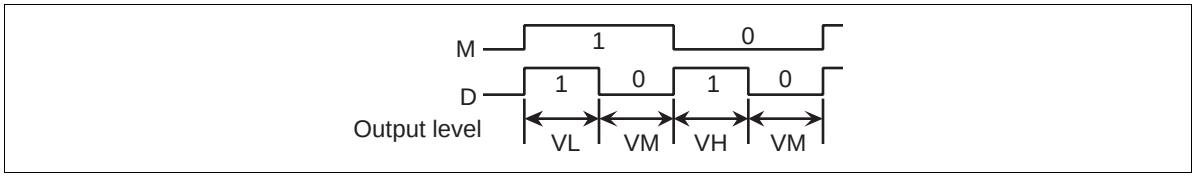


Figure 2 Selection of LCD Drive Output Level

Block Diagram

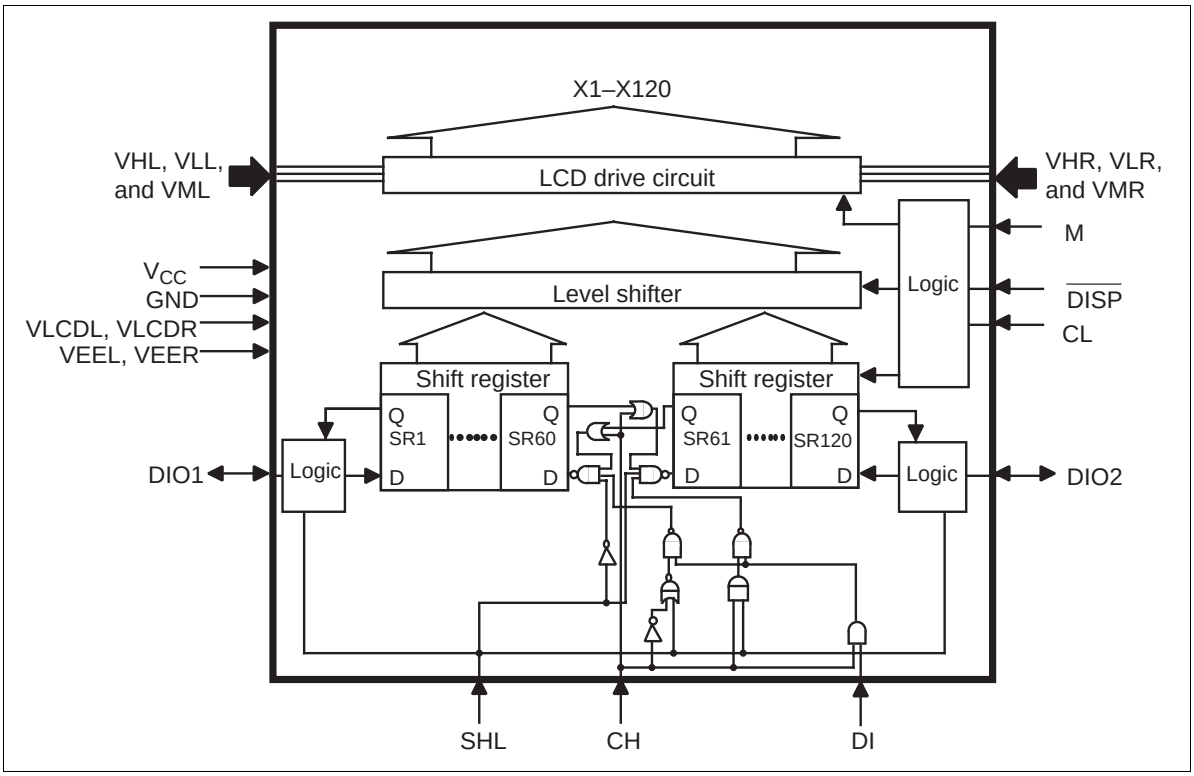


Figure 3 Block Diagram

Block Functions

LCD Drive Circuit

The 120-bit LCD drive circuit generates three voltage levels VH, VL, and VM, which drive the LCD panel. One of these three levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes logic control signal (5V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 120-bit shift register shifts the data input via the DIO pin with shift clock CL. The SHL pin selects the data shift direction.

Absolute Maximum Ratings[*1]

Item		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	2 and 7
	LCD drive circuit	VLCD	–0.3 to +40.0	V	2 and 7
		V_{EE}	–40.0 to +0.3	V	2 and 7
Input voltage (1)		VT1	–0.3 to V_{CC} + 0.3	V	2 and 3
Input voltage (2)		VT2	= VLCD	V	4
Input voltage (3)		VT3	= V_{EE}	V	5
Input voltage (4)		VT4	V_{EE} – 0.3 to VLCD + 0.3	V	6
Operating temperature		T_{opr}	–30 to +75	°C	
Storage temperature		T_{stg}	–55 to +110	°C	

Notes: 1 If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

2. The reference point is GND (0V).
3. Applies to the CL, M, SHL, DI, $\overline{DISP}$, CH, DIO1, and DIO2 pins.
4. Applies to the VH pin.
5. Applies to the VL pin.
6. Applies to the VM pin.
7. Conform to the following turn-on/off sequence of the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, the LSI reliability will be affected.

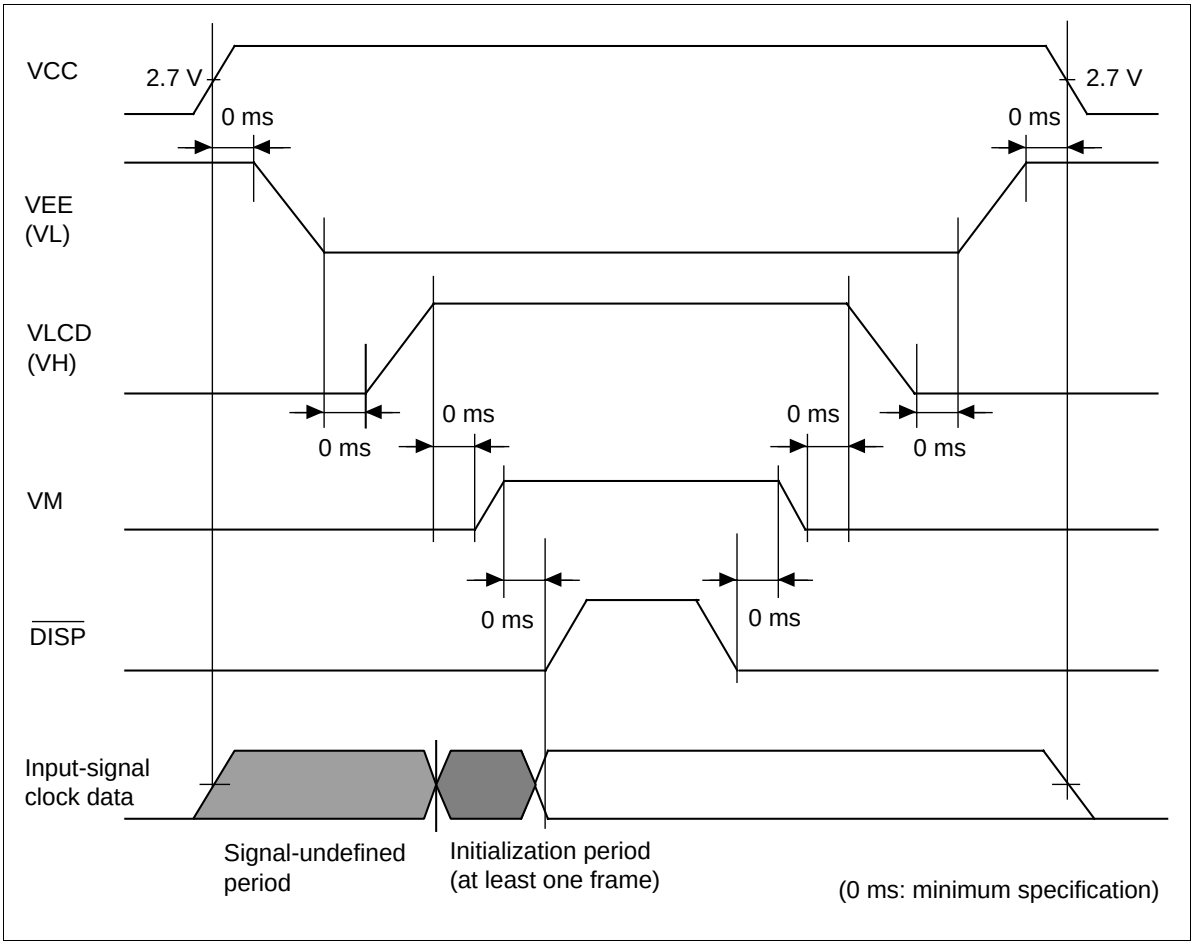


Figure 4 Power and Signal Sequence

7.1 Turning on the power

1) Turn on the power in the order of GND-VCC, GND-VEE (VL), GND-VLCD (VH), and VM. Then, ground the $\overline{DISP}$ pin.
2) The LCD forcibly outputs the VM level by the DISPOFF function.
3) Even if an input signal is disturbed immediately after VCC is applied, the DISPOFF function has priority.
4) Input the appropriate signal to initialize the registers in the driver. The initialization period must be at least one frame.
5) The preparation for normal display is completed. Apply the VCC level to the $\overline{DISP}$ pin to cancel the DISPOFF function. At this time, the level of pins VEE (VL), VLCD (VH), and VM must rise to the appropriate potential.

7.2 Turning off the power

The procedure is basically the reverse of that for turning on the power.

1) Ground the $\overline{DISP}$ pin.
2) Turn off the LCD power in the order of VM, GND-VLCD (VH), and GND-VEE (VL).
3) Ground VCC and the input signal.

   At this time, the level of pins VEE (VL), VLCD (VH), and VM must fall to 0 V. Since the DISPOFF function stops when VCC falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.7 to 5.5V, GND = 0V, VLCD–V_{EE} = 40 to 75V, and Ta = –30 to + 75 °C, unless otherwise stated)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Note
Input high level voltage	VIH	CL, M, SHL, CH, DI, DIO1, DIO2, and $\overline{DISP}$	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage	VIL		0	—	$0.3 \times V_{CC}$	V		
Output high level voltage	VOH	DIO1 and DIO2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	VOL	DIO1 and DIO2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Xj ON resistance	RON	X1 to X120, and V	—	0.5	1.0	kΩ	I_{ON} = 150 µA	1
Input leakage current (1)	I_{IL1}	CL, M, SHL, CH, DI, DIO1, DIO2, and $\overline{DISP}$	–5	—	5	µA	VIN = V_{CC} to GND	
Input leakage current (2)	I_{IL2}	VH, VL, and VM	–25	—	25	µA		
Current consumption	I_{CC}	V_{CC}	—	0.1	0.5	mV	f_{CL} = 160 kHz f_M = 6 kHz	2
Current consumption	I_{LCD}	VLCD	—	1.5	2.0	mA		

Notes: 1 Indicates the resistance between one of the pins X1–X120 and one of the voltage supply pins VH, VL, or VM, when load current is applied to the X pin; defined under the following conditions: VLCD = VH = 36.0V, V_{EE} = VL = –30.0V, VM = 3V, and GND = 0V.
VH, VL, and VM voltages must be within VLCD = VH = 23 to 40.5V, V_{EE} = VL = –17 to –34.5V, and 9V > VM > –4V.

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, ViH and ViL must be held at V_{CC} and GND, respectively.
3. The voltage of each signal is shown in figure 5.

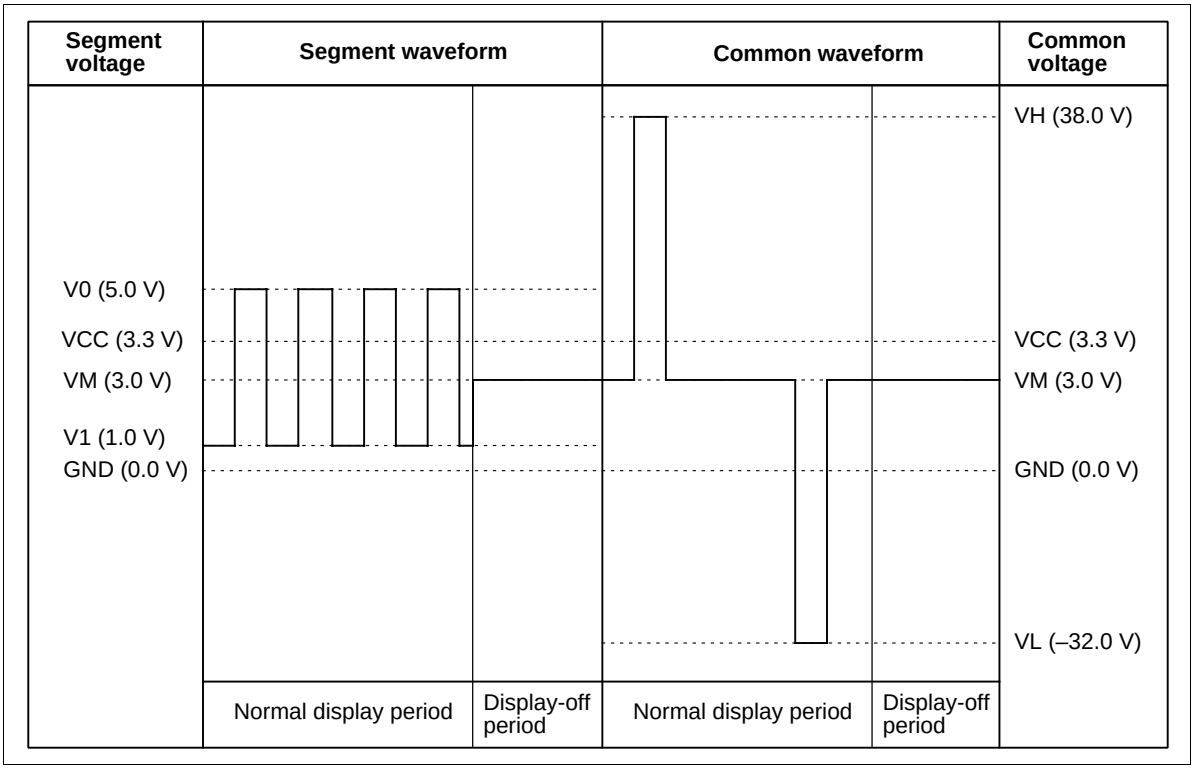


Figure 5 Signal Voltages

AC Characteristics (common driver timing 1) (V_{CC} = 2.7 to 5.5V, GND = 0V, and Ta = –30 to +75 °C)

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high level width	t_{CWH}	CL	30	—	ns	
Clock low level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, and CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, and CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, and CL	—	350	ns	1
Output delay time (1)	t_{pd1}	X (n) and CL	—	1.2	µs	2
Output delay time (2)	t_{pd2}	X (n) and M	—	1.2	µs	2

Notes: 1. Defined by connecting the load circuit in Figure 6.
2. Defined by connecting the load circuit in Figure 6.

AC Characteristics (common driver timing 2) (V_{CC} = 5.0V ± 10%, GND = 0V, and Ta = –30 to +75 °C)

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high level width	t_{CWH}	CL	30	—	ns	
Clock low level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, and CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, and CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, and CL	—	150	ns	1
Output delay time (1)	t_{pd1}	X (n) and CL	—	0.7	µs	2
Output delay time (2)	t_{pd2}	X (n) and M	—	0.7	µs	2

Notes: 1. Defined by connecting the load circuit shown in Figure 6.
2. Defined by connecting the load circuit shown in Figure 6.

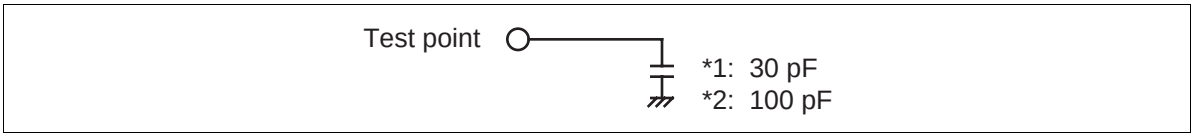


Figure 6 Load Circuit

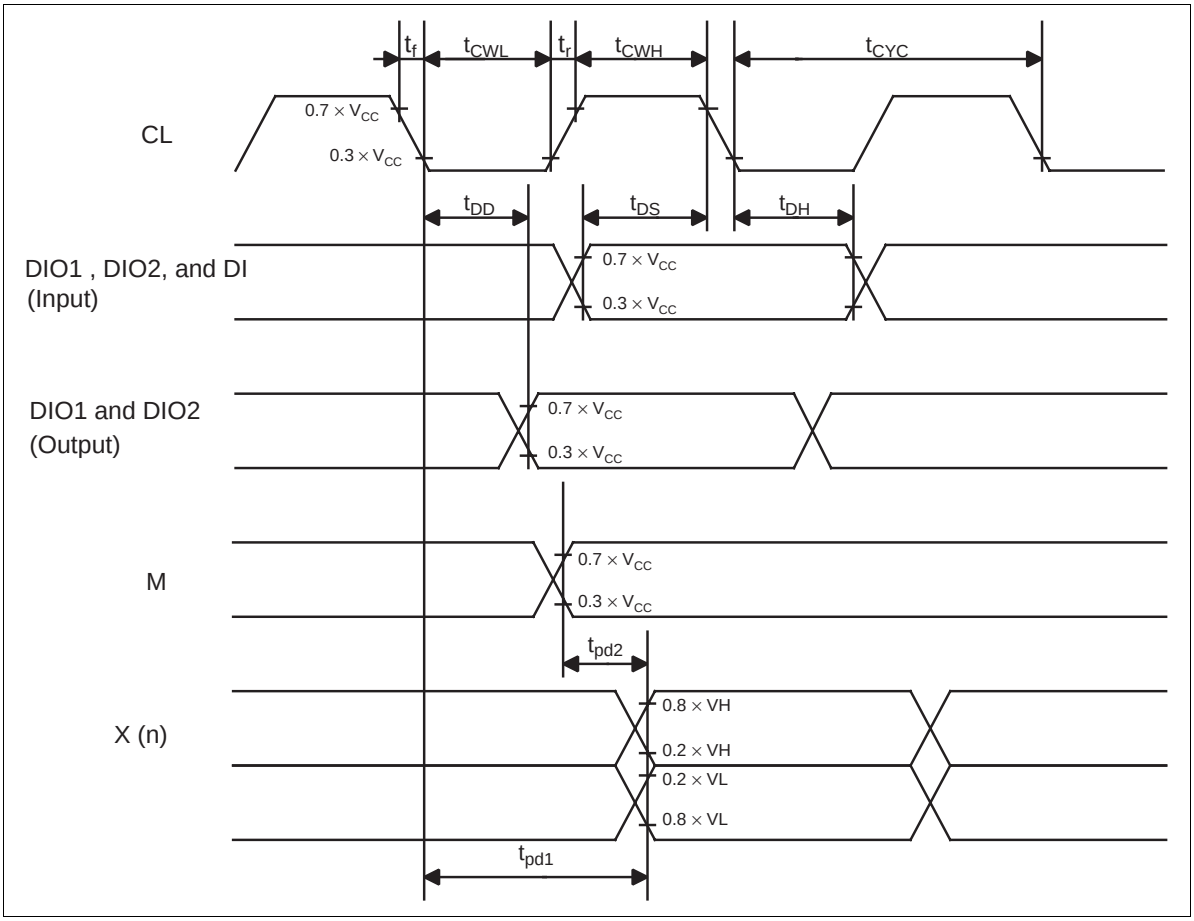


Figure 7 AC Characteristics