

MOS INTEGRATED CIRCUIT
 μ PD6901

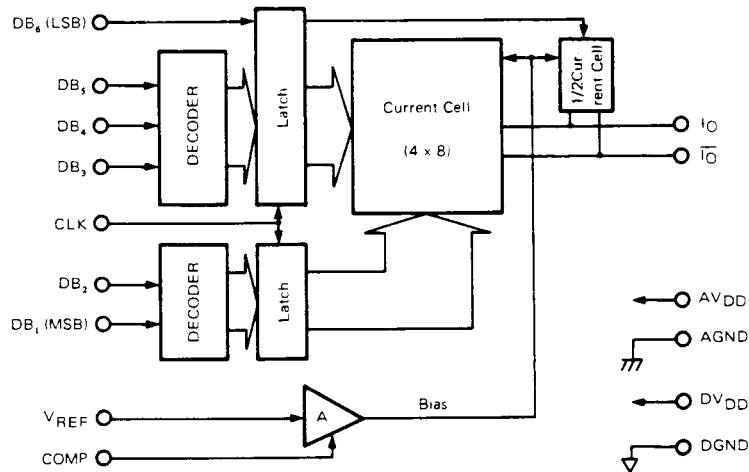
6 BIT D/A CONVERTER FOR VIDEO SIGNAL PROCESSING
CMOS LSI

The μ PD6901 is an 6 bit D/A converter for use in video applications. The high-speed CMOS processing technology and the matrix current cell method adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 20 Msp/s can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and video systems. ★

FEATURES

- Resolution : 6 bits
- Conversion rate : 20 Msp/s
- Linearity : $\pm 1/2$ LSB MAX.
- Reference voltage : 2.0 V TYP.
- Power supply voltage : +5 V single
- Low power consumption (110 mW TYP.)
- TTL compatible (Digital inputs)
- 16 pin plastic DIP, and 16 pin plastic SOP (375 mil)

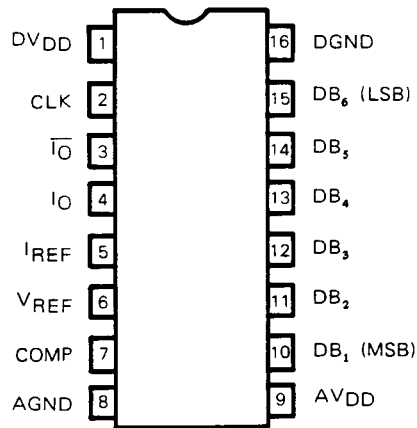
BLOCK DIAGRAM



ORDERING INFORMATION

Ordering Name	Package
μ PD6901C	16 pin plastic DIP (300 mil)
μ PD6901G	16 pin plastic SOP (375 mil)

CONNECTION DIAGRAM (Top View)



- | | | |
|----|------------------|-------------------------------|
| 1 | DVDD | Digital power supply |
| 2 | CLK | Sampling clock input |
| 3 | $\overline{I_O}$ | Complementary current output |
| 4 | I _O | Current output |
| 5 | I _{REF} | Full-scale current adjustment |
| 6 | V _{REF} | Reference voltage input |
| 7 | COMP | Amp compensation |
| 8 | AGND | Analog GND |
| 9 | AVDD | Analog power supply |
| 10 | DB ₁ | Digital input (MSB) |
| 11 | DB ₂ | Digital input (2nd) |
| 12 | DB ₃ | Digital input (3rd) |
| 13 | DB ₄ | Digital input (4th) |
| 14 | DB ₅ | Digital input (5th) |
| 15 | DB ₆ | Digital input (LSB) |
| 16 | DGND | Digital GND |

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power supply voltage	-0.3 to +7.0	V
Input terminal voltage	-0.3 to V _{DD} +0.3	V
Output terminal voltage	-0.3 to V _{DD} +0.3	V
Analog power supply voltage	DV _{DD} -0.3 to DV _{DD} +0.3	V
Analog GND voltage	DGND-0.3 to DGND+0.3	V
Operating temperature range	-20 to +75	°C
Storage temperature range	-40 to +125	°C

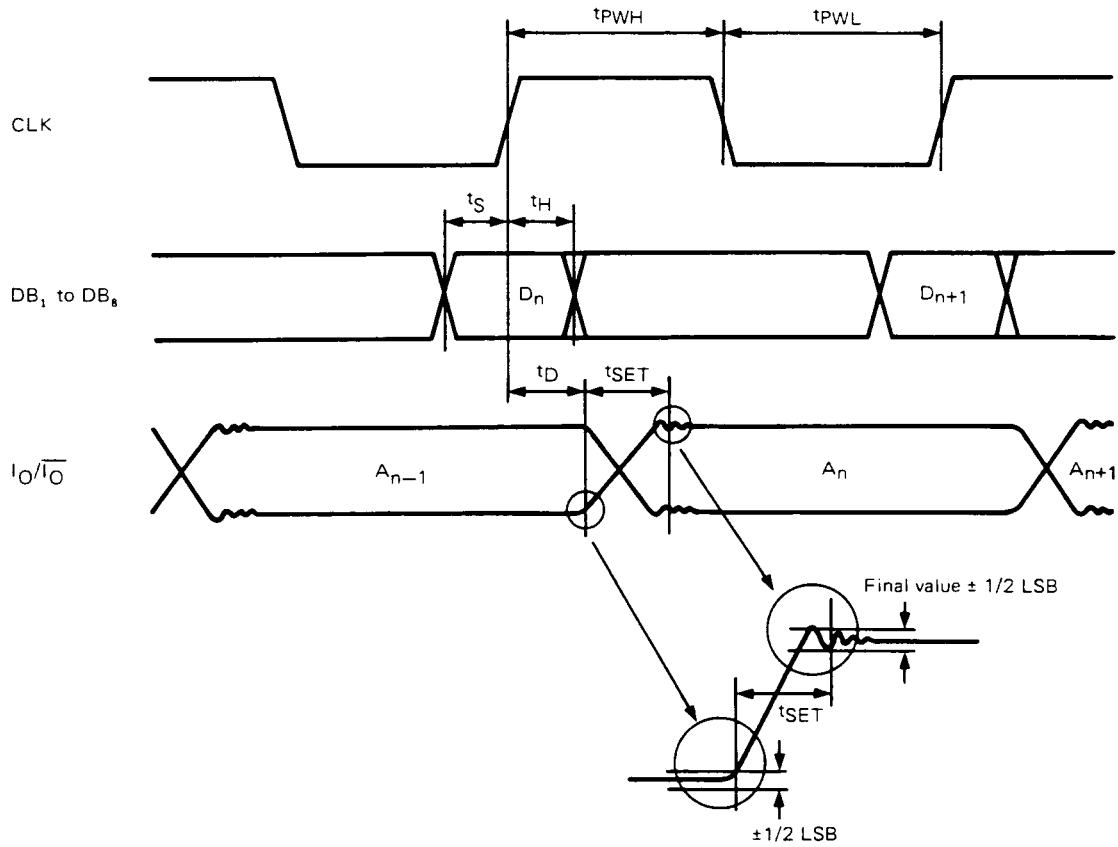
RECOMMENDED OPERATING CONDITIONS (T_a = -20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	V _{DD}	4.5	5.0	5.5	V	
Reference voltage	V _{REF}	1.8	2.0	2.2	V	
Reference resistance	R _{REF}		390		Ω	
Sampling clock	f _{samp}	DC		20	MHz	
Sampling clock low level pulse width	t _{PWL}	15			ns	
Sampling clock high level pulse width	t _{PWH}	15			ns	
Data set up time	t _S	20			ns	
Data hold time	t _H	10			ns	
Digital input high level	V _{IH}	2.7			V	
Digital input low level	V _{IL}			0.6	V	
Compensation capacity	C _{COMP}	0.01	1.0		μF	

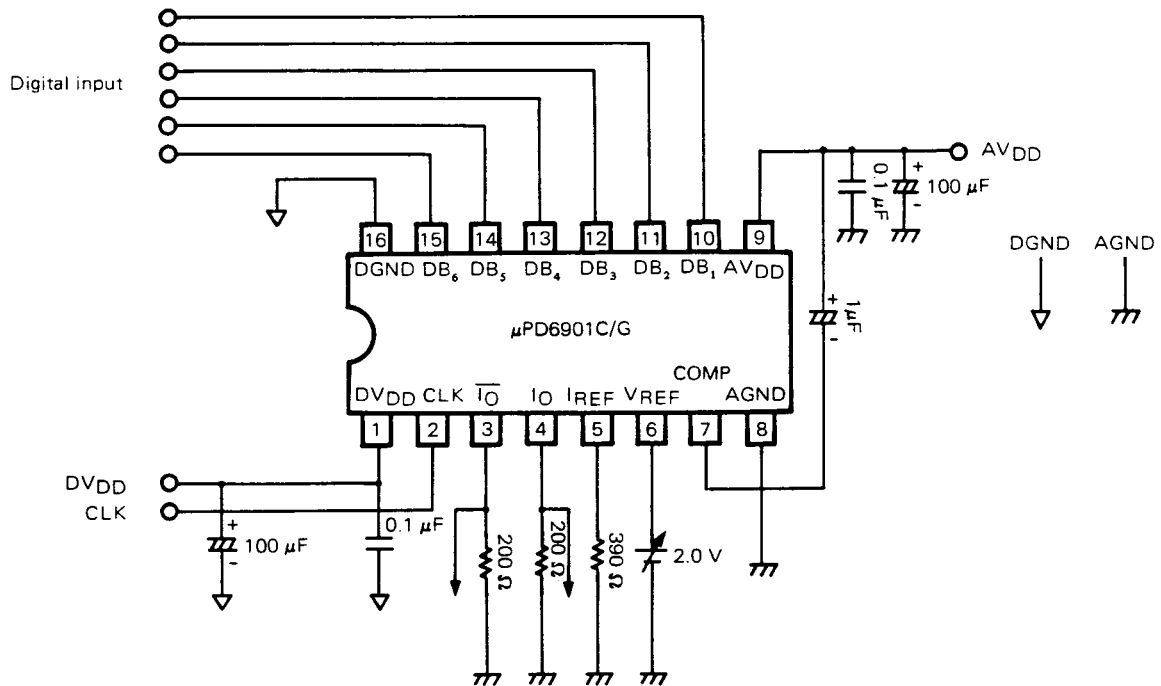
ELECTRICAL CHARACTERISTICS (T_a = -20 to +75 °C, V_{DD} = 5 V ± 0.5 V, f_{samp} = 20 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power supply current	I _{DD}		22	50	mA	V _{DD} = 5.0 V
Resolution	RES		6		bit	
Non-linearity error	NL		±0.11	±0.5	LSB	T _a = 0 to 60°C, V _{DD} = 5 V ± 0.25 V
Differential non-linearity	DNL		±0.04	±0.5	LSB	T _a = 0 to 60°C, V _{DD} = 5 V ± 0.25 V
Output compliance	V _O	2.5	3.0		V	V _{DD} = 5.0 V
Analog output delay time	t _D		40		ns	
Settling time	t _{SET}		40		ns	
Full-scale current	I _{FS}	9	10	11	mA	V _{REF} =2.0 V, R _{REF} =390 Ω
Zero-scale offset current	I _{ZS}			20	μA	V _{REF} =2.0 V, R _{REF} =390 Ω
Digital input capacitance	C _{DI}		10	20	pF	
Digital input current	I _I			10	μA	

TIMING CHART



TEST CIRCUIT



PIN DESCRIPTIONS

DGND (Pin 16)	Digital system ground
AGND (Pin 8)	Analog system ground
DVDD (Pin 1)	Digital system power supply (+5 V)
AVDD (Pin 9)	Analog system power supply (+5 V)

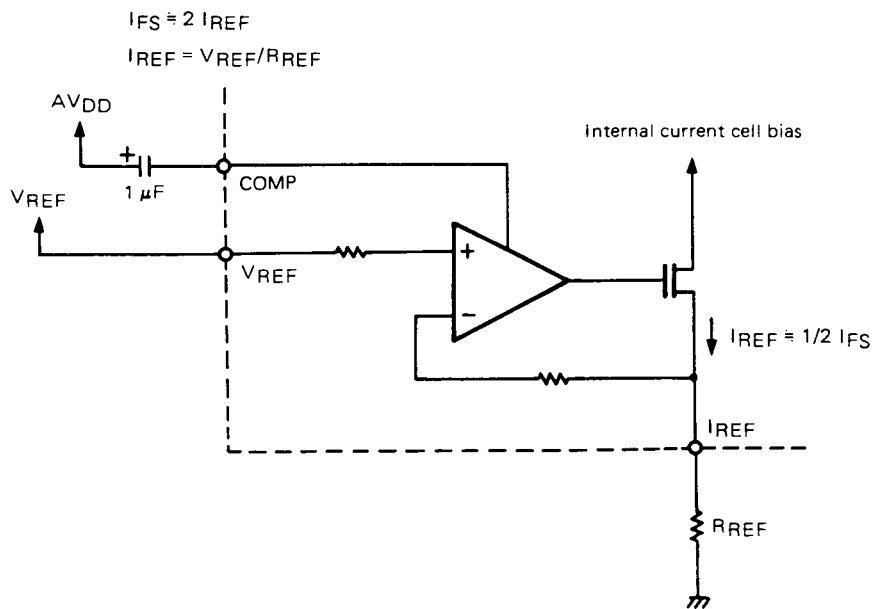
The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

Insert by-pass capacitors of about 0.01 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible, to the μPD6901C pins. Supply the digital system power from the analog power line through the low path filter to prevent from lurch up.

I _{REF} (Pin 5)	Full-scale current adjustment pin
V _{REF} (Pin 6)	Reference voltage input pin

These pins are used in adjustment of the analog output current (full-scale current).

The analog output current (full-scale current I_{FS}) is set by the reference voltage V_{REF} and the reference resistance R_{REF} connected between the I_{REF} pin and analog ground.



The recommended reference voltage and reference resistance values are V_{REF} = 2.0 V and R_{REF} = 390 Ω respectively. The output analog current I_{FS} in this case will be 10 mA. Also connect by-pass capacitors of about 0.01 μF and 47 μF between the V_{REF} pin and GND in the same way as the by-pass capacitors connected to the power pins.

COMP (Pin 7)	Phase compensation capacitor connection
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A capacitor for phase compensation of the internal amplifier is connected to this pin. Connect a 1.0 μF capacitor between this pin and analog V_{DD}.

DB₁ to DB₆ (Pins 10 thru 15) Digital data input pins

DB₁ to DB₆ are the 6 bit digital data input pins. The code format is binary, and the input voltage level is TTL compatible.

Digital input code						Analog output current
DB ₁ (MSB)	DB ₂	DB ₃	DB ₄	DB ₅	DB ₆ (LSB)	
0	0	0	0	0	0	0 note
0	0	0	0	0	1	1/64 I _{FS}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	61/64 I _{FS}
1	1	1	1	1	0	62/64 I _{FS}
1	1	1	1	1	1	63/64 I _{FS}

Note: Excluding offset current

Digital data (DB₁ to DB₆) is latched by the rising edge of the sampling clock, and converted to corresponding analog outputs.

CLK (Pin 2) Sampling clock input pin

Digital data is latched by the rising edge of the clock signal applied to the sampling clock input pin, and is subsequently converted to analog outputs. The maximum clock frequency is 20 MHz.

I_O (Pin 4) Analog signal output pin

\overline{I}_O (Pin 3) Analog signal complementary output pin

These two pins are current output pins. The full-scale output current is determined by the reference resistance R_{REF} and reference voltage V_{REF}.

$$I_{FS} = I_O + \overline{I}_O = 2 V_{REF}/R_{REF}$$

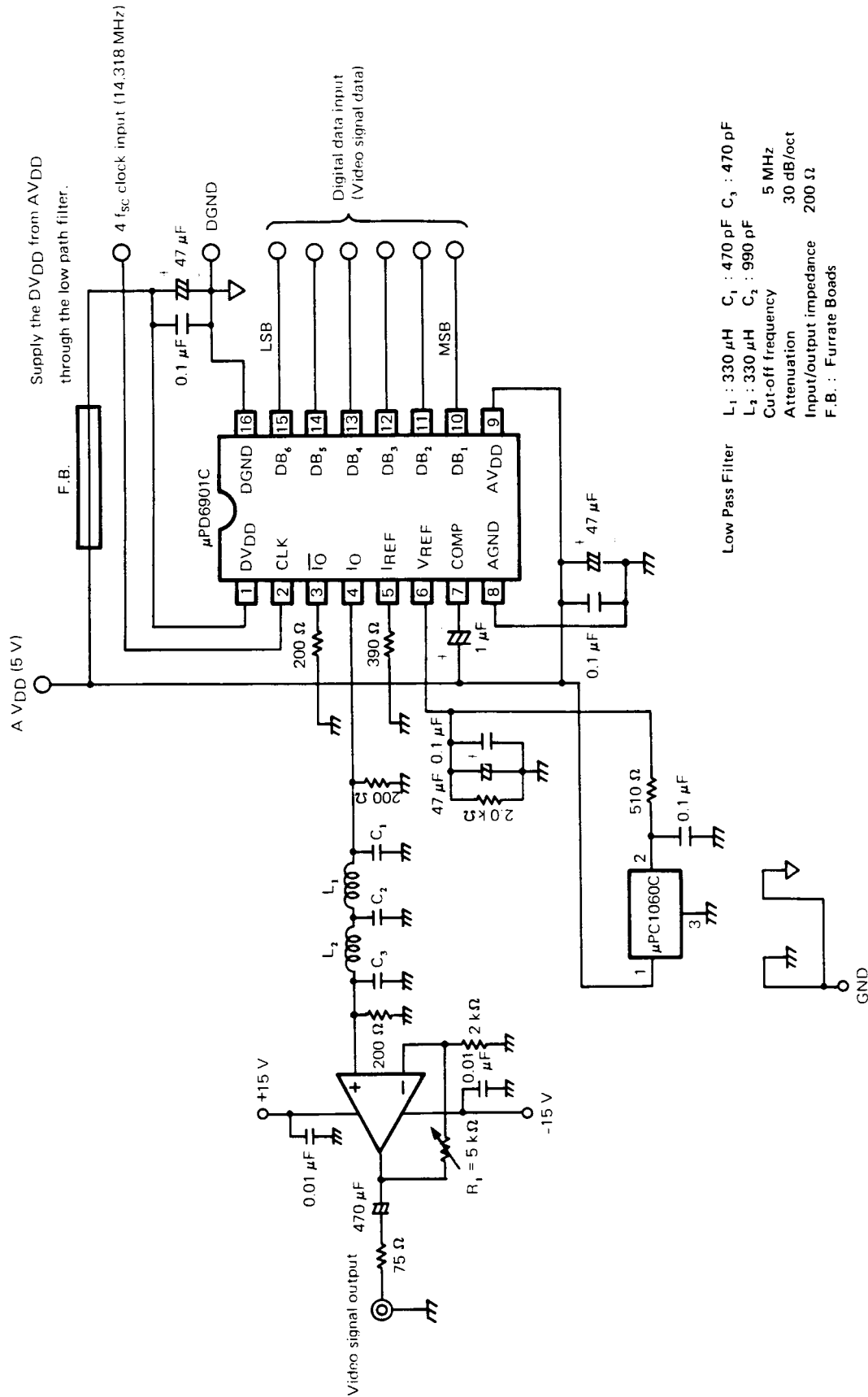
\overline{I}_O is the complementary output pin of I_O. The added output current from the I_O and \overline{I}_O pins becomes the full-scale current in accordance with the above equation. Analog output current can be easily converted to an analog output voltage by connecting a resistance between the I_O or \overline{I}_O pin and analog ground. In this case resistances must also be connected to the I_O and \overline{I}_O pins.

Example of an Application Circuit

This example shows D/A conversion of video signal (NTSC) digital data at a conversion rate of four times the subcarrier frequency (4 f_{sc}) to obtain the video output signal.

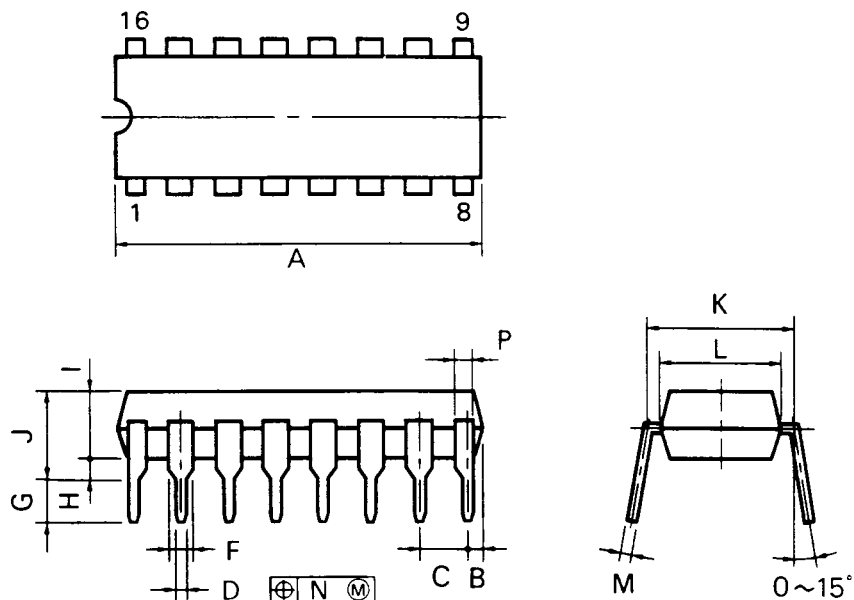
The analog output signal is passed via a low-pass filter (LPF) to a video amplifier to be amplified prior to output.

APPLICATION CIRCUIT



NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.
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16PIN PLASTIC DIP (300 mil)



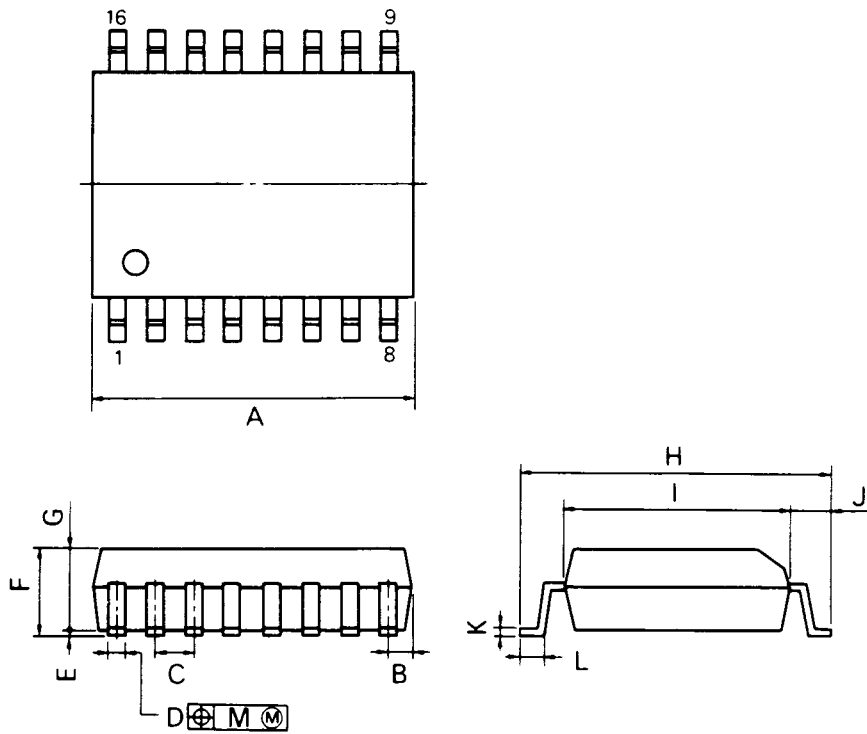
P16C-100-300B

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± ⁰ _{0.10}	0.020 ^{-0.0004} _{-0.0005}
F	1.1 MIN.	0.043 MIN.
G	3.5 ± ⁰ _{0.3}	0.138 ± ⁰ _{0.012}
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	0.25 ^{-0.10} _{-0.08}	0.010 ^{-0.0004} _{-0.0003}
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16 PIN PLASTIC SOP (375 mil)



P16GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.08}	0.016 ^{+0.004} _{-0.003}
E	0.1 ^{+0.2} _{-0.1}	0.004 ^{+0.008} _{-0.004}
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ^{+0.3}	0.406 ^{+0.012} _{-0.013}
I	7.2	0.283
J	1.6	0.063
K	0.15 ^{+0.10} _{-0.08}	0.006 ^{+0.004} _{-0.002}
L	0.8 ^{+0.2}	0.031 ^{+0.008} _{-0.008}
M	0.12	0.005