

**FEATURES**

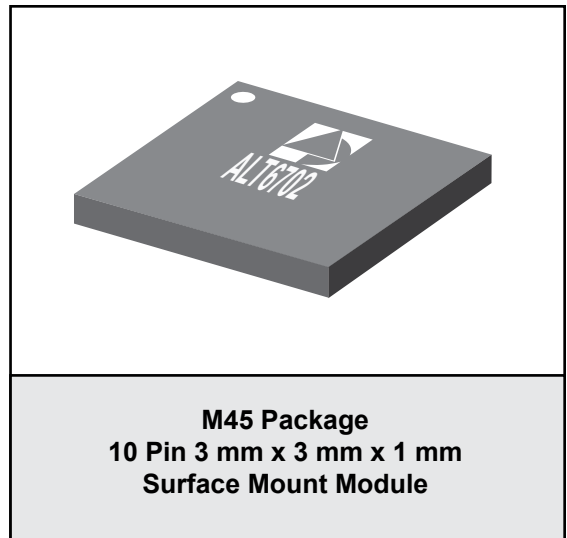
- Mixed-Mode HSPA, EVDO, LTE Compliant
- 4th Generation HELP™ technology
- High Efficiency (R99 waveform):
  - 39 % @ P<sub>OUT</sub> = +28.6 dBm
  - 35 % @ P<sub>OUT</sub> = +17.5 dBm
  - 23 % @ P<sub>OUT</sub> = +13.5 dBm
  - 26 % @ P<sub>OUT</sub> = +9 dBm
  - 13 % @ P<sub>OUT</sub> = +3.5 dBm
- Low Quiescent Current: 2 mA
- Low Leakage Current in Shutdown Mode: <5  $\mu$ A
- Internal Voltage Regulator
- Integrated “daisy chainable” directional coupler with CPL<sub>IN</sub> and CPL<sub>OUT</sub> port
- Internal DC blocks on RF IN/OUT ports
- Optimized for a 50  $\Omega$  System
- 1.8 V Control Logic
- RoHS Compliant Package, 260 °C MSL-3

**APPLICATIONS**

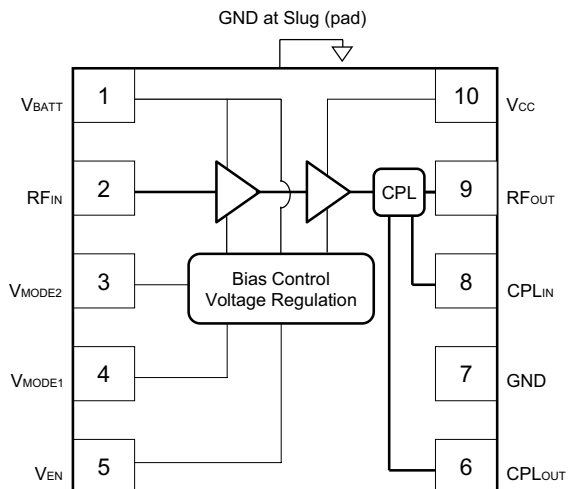
- Band 2 WCDMA/HSPA Wireless Devices
- Band 2 LTE Wireless Devices
- Band Class 1 and 14 CDMA/EVDO Wireless Devices
- Band 25 LTE Devices

**PRODUCT DESCRIPTION**

The ALT6702 HELP4™ PA is a 4th generation HELP™ product for LTE and WCDMA devices operating in UMTS PCS (Band 2) and for CDMA devices operating in Band Class 1 and Band Class 14. This PA incorporates ANADIGICS’ HELP4™ technology to deliver exceptional efficiency at low power levels and low quiescent current without the need for external voltage regulators or converters. The device is manufactured using advanced InGaP-Plus™ HBT technology offering state-of-the-art reliability, temperature stability, and ruggedness. Three selectable bias modes that optimize efficiency for different output power levels and a shutdown



mode with low leakage current increase handset talk and standby time. A “daisy chainable” directional coupler is integrated in the module, thus eliminating the need of an external coupler. The self-contained 3 mm x 3 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50  $\Omega$  system.


**Figure 1: Block Diagram**

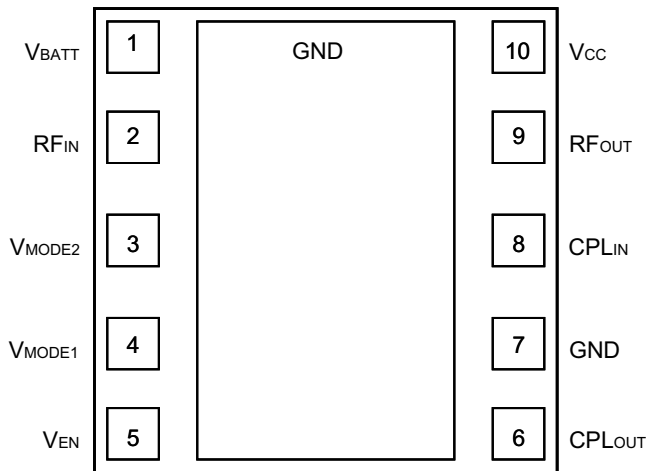


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V <sub>BATT</sub>	Battery Voltage
2	RF <sub>IN</sub>	RF Input
3	V <sub>MODE2</sub>	Mode Control Voltage 2
4	V <sub>MODE1</sub>	Mode Control Voltage 1
5	V <sub>EN</sub>	PA Enable Voltage
6	CPL <sub>OUT</sub>	Coupler Output
7	GND	Ground
8	CPL <sub>IN</sub>	Coupler Input
9	RF <sub>OUT</sub>	RF Output
10	V <sub>CC</sub>	Supply Voltage

## ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage ( $V_{CC}$ )	0	+5	V
Battery Voltage ( $V_{BATT}$ )	0	+6	V
Control Voltages ( $V_{MODE1}$ , $V_{MODE2}$ , $V_{EN}$ )	0	+3.5	V
RF Input Power ( $P_{IN}$ )	-	+10	dBm
Storage Temperature ( $T_{STG}$ )	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	1850	-	1915	MHz	
Supply Voltage ( $V_{CC}$ )	+3.1	+3.4	+4.35	V	$P_{OUT} < +28.6$ dBm
Enable Voltage ( $V_{EN}$ )	+1.35 0	+1.8 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage ( $V_{MODE1}$ , $V_{MODE2}$ )	+1.35 0	+1.8 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
WCDMA / UMTS Output Power <sup>(1, 3)</sup> R99, HPM HSPA (MPR=0), HPM LTE <sup>(2)</sup> R99, MPM LTE <sup>(2)</sup> & HSPA (MPR=0), MPM R99, LPM LTE <sup>(2)</sup> & HSPA (MPR=0), LPM	27.8 26.8 26.6 - - - -	28.6 27.6 27.4 17.5 16.5 9.0 8.0	- - - - - -	dBm	3GPP TS 34.121-1, Rel 8 Table C.11.1.3 for WCDMA, SUBTEST 1 TS 36.101 Rel 8 for LTE
CDMA Output Power <sup>(1, 3)</sup> HPM MPM LPM	27.2 - -	28.0 16.5 8.0	- - -	dBm	CDMA2000, RC-1
Case Temperature ( $T_C$ )	-40	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) For Operation at 3.1 V,  $P_{OUT}$  is derated by 0.8 dB.

(2) LTE Waveform: Up to 20 MHz, 18 RB's, QPSK.

(3) For Operation at +105 °C,  $P_{OUT}$  is derated by 1.0 dB.

**Table 4: Electrical Specifications - LTE Operation = 10 MHz QPSK 12 RB (Start = 0)**  
**(T<sub>C</sub> = +25 °C, V<sub>BATT</sub> = V<sub>CC</sub> = +3.4 V, V<sub>ENABLE</sub> = +1.8 V, 50 Ω system)**

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P <sub>OUT</sub>	V <sub>MODE1</sub>	V <sub>MODE2</sub>
Gain	25 16 8	27.5 19 10.5	30 22 13	dB	P <sub>OUT</sub> = +27.4 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR E-UTRA at ± 10 MHz offset	- - -	-39 -39 -40	-34 -34 -34	dBc	P <sub>OUT</sub> = +27.4 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR UTRA at ± 7.5 MHz offset	- - -	-39 -40 -40	-36 -36 -36	dBc	P <sub>OUT</sub> = +27.4 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR UTRA at ± 12.5 MHz offset	- - -	-59 -59 -60	-40 -40 -40	dBc	P <sub>OUT</sub> = +27.4 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency	31 26 19	34 30 23	- - -	%	P <sub>OUT</sub> = +27.4 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (I <sub>cq</sub> ) Low Bias Mode	-	2	3.5	mA	through V <sub>CC</sub> pin	1.8 V	1.8 V
Mode Control Current	-	0.08	0.15	mA	through V <sub>MODE</sub> pins, V <sub>MODE1,2</sub> = +1.8 V		
Enable Current	-	0.04	0.1	mA	through V <sub>EN</sub> pin, V <sub>EN</sub> = +1.8 V		
BATT Current	-	0.8	1.5	mA	through V <sub>BATT</sub> pin, V <sub>MODE1,2</sub> = +1.8 V		
Leakage Current	-	<5	8	μA	V <sub>BATT</sub> = V <sub>CC</sub> = +4.35 V V <sub>EN</sub> = 0 V, V <sub>MODE1,2</sub> = 0 V		
Noise Power	- - -	-135 -135 -146	-133 - -	dBm/Hz	1930 MHz to 1990 MHz GPS Band ISM Band		
Harmonics 2fo 3fo, 4fo	- - -	-44 -50	-35 -42	dBc	P <sub>OUT</sub> ≤ +27.4 dBm		
Coupling Factor	-	20	-	dB			
Directivity	-	20	-	dB			
Coupler In_Out Daisy Chain Insertion Loss	-	<0.25	-	dB	698 Mhz to 2620 MHz Pin 8 to 9, Shutdown Mode		
Spurious Output Level (all spurious outputs)	-	-	<-70	dBc	P <sub>OUT</sub> < +27.4 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating ranges		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

## Notes:

1. ACLR and Efficiency are measured at 1880 MHz.

**Table 5: Electrical Specifications - WCDMA Operation (R99 waveform)**  
**(T<sub>C</sub> = +25 °C, V<sub>CC</sub> = +3.4 V, V<sub>BATT</sub> = +3.4 V, V<sub>EN</sub> = +1.8 V, 50 Ω system)**

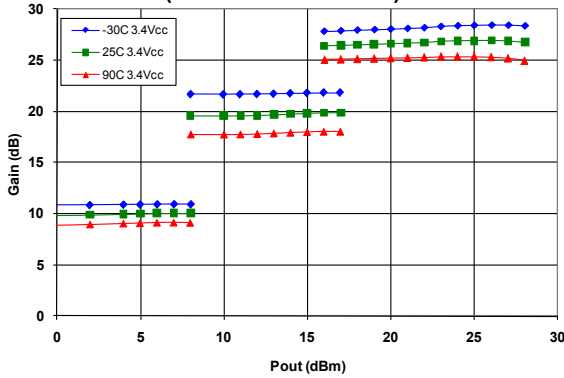
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P <sub>OUT</sub>	V <sub>MODE1</sub>	V <sub>MODE2</sub>
Gain	25 16 8	27.5 19 10.5	30 22 13	dB	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17.5 dBm P <sub>OUT</sub> = +9 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR1 at 5 MHz offset	- - -	-41 -43 -43	-37.5 -37.5 -37.5	dBc	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17.5 dBm P <sub>OUT</sub> = +9 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR2 at 10 MHz offset	- - -	-54 -55 -59	-48 -48 -48	dBc	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17.5 dBm P <sub>OUT</sub> = +9 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency	35 31 - 22 -	39 35 23 26 13	- - - - -	%	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17.5 dBm P <sub>OUT</sub> = +13.5 dBm P <sub>OUT</sub> = +9 dBm P <sub>OUT</sub> = +3.5 dBm	0 V 1.8 V 1.8 V 1.8 V 1.8 V	0 V 0 V 0 V 1.8 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P <sub>OUT</sub> < +28.6 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

**Table 6: Electrical Specifications - CDMA Operation (CDMA2000, RC-1)**  
**(T<sub>C</sub> = +25 °C, V<sub>BATT</sub> = V<sub>CC</sub> = +3.4 V, V<sub>ENABLE</sub> = +1.8 V, 50 Ω system)**

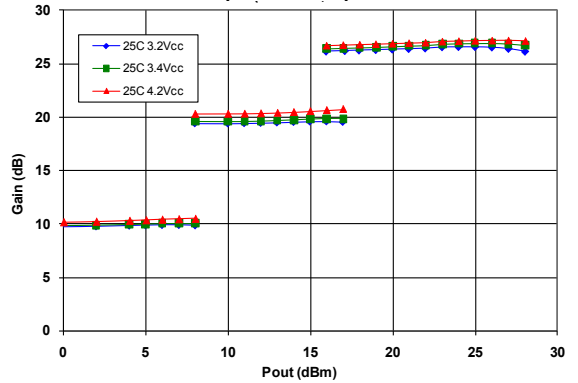
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P <sub>OUT</sub>	V <sub>MODE1</sub>	V <sub>MODE2</sub>
Gain	25 16 8	27.5 19 10.5	30 22 13	dB	P <sub>OUT</sub> = +28 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 1.25 MHz offset Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-50 -56 -57	-46.5 -46.5 -46.5	dBc	P <sub>OUT</sub> = +28 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 1.98 MHz offset Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-56 <-60 <-60	-53 -53 -53	dBc	P <sub>OUT</sub> = +28 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency	33 27 18	37 31 22	- - -	%	P <sub>OUT</sub> = +28 dBm P <sub>OUT</sub> = +16.5 dBm P <sub>OUT</sub> = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P <sub>OUT</sub> < +28 dBm, In-Band VSWR <5:1, Out-Of-Band VSWR <10:1 Applies to all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

**PERFORMANCE DATA PLOTS:  
(LTE Operation at 1880 MHz and 50 Ω system)**

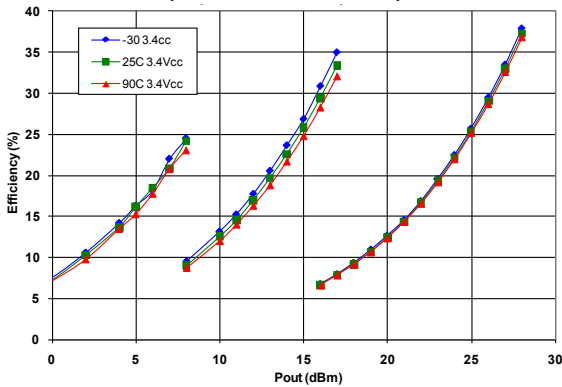
**Figure 3: LTE Gain (dB) over Temperature**  
( $V_{BATT} = V_{CC} = +3.4\text{ V}$ )



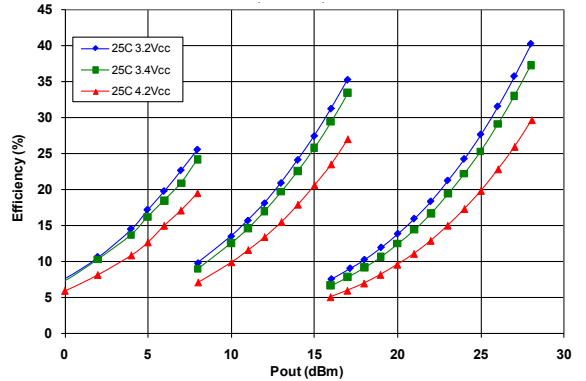
**Figure 4: LTE Gain (dB) over Voltage**  
( $T_c = 25\text{ °C}$ )



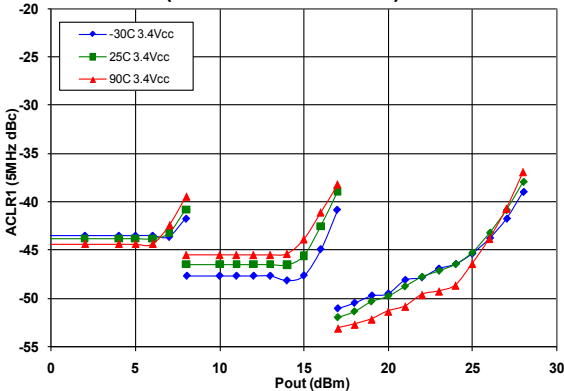
**Figure 5: LTE PAE (%) over Temperature**  
( $V_{BATT} = V_{CC} = +3.4\text{ V}$ )



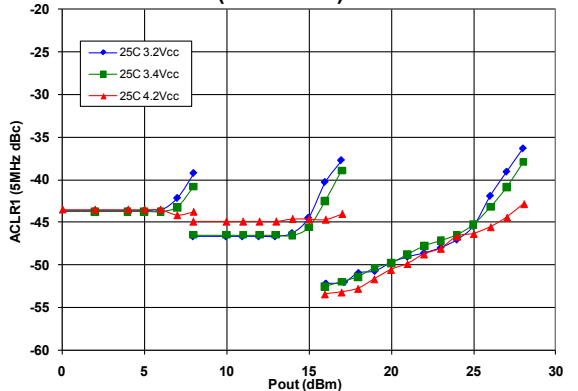
**Figure 6: LTE PAE (%) over Voltage**  
( $T_c = 25\text{ °C}$ )



**Figure 7: LTE ACLR1 (dBc) over Temperature**  
( $V_{BATT} = V_{CC} = +3.4\text{ V}$ )



**Figure 8: LTE ACLR1 (dBc) over Voltage**  
( $T_c = 25\text{ °C}$ )



**APPLICATION INFORMATION**

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: <http://www.anadigics.com>

**Shutdown Mode**

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the  $V_{EN}$ ,  $V_{MODE1}$  and  $V_{MODE2}$  voltages.

**Bias Modes**

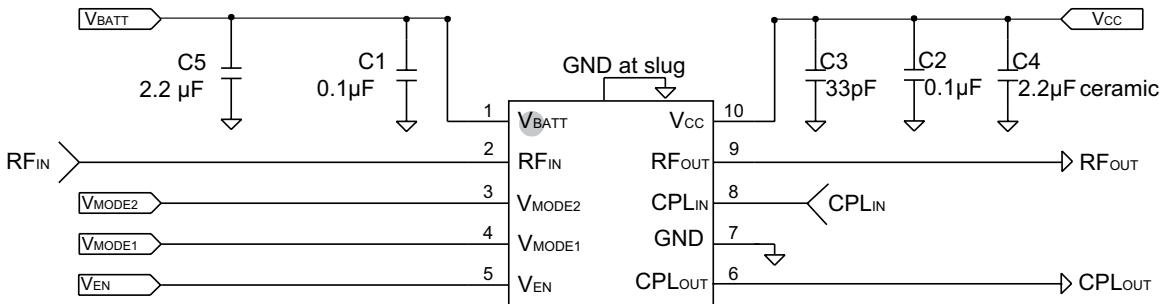
The power amplifier may be placed in either Low, Medium or High Bias modes by applying the appropriate logic level (see Operating Ranges table)

to the  $V_{MODE}$  pins. The Bias Control table below lists the recommended modes of operation for various applications.

Three operating modes are recommended to optimize current consumption. High Bias/High Power operating mode is for  $P_{OUT}$  levels  $\geq 16$  dBm. At  $\sim 17$  dBm - 8 dBm, the PA could be switched to Medium Power Mode. For  $P_{OUT}$  levels  $\leq -9$  dBm, the PA could be switched to Low Power Mode for extremely low current consumption.

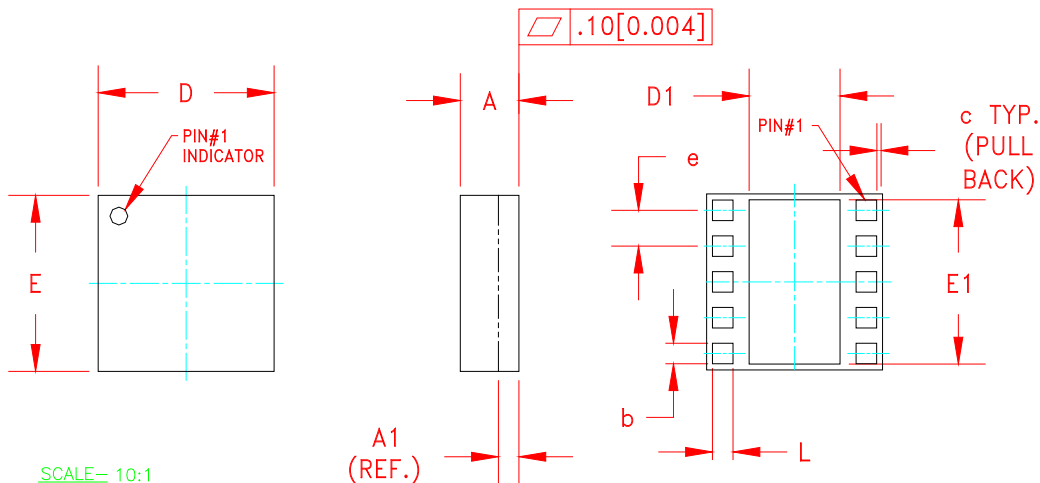
**Table 7: Bias Control**

APPLICATION	$P_{OUT}$ LEVELS	BIAS MODE	$V_{EN}$	$V_{MODE1}$	$V_{MODE2}$	$V_{CC}$	$V_{BATT}$
Low power (Low Bias Mode)	< +9 dBm	Low	+1.8 V	+1.8 V	+1.8 V	3.1 - 4.35 V	> 3.1 V
Med power (Medium Bias Mode)	> 8 dBm < +17 dBm	Low	+1.8 V	+1.8 V	0 V	3.1 - 4.35 V	> 3.1 V
High power (High Bias Mode)	> +16 dBm	High	+1.8 V	0 V	0 V	3.1 - 4.35 V	> 3.1 V
Shutdown	-	Shutdown	0 V	0 V	0 V	3.1 - 4.35 V	> 3.1 V



**Figure 9: Evaluation Board Schematic**

PACKAGE OUTLINE



SCALE= 10:1

SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.91	1.03	1.13	0.035	0.041	0.044	—
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						—
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	—	0.10	—	—	0.004	—	—
D	2.88	3.00	3.12	0.113	0.118	0.123	—
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	—
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e	0.60			0.024			3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
5. LAMINATE CONTROL DRAWING SPECIFIED BY PART NUMBER.

Figure 10: M45 Package Outline - 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module

TOP BRAND

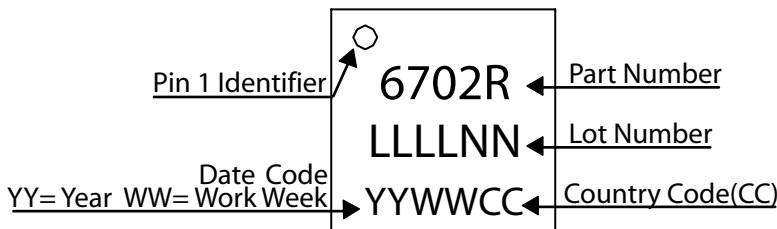
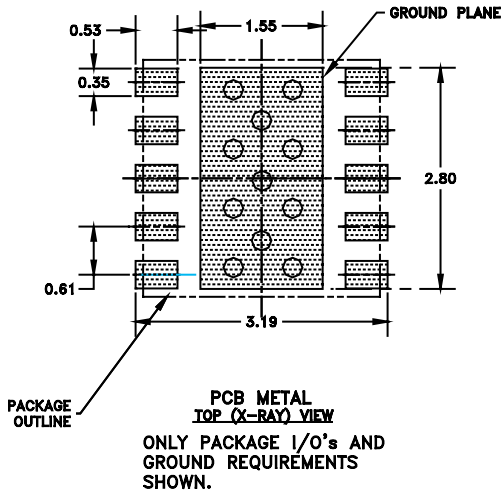


Figure 11: Branding Specification - M45 Package

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

- (1) OUTLINE DRAWING REFERENCE: P8002478\_E
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.
- (4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.
- (5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)

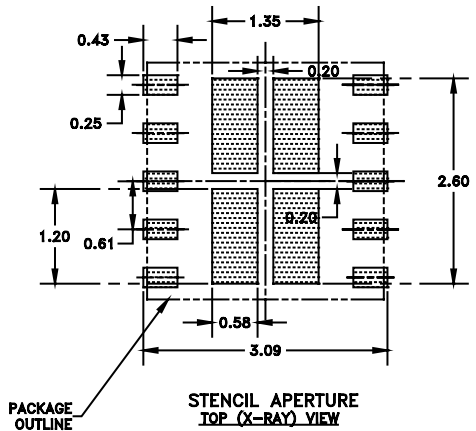
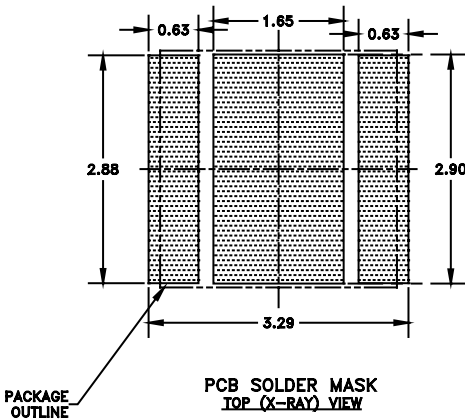


Figure 12: Recommended PCB Layout Information



**ORDERING INFORMATION**

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ALT6702RM45Q7	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
ALT6702RM45P9	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Partial Tape and Reel

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