

MB814101-80L/-10L/-12L

CMOS 4M x 1 BIT NIBBLE MODE LOW POWER DYNAMIC RAM

CMOS 4M x 1 Bit Nibble Mode Low Power Dynamic RAM

The Fujitsu MB814101 is a fully decoded CMOS dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x 1 configuration. The MB814101 features a nibble mode of operation whereby high-speed serial access of up to 4 bits of data can be selected. The MB814101 DRAM is ideally suited for mainframes, buffers, hand-held computers, and other memory applications where very low power dissipation and compact layout are basic requirements of the design. Since the standby current of the MB814101 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

The MB814101 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814101 are not critical and all inputs are TTL compatible.

Features

Parameter	MB814101-80L	MB814101-10L	MB814101-12L
RAS Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
CAS Access Time	20 ns max.	25 ns max.	30 ns max.
Nibble Mode Cycle Time	50 ns min.	55 ns min.	60 ns min.
Low Power Dissipation			
• Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/1.1 mW max. (CMOS level)		

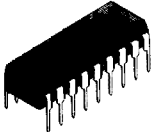
- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 128 ms
- Common I/O capability by using early write
- RAS only, CAS-before-RAS, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)


Parameter	Symbol	Value	Unit
Voltage at any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7	V
Voltage of V _{CC} supply relative to V _{SS}	V _{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T _{STG}	-55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

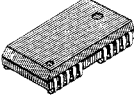
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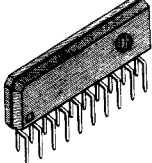
DIP-18P-M04



LCC-26P-M04



LCC-26P-M03



ZIP-20P-M02

T.B.D.

T.B.D.

FPT-26P-M01

FPT-26P-M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

