Am5380/Am53C80N*

SCSI Interface Controller

DISTINCTIVE CHARACTERISTICS

SCSI Interface

- Asynchronous interface to 1.5 megabytes per second
- Supports Initiator and Target roles
- Parity generation with optional checking
- Supports Arbitration
- Direct control of all bus signals
- High current outputs drive SCSI Bus directly

CPU Interface

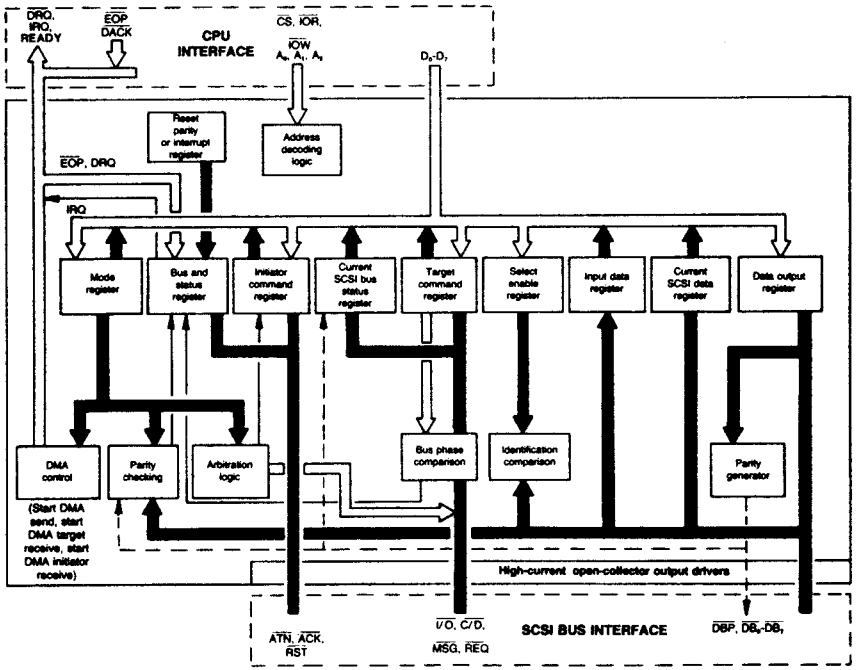
- Memory or I/O mapped interface
- DMA or programmed I/O
- Normal or Block mode DMA
- Optional CPU interrupts

GENERAL DESCRIPTION

The Am5380/Am53C80N Small Computer Systems Interface (SCSI) Interface Controller is a 40-pin NMOS/CMOS device designed to accommodate the SCSI as defined by the ANSI X3T9.2 committee. The Am5380/Am53C80N operates in both the Initiator and Target roles and can, therefore, be used in host adapter, host port and formatter designs. This device supports Arbitration, including Reselection. Special high-current open-collector output drivers, capable of sinking 48 mA at 0.5 V, allow for direct connection to the SCSI Bus.

The Am5380/Am53C80N communicates with the system microprocessor as a peripheral device. The chip is controlled by reading and writing several internal registers which may be addressed as standard or memory-mapped I/O. Minimal processor intervention is required for DMA transfers because the Am5380/Am53C80N controls the necessary handshake signals. The Am5380/Am53C80N interrupts the CPU when it detects a bus condition that requires attention. Normal and Block mode DMA is provided to match many popular DMA controllers.

BLOCK DIAGRAM

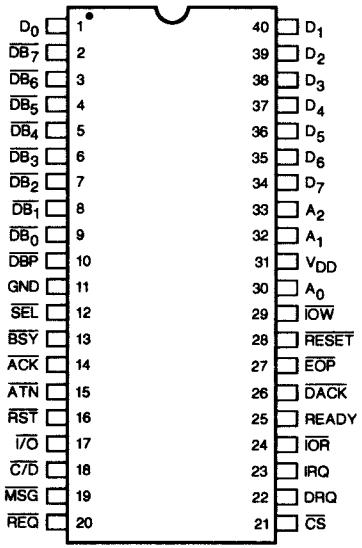


BD006561

Publication # 08289 | Rev. B | Amendment /0
Issue Date: October 1988

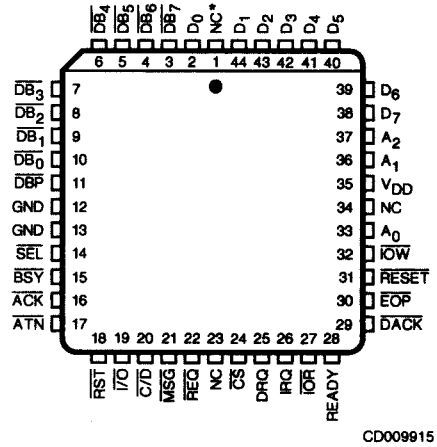
CONNECTION DIAGRAMS
Top View

DIPs



CD009900

PLCC

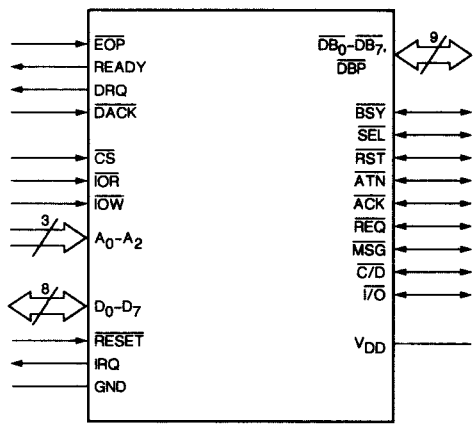


CD009915

*NC = No Connection

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



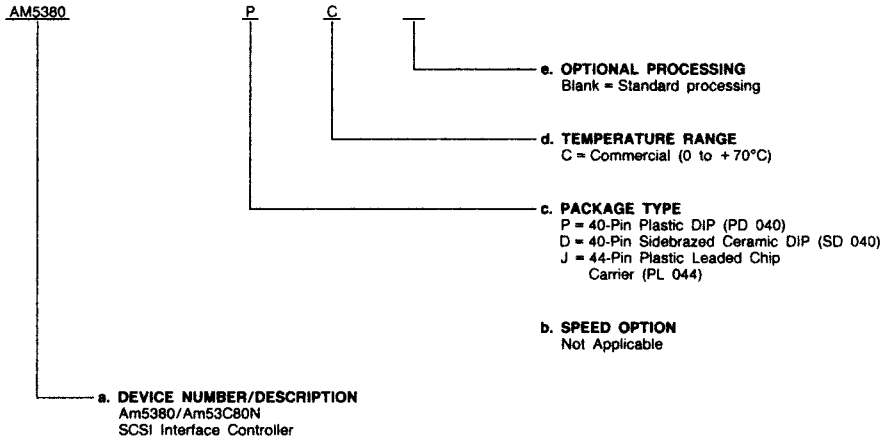
LS002643

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM5380	PC, DC, JC
AM53C80N	PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

PIN DESCRIPTION

Microprocessor Interface Signals

$A_0 - A_2$ Address Lines (Input)
These signals are used with $\overline{CS}$, $\overline{IOR}$ or $\overline{IOW}$ to address all internal registers.

$\overline{CS}$ Chip Select (Input, Active LOW)
$\overline{CS}$ enables a read or write of the internal register selected by $A_0 - A_2$.

$\overline{DACK}$ DMA Acknowledge (Input, Active LOW)
$\overline{DACK}$ resets DRQ and selects the data register for input or output data transfers.

DRQ DMA Request (Output)
DRQ indicates that the data register is ready to be read or written. DRQ occurs only if DMA mode is TRUE in the Command Register. DRQ is cleared by $\overline{DACK}$.

$D_0 - D_7$ Data Lines (Input/Output; Three-State, Active HIGH)
Bidirectional microprocessor data bus lines.

$\overline{EOP}$ End of Process (Input, Active LOW)
$\overline{EOP}$ is used to terminate a DMA transfer. If asserted during a DMA cycle, the current byte will be transferred, but no additional bytes will be requested.

$\overline{IOR}$ I/O Read (Input, Active LOW)
$\overline{IOR}$ is used to read an internal register selected by $\overline{CS}$ and $A_0 - A_2$. It also selects the Input Data Register when used with $\overline{DACK}$.

$\overline{IOW}$ I/O Write (Input, Active LOW)
$\overline{IOW}$ is used to write an internal register selected by $\overline{CS}$ and $A_0 - A_2$. It also selects the Output Data Register when used with $\overline{DACK}$.

IRQ Interrupt Request (Output)
IRQ alerts a microprocessor of an error condition or an event completion.

READY Ready (Output)
READY can be used to control the speed of Block mode DMA transfers. This signal goes active to indicate the chip is ready to send/receive data and remains FALSE after a transfer until the last byte is sent or until the DMA MODE bit is reset.

$\overline{RESET}$ Reset (Input, Active LOW)
$\overline{RESET}$ clears all registers. It does not force the SCSI $\overline{RST}$ signal to the active state.

Power Signals

V_{DD} +5-Volt Power Supply

GND Ground

SCSI Interface Signals

The following signals are all bidirectional, active-LOW, open-collector signals. With 48-mA sink capability, all pins interface directly with the SCSI Bus.

$\overline{ACK}$ Acknowledge (Input/Output; Open Collector, Active LOW)
Driven by an Initiator, $\overline{ACK}$ indicates an acknowledgment for a $\overline{REQ}/\overline{ACK}$ data-transfer handshake. In the Target role, $\overline{ACK}$ is received as a response to the $\overline{REQ}$ signal.

$\overline{ATN}$ Attention (Input/Output; Open Collector, Active LOW)
Driven by an Initiator, $\overline{ATN}$ indicates an Attention condition. This signal is received in the Target role.

$\overline{BSY}$ Busy (Input/Output; Open Collector, Active LOW)
This signal indicates that the SCSI Bus is being used and can be driven by both the Initiator and the Target device.

$\overline{C/D}$ Control/Data (Input/Output; Open Collector, Active LOW)
A signal driven by the Target, $\overline{C/D}$ indicates Control or Data information is on the Data Bus. This signal is received by the Initiator.

$\overline{I/O}$ Input/Output (Input/Output; Open Collector, Active LOW)
$\overline{I/O}$ is a signal driven by a Target which controls the direction of data movement on the SCSI Bus. TRUE indicates input to the Initiator. This signal is also used to distinguish between Selection and Reselection phases.

$\overline{MSG}$ Message (Input/Output; Open Collector, Active LOW)
$\overline{MSG}$ is a signal driven by the Target during the Message phase. This signal is received by the Initiator.

$\overline{REQ}$ Request (Input/Output; Open Collector, Active LOW)
Driven by a Target, $\overline{REQ}$ indicates a request for a $\overline{REQ}/\overline{ACK}$ data-transfer handshake. This signal is received by the Initiator.

$\overline{RST}$ SCSI Bus RESET (Input/Output; Open Collector, Active LOW)
The $\overline{RST}$ signal indicates an SCSI Bus RESET condition.

$\overline{DB_0} - \overline{DB_7}$, $\overline{DBP}$ Data Bits, Parity Bit (Input/Output; Open Collector, Active LOW)
These eight data bits ($\overline{DB_0} - \overline{DB_7}$), plus a parity bit ($\overline{DBP}$) form the Data Bus. $\overline{DB_7}$ is the most significant bit (MSB) and has the highest priority during the Arbitration phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during Arbitration.

$\overline{SEL}$ Select (Input/Output; Open Collector, Active LOW)
$\overline{SEL}$ is used by an Initiator to select a Target, or by a Target to reselect an Initiator.

FUNCTIONAL DESCRIPTION

General

The Am5380/Am53C80N Small Computer Systems Interface (SCSI) device appears as a set of eight registers to the controlling CPU. By reading and writing the appropriate registers, the CPU may initiate any SCSI Bus activity or may sample and assert any signal on the SCSI Bus. This allows the user to implement all or portions of the SCSI protocol in software. These registers are read (written) by activating $\overline{CS}$ with an address on $A_0 - A_2$ and then issuing an $\overline{IOR}$ ($\overline{IOW}$) pulse. This section describes the operation of the internal registers.

TABLE 1. REGISTER SUMMARY

Address				
A_2	A_1	A_0	R/W	Register Name
0	0	0	R	Current SCSI Data
0	0	0	W	Output Data
0	0	1	R/W	Initiator Command
0	1	0	R/W	Mode
0	1	1	R/W	Target Command
1	0	0	R	Current SCSI Bus Status
1	0	0	W	Select Enable
1	0	1	R	Bus and Status
1	0	1	W	Start DMA Send
1	1	0	R	Input Data
1	1	0	W	Start DMA Target Receive
1	1	1	R	Reset Parity/Interrupts
1	1	1	W	Start DMA Initiator Receive

Data Registers

The data registers are used to transfer SCSI commands, data, status, and message bytes between the microprocessor Data Bus and the SCSI Bus. The Am5380/Am53C80N does not interpret any information that passes through the data registers. The data registers consist of the transparent Current SCSI Data Register, the Output Data Register, and the Input Data Register.

Current SCSI Data Register — Address 0 (Read Only)

The Current SCSI Data Register is a read-only register which allows the microprocessor to read the active SCSI Data Bus. This is accomplished by activating $\overline{CS}$ with an address on $A_2 - A_0$ of 000 and issuing an $\overline{IOR}$ pulse. If parity checking is enabled, the SCSI Bus parity is checked at the beginning of the read cycle. This register is used during a programmed I/O data read or during Arbitration to check for higher priority arbitrating devices. Parity is not guaranteed valid during Arbitration.

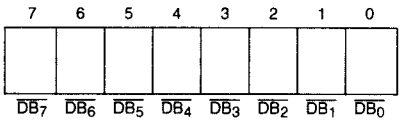


Figure 1. Current SCSI Data Register

Output Data Register — Address 0 (Write Only)

The Output Data Register is a write-only register that is used to send data to the SCSI Bus. This is accomplished by either using a normal CPU write, or under DMA control, by using $\overline{IOW}$ and $\overline{DACK}$. This register is also used to assert the proper ID bits or the SCSI Bus during the Arbitration and Selection phases.

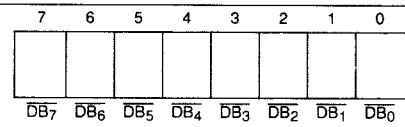


Figure 2. Output Data Register

Input Data Register — Address 6 (Read Only)

The Input Data Register is a read-only register that is used to read latched data from the SCSI Bus. Data is latched either during a DMA Target receive operation when $\overline{ACK}$ goes active or during a DMA Initiator receive when $\overline{REQ}$ goes active. The DMA MODE bit (port 2, bit 1) must be set before data can be latched in the Input Data Register. This register may be read under DMA control using $\overline{IOR}$ and $\overline{DACK}$. Parity is optionally checked when the Input Data Register is loaded.

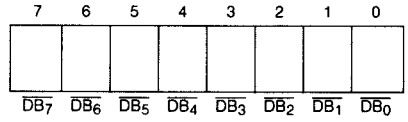


Figure 3. Input Data Register

Initiator Command Register — Address 1 (Read/Write)

The Initiator Command Register is a read/write register which is used to assert certain SCSI Bus signals, to monitor those signals, and to monitor the progress of bus arbitration. Many of these bits are significant only when being used as an Initiator; however, most can be used during Target role operation.

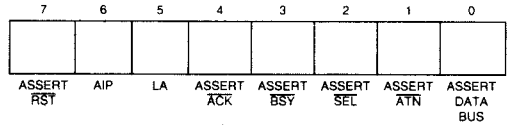


Figure 4-1. Initiator Command Register — Register Read

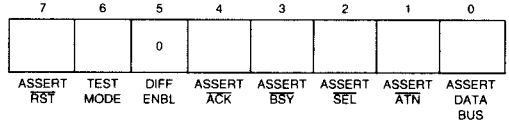


Figure 4-2. Initiator Command Register — Register Write

The following describes the operation of all bits in the Initiator Command Register.

Bit 7 — ASSERT $\overline{RST}$

Whenever a one is written to bit 7 of the Initiator Command Register, the $\overline{RST}$ signal is asserted on the SCSI Bus. The $\overline{RST}$ signal will remain asserted until this bit is reset or until an external $\overline{RESET}$ occurs. After this bit is set (1), IRQ goes active and all internal logic and control registers are reset (except for the interrupt latch and the ASSERT $\overline{RST}$ bit). Writing a zero to bit 7 of the Initiator Command Register de-asserts the $\overline{RST}$ signal. Reading this register simply reflects the status of this bit.

Bit 6 — AIP (Arbitration in Progress) (Read Bit)

This bit is used to determine if Arbitration is in progress. For this bit to be active, the ARBITRATE bit (port 2, bit 0) must

have been set previously. It indicates that a Bus-Free condition has been detected and that the chip has asserted $\overline{BSY}$ and the contents of the Output Data Register (port 0) onto the SCSI Bus. AIP will remain active until the ARBITRATE bit is reset.

Bit 6 — TEST MODE (Write Bit)

This bit may be written during a test environment to disable all output drivers, effectively removing the Am5380/Am53C80N from the circuit. Resetting this bit returns the part to normal operation.

Bit 5 — LA (Lost Arbitration) (Read Bit)

This bit, when active, indicates that the Am5380/Am53C80N detected a Bus-Free condition, arbitrated for use of the bus by asserting $\overline{BSY}$ and its ID on the Data Bus, and lost Arbitration due to $\overline{SEL}$ being asserted by another bus device. For this bit to be active, the ARBITRATE bit (port 2, bit 0) must be active.

Bit 5 — DIFF ENBL (Differential Enable) (Write Bit)

This bit should be written with a zero for proper operation.

Bit 4 — ASSERT $\overline{ACK}$

This bit is used by the bus initiator to assert $\overline{ACK}$ on the SCSI Bus. In order to assert $\overline{ACK}$, the TARGETMODE bit (port 2, bit 6) must be FALSE. Writing a zero to this bit resets $\overline{ACK}$ on the SCSI Bus. Reading this register simply reflects the status of this bit.

Bit 3 — ASSERT $\overline{BSY}$

Writing a one (1) into this bit position asserts $\overline{BSY}$ onto the SCSI Bus. Conversely, a zero resets the $\overline{BSY}$ signal. Asserting $\overline{BSY}$ indicates a successful selection or reselection and resetting this bit creates a Bus-Disconnect condition. Reading this register simply reflects the status of this bit.

Bit 2 — ASSERT $\overline{SEL}$

Writing a one (1) into this bit position asserts $\overline{SEL}$ onto the SCSI Bus. $\overline{SEL}$ is normally asserted after Arbitration has been successfully completed. $\overline{SEL}$ may be de-asserted by resetting this bit to a zero. A read of this register simply reflects the status of this bit.

Bit 1 — ASSERT $\overline{ATN}$

$\overline{ATN}$ may be asserted on the SCSI Bus by setting this bit to a one (1) if the TARGETMODE bit (port 2, bit 6) is FALSE. $\overline{ATN}$ is normally asserted by the initiator to request a Message Out bus phase. Note that since ASSERT $\overline{SEL}$ and ASSERT $\overline{ATN}$ are in the same register, a select with $\overline{ATN}$ may be implemented with one CPU write. $\overline{ATN}$ may be de-asserted by resetting this bit to zero. A read of this register simply reflects the status of this bit.

Bit 0 — ASSERT DATA BUS

The ASSERT DATA BUS bit, when set, allows the contents of the Output Data Register to be enabled as chip outputs on the signals $\overline{DB_0}$ - $\overline{DB_7}$. Parity is also generated and asserted on $\overline{DBP}$.

When connected as an Initiator, the outputs are only enabled if the TARGETMODE bit (port 2, bit 6) is FALSE, the received signal $\overline{I/O}$ is FALSE, and the phase signals ($\overline{C/D}$, $\overline{I/O}$, and $\overline{MSG}$) match the contents of the ASSERT $\overline{C/D}$, ASSERT $\overline{I/O}$, and ASSERT $\overline{MSG}$ in the Target Command Register.

This bit should also be set during DMA send operations.

Mode Register — Address 2 (Read/Write)

The Mode Register is used to control the operation of the chip. This register determines whether the Am5380/Am53C80N operates as an Initiator or a Target, whether DMA transfers are being used, whether parity is checked, and whether interrupts are generated on various external conditions. This register may be read to check the value of these internal control bits. Figure 5 describes the operation of these control bits.

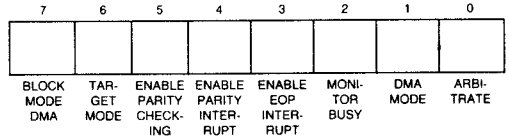


Figure 5. Mode Register

Bit 7 — BLOCK MODE DMA

The BLOCK MODE DMA bit controls the characteristics of the DMA DRQ-$\overline{DACK}$ handshake. When this bit is reset (0) and the DMA MODE bit is active (1), the DMA handshake uses the normal interlocked handshake, and the rising edge of $\overline{DACK}$ indicates the end of each byte being transferred. In block mode operations, BLOCK MODE DMA bit set (1) and DMA MODE bit set (1), the end of $\overline{IOR}$ or $\overline{IOW}$ signifies the end of each byte transferred and $\overline{DACK}$ is allowed to remain active throughout the DMA operation. READY can then be used to request the next transfer.

Bit 6 — TARGETMODE

The TARGETMODE bit allows the Am5380/Am53C80N to operate as either an SCSI Bus Initiator, bit reset (0), or as an SCSI Bus Target device, bit set (1). In order for the signals $\overline{ATN}$ and $\overline{ACK}$ to be asserted on the SCSI Bus, the TARGETMODE bit must be reset (0). In order for the signals $\overline{C/D}$, $\overline{I/O}$, $\overline{MSG}$, and $\overline{REQ}$ to be asserted on the SCSI Bus, the TARGETMODE bit must be set (1).

Bit 5 — ENABLE PARITY CHECKING

The ENABLE PARITY CHECKING bit determines whether parity errors will be ignored or saved in the parity error latch. If this bit is reset (0), parity will be ignored. Conversely, if this bit is set (1), parity errors will be saved.

Bit 4 — ENABLE PARITY INTERRUPT

The ENABLE PARITY INTERRUPT bit, when set (1), will cause an interrupt (IRQ) to occur if a parity error is detected. A parity interrupt will only be generated if the ENABLE PARITY CHECKING bit (bit 5) is also enabled (1).

Bit 3 — ENABLE EOP INTERRUPT

The ENABLE EOP INTERRUPT, when set (1), causes an interrupt to occur when the $\overline{EOP}$ (End of Process) signal is received from the DMA controller logic.

Bit 2 — MONITOR BUSY

The MONITOR BUSY bit, when TRUE (1), causes an interrupt to be generated for an unexpected loss of $\overline{BSY}$. When the interrupt is generated due to loss of $\overline{BSY}$, the lower six bits of the Initiator Command Register are reset (0) and all signals are removed from the SCSI Bus.

Bit 1 — DMA MODE

The DMA MODE bit is normally used to enable a DMA transfer and must be set (1) prior to writing ports 5 through 7. Ports 5 through 7 are used to start DMA transfers. The TARGETMODE bit (port 2, bit 6) must be consistent with writes to port 6 and 7 [i.e., set (1) for a write to port 6 and reset (0) for a write to port 7]. The control bit ASSERT DATA BUS (port 1, bit 0) must be TRUE (1) for all DMA send operations. In the DMA mode, $\overline{REQ}$ and $\overline{ACK}$ are automatically controlled.

The DMA MODE bit is not reset upon the receipt of an $\overline{EOP}$ signal. Any DMA transfer may be stopped by writing a zero into this bit location; however, care must be taken not to cause $\overline{CS}$ and $\overline{DACK}$ to be active simultaneously.

Bit 0 — ARBITRATE

The ARBITRATE bit is set (1) to start the Arbitration process. Prior to setting this bit, the Output Data Register should contain the proper SCSI device ID value. Only one data bit should be active for SCSI Bus Arbitration. The Am5380/Am53C80N will wait for a Bus-Free condition before entering the Arbitration phase. The results of the Arbitration phase may be determined by reading the status bits LA and AIP (port 1, bits 5 and 6, respectively).

Target Command Register — Address 3 (Read/Write)

When connected as a target device, the Target Command Register allows the CPU to control the SCSI Bus Information Transfer phase and/or to assert $\overline{REQ}$ simply by writing this register. The TARGETMODE bit (port 2, bit 6) must be TRUE (1) for bus assertion to occur. The SCSI Bus phases are described in Table 2.

TABLE 2. SCSI INFORMATION TRANSFER PHASES

Bus Phase	ASSERT $\overline{I/O}$	ASSERT $\overline{C/D}$	ASSERT $\overline{MSG}$
Data Out	0	0	0
Unspecified	0	0	1
Command	0	1	0
Message Out	0	1	1
Data In	1	0	0
Unspecified	1	0	1
Status	1	1	0
Message In	1	1	1

When connected as an Initiator with DMA Mode TRUE, if the phase lines ($\overline{I/O}$, $\overline{C/D}$, and $\overline{MSG}$) do not match the phase bits in the Target Command Register, a phase-mismatch interrupt is generated when $\overline{REQ}$ goes active. In order to send data as an Initiator, the ASSERT $\overline{I/O}$, ASSERT $\overline{C/D}$, and ASSERT $\overline{MSG}$ bits must match the corresponding bits in the Current SCSI Bus Status Register (port 4). The ASSERT $\overline{REQ}$ bit (bit 3) has no meaning when operating as an Initiator.

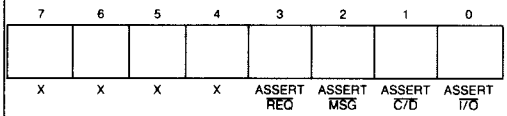


Figure 6. Target Command Register

Current SCSI Bus Status Register — Address 4 (Read Only)

The Current SCSI Bus Status Register is a read-only register which is used to monitor seven SCSI Bus control signals plus the Data Bus parity bit. For example, an Initiator device can use this register to determine the current bus phase and to poll $\overline{REQ}$ for pending data transfers. This register may also be used to determine why a particular interrupt occurred. Figure 7 describes the Current SCSI Bus Status Register.

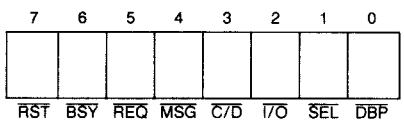


Figure 7. Current SCSI Bus Status Register

Select Enable Register — Address 4 (Write Only)

The Select Enable Register is a write-only register which is used as a mask to monitor a signal ID during a selection attempt. The simultaneous occurrence of the correct ID bit, $\overline{BSY}$ FALSE, and $\overline{SEL}$ TRUE will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the ENABLE PARITY CHECKING bit (port 2, bit 5) is active (1), parity will be checked during selection.

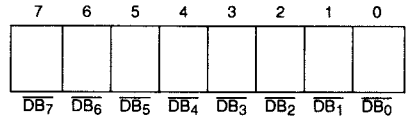


Figure 8. Select Enable Register

Bus and Status Register — Address 5 (Read Only)

The Bus and Status Register is a read-only register which can be used to monitor the remaining SCSI control signals not found in the Current SCSI Bus Status Register ($\overline{ATN}$ and $\overline{ACK}$), as well as six other status bits. The following describes each bit of the Bus and Status Register individually.

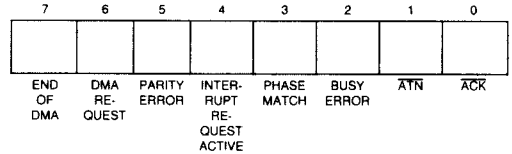


Figure 9. Bus and Status Register

Bit 7 — END OF DMA TRANSFER

The END OF DMA TRANSFER bit is set if $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active for at least 100 ns. Since the $\overline{EOP}$ signal can occur during the last byte sent to the Output Data Register (port 0), the $\overline{REQ}$ and $\overline{ACK}$ signals should be monitored to ensure that the last byte has been transferred. This bit is reset when the DMA MODE bit is reset (0) in the Mode Register (port 2).

Bit 6 — DMA REQUEST

The DMA REQUEST bit allows the CPU to sample the output pin DRQ. DRQ can be cleared by asserting $\overline{DACK}$ or by resetting the DMA MODE bit (bit 1) in the Mode Register (port 2). The DRQ signal does not reset when a phase-mismatch interrupt occurs.

Bit 5 — PARITY ERROR

This bit is set if a parity error occurs during a data receive or a device selection. The PARITY ERROR bit can only be set (1) if the ENABLE PARITY CHECK bit (port 2, bit 5) is active (1). This bit may be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 4 — INTERRUPT REQUEST ACTIVE

This bit is set if an enabled interrupt condition occurs. It reflects the current state of the IRQ output and can be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 3 — PHASE MATCH

The SCSI signals, $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$, represent the current Information Transfer phase. The PHASE MATCH bit indicates whether the current SCSI Bus phase matches the lower 3 bits of the Target Command Register. PHASE MATCH is continu-

ously updated and is only significant when operating as a Bus Initiator. A phase match is required for data transfers to occur on the SCSI Bus.

Bit 2 — BUSY ERROR

The BUSY ERROR bit is active if an unexpected loss of the $\overline{BSY}$ signal has occurred. This latch is set whenever the MONITOR BUSY bit (port 2, bit 2) is TRUE and $\overline{BSY}$ is FALSE. An unexpected loss of $\overline{BSY}$ will disable any SCSI outputs and will reset the DMA MODE bit (port 2, bit 1).

Bit 1 — ATN

This bit reflects the condition of the SCSI Bus control signal $\overline{ATN}$. This signal is normally monitored by the Target device.

Bit 0 — ACK

This bit reflects the condition of the SCSI Bus control signal $\overline{ACK}$. This signal is normally monitored by the Target device.

DMA Registers

Three write-only registers are used to initiate all DMA activity. They are Start DMA Send (port 5), Start DMA Target Receive (port 6), and Start DMA Initiator Receive (port 7). Simply writing these registers starts the DMA transfers. Data presented to the Am5380/Am53C80N on signals $D_0 - D_7$ during the register write is meaningless and has no effect on the operation. Prior to writing these registers, the BLOCK MODE DMA bit (bit 7). The DMA MODE bit (bit 1) and the TARGET-MODE bit (bit 6) in the Mode Register (port 2) must be appropriately set. The individual registers are briefly described as follows:

Start DMA Send — Address 5 (Write Only)

This register is written to initiate a DMA send, from the DMA to the SCSI Bus, for either Initiator or Target role operations. The DMA MODE bit (port 2, bit 1) must be set prior to writing this register.

Start DMA Target Receive — Address 6 (Write Only)

This register is written to initiate a DMA receive — from the SCSI Bus to the DMA, for Target operation only. The DMA MODE bit (bit 1) and the TARGETMODE bit (bit 6) in the Mode Register (port 2) must both be set (1) prior to writing this register.

Start DMA Initiator Receive — Address 7 (Write Only)

This register is written to initiate a DMA receive — from the SCSI Bus to the DMA, for Initiator operation only. The DMA MODE bit (bit 6) must be FALSE (0) in the Mode Register (port 2) prior to writing this register.

Reset Parity/Interrupt — Address 7 (Read Only)

Reading this register resets the PARITY ERROR bit (bit 5), the INTERRUPT REQUEST bit (bit 4), and the BUSY ERROR bit (bit 2) in the Bus and Status Register (port 5).

On-Chip SCSI Hardware Support

The Am5380/Am53C80N is easy to use because of its simple architecture. The chip allows direct control and monitoring of the SCSI Bus by providing a latch for each signal. However, portions of the protocol define timings which are much too quick for traditional microprocessors to control. Therefore, hardware support has been provided for DMA transfers, bus arbitration, phase-change monitoring, bus disconnection, bus reset, parity generation, parity checking, and device selection/reselection.

Arbitration is accomplished using a Bus-Free filter to continuously monitor $\overline{BSY}$. If $\overline{BSY}$ remains inactive for at least 400 ns then the SCSI Bus is considered free and Arbitration may begin. Arbitration will begin if the bus is free, $\overline{SEL}$ is inactive, and the ARBITRATION bit (port 2, bit 0) is active. Once arbitration has begun ($\overline{BSY}$ asserted), an arbitration delay of 2.2 μs must elapse before the Data Bus can be examined to determine if Arbitration has been won. This delay must be implemented in the controlling software driver.

The Am5380/Am53C80N is a clockwise device. Delays such as bus-free delay, bus-set delay, and bus-settle delay are implemented using gate delays. These delays may differ between devices because of inherent process variations, but are well within the proposed ANSI X3T9.2 specification.

Interrupts

The Am5380/Am53C80N provides an interrupt output (IRQ) to indicate a task completion or an abnormal bus occurrence. The use of interrupts is optional and may be disabled by resetting the appropriate bits in the Mode Register (port 2) or the Select Enable Register (port 4).

When an interrupt occurs, the Bus and Status Register and the Current SCSI Bus Status Register must be read to determine which condition created the interrupt. IRQ can be reset simply by reading the Reset Parity/Interrupt Register (port 7) or by an external chip reset ($\overline{RESET}$ active for 200 ns).

Assuming the Am5380/Am53C80N has been properly initialized, an interrupt will be generated if the chip is selected or reselected, if an $\overline{EOP}$ signal occurs during a DMA transfer, if an SCSI Bus reset occurs, if a parity error occurs during a data transfer, if a bus phase mismatch occurs, or if an SCSI Bus disconnection occurs.

Selection/Reselection

The Am5380/Am53C80N can generate a select interrupt if $\overline{SEL}$ is TRUE (1), its device ID is TRUE (1), and $\overline{BSY}$ is FALSE for at least a bus-settle delay (400 ns). If $\overline{I/O}$ is active, this should be considered a reselect interrupt. The correct ID bit is determined by a match in the Select Enable Register (port 4). Only a single bit match is required to generate an interrupt. This interrupt may be disabled by writing zeros into all bits of the Select Enable Register.

If parity is supported, parity should also be good during the selection phase. Therefore, if the ENABLE PARITY bit (port 2, bit 5) is active, then the PARITY ERROR bit should be checked to ensure that a proper selection has occurred. The ENABLE PARITY INTERRUPT bit need not be set for this interrupt to be generated.

The proposed SCSI specification also requires that no more that two device IDs be active during the selection process. To ensure this, the Current SCSI Data Register (port 0) should be read.

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 10 and 11, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	X	0	X	0
END OF DMA	DMA REQUEST	PARITY ERROR	INTERRUPT REQUEST ACTIVE	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Figure 10. Bus and Status Register

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 11. Current SCSI Bus Status Register

End of Process (EOP) Interrupt

An End of Process signal ($\overline{EOP}$) which occurs during a DMA transfer (DMAMODE TRUE) will set the END OF DMA Status bit (port 5, bit 7) and will optionally generate an interrupt if ENABLE EOP INTERRUPT bit (port 2, bit 3) is TRUE. The $\overline{EOP}$ pulse will not be recognized (END OF DMA bit set) unless $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are concurrently active for at least 100 ns. DMA transfers can still occur if $\overline{EOP}$ was not asserted at the correct time. This interrupt can be disabled by resetting the ENABLE EOP INTERRUPT bit.

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for this interrupt are shown in Figures 12 and 13, respectively.

7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	X
END OF DMA	DMA REQUEST	PARITY ERROR	INTERRUPT REQUEST ACTIVE	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Figure 12. Bus and Status Register

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 13. Current SCSI Bus Status Register

The END OF DMA bit is used to determine when a block transfer is complete. Receive operations are complete when there is no data left in the chip and no additional handshakes occurring. The only exception to this is receiving data as an Initiator and the Target opts to send additional data for the same phase. In this case, $\overline{REQ}$ goes active and the new data is present in the Input Data Register. Since a phase-mismatch interrupt will not occur, $\overline{REQ}$ and $\overline{ACK}$ need to be sampled to determine that the Target is attempting to send more data.

For send operations, the END OF DMA bit is set when the DMA finishes its transfer, but the SCSI transfer may still be in progress. If connected as a Target, $\overline{REQ}$ and $\overline{ACK}$ should be sampled until both are FALSE. If connected as an Initiator, a phase change interrupt can be used to signal the completion of the previous phase. It is possible for the Target to request additional data for the same phase. In this case, a phase change will not occur and both $\overline{REQ}$ and $\overline{ACK}$ must be sampled to determine when the last byte was transferred.

SCSI Bus Reset

The Am5380/Am53C80N generates an interrupt when the $\overline{RST}$ signal transitions to TRUE. The device releases all bus signals within a bus-clear delay (800 ns) of this transition. This interrupt also occurs after setting the ASSERT $\overline{RST}$ bit (port 1, bit 7). This interrupt cannot be disabled. (Note: $\overline{RST}$ is not latched in bit 7 of the Current SCSI Bus Status Register and may not be active when this port is read. For this case, the Bus Reset interrupt may be determined by default).

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 14 and 15, respectively.

7	6	5	4	3	2	1	0
0	X	0	1	X	0	X	X
END OF DMA	DMA REQUEST	PARITY ERROR	INTERRUPT REQUEST ACTIVE	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Figure 14. Bus and Status Register

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 15. Current SCSI Bus Status Register

Parity Error

An interrupt is generated for a received parity error if the ENABLE PARITY CHECK (bit 5) and the ENABLE PARITY INTERRUPT (bit 4) bits are set (1) in the Mode Register (port 2). Parity is checked during a read of the Current SCSI Data Register (port 0) and during a DMA receive operation. A parity error can be detected without generating an interrupt by disabling the ENABLE PARITY INTERRUPT bit and checking the PARITY ERROR flag (port 5, bit 5).

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 16 and 17, respectively.

7	6	5	4	3	2	1	0
0	X	1	1	1	0	X	X
END OF DMA	DMA REQUEST	PARITY ERROR	INTERRUPT REQUEST ACTIVE	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Figure 16. Bus and Status Register

7	6	5	4	3	2	1	0
0	1	1	X	X	X	0	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 17. Current SCSI Bus Status Register

Bus Phase Mismatch

The SCSI phase lines are comprised of the signals $\overline{I/O}$, $\overline{C/D}$, and $\overline{MSG}$. These signals are compared with the corresponding bits in the Target Command Register: ASSERT $\overline{I/O}$ (bit 0), ASSERT $\overline{C/D}$ (bit 1), and ASSERT $\overline{MSG}$ (bit 2). The comparison occurs continually and is reflected in the PHASE MATCH bit (bit 3) of the Bus and Status Register (port 5). If the DMA MODE bit (port 2, bit 1) is active and a phase mismatch occurs when $\overline{REQ}$ transitions from FALSE to TRUE, an interrupt (IRQ) is generated.

A phase mismatch prevents the recognition of $\overline{REQ}$ and removes the chip from the bus during an Initiator send operation ($\overline{DB_0}$ – $\overline{DB_7}$ and $\overline{DBP}$ will not be driven even though the ASSERT DATA BUS bit (port 1, bit 0) is active). This interrupt is only significant when connected as an Initiator and may be disabled by resetting the DMA MODE bit (Note: it is possible for this interrupt to occur when connected as a Target if another device is driving the phase lines to a different state).

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 18 and 19, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	0	0	X	0
END OF DMA	DMA REQUEST	PARITY ERROR	INTERRUPT REQUEST ACTIVE	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Figure 18. Bus and Status Register

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	C/$\overline{D}$	I/$\overline{O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 19. Current SCSI Bus Status Register

Loss of $\overline{BSY}$

If the MONITOR BUSY bit (bit 2) in the Mode Register (port 2) is active, an interrupt will be generated if the $\overline{BSY}$ signal goes FALSE for at least a bus-settle delay (400 ns). This interrupt may be disabled by resetting the MONITOR BUSY bit. Register values are displayed in Figures 20 and 21.

7	6	5	4	3	2	1	0
0	0	0	1	X	1	0	0
END OF DMA	DMA REQUEST	PARITY ERROR	INTERRUPT REQUEST ACTIVE	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Figure 20. Bus and Status Register

7	6	5	4	3	2	1	0
0	0	0	X	X	X	0	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	C/$\overline{D}$	I/$\overline{O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 21. Current SCSI Bus Status Register

Reset Conditions

Three possible reset situations exist with the Am5380/Am53C80N, as follows:

Hardware Chip Reset

When the signal $\overline{RST}$ is active for at least 200 ns, the Am5380/Am53C80N device is re-initialized and all internal logic and control registers are cleared. This is a chip reset only and does not create an SCSI Bus-Reset condition.

SCSI Bus Reset ($\overline{RST}$) Received

When an SCSI $\overline{RST}$ signal is received, an IRQ interrupt is generated and a chip reset is performed. All internal logic and registers are cleared, except for the IRQ interrupt latch and the ASSERT $\overline{RST}$ bit (bit 7) in the Initiator Command Register (port 1). (Note: The $\overline{RST}$ signal may be sampled by reading the Current SCSI Bus Status Register (port 4); however, this signal is not latched and may not be present when this port is read.)

SCSI Bus Reset ($\overline{RST}$) Issued

If the CPU sets the ASSERT $\overline{RST}$ bit (bit 7) in the Initiator Command Register (port 1), the $\overline{RST}$ signal goes active on the SCSI Bus and an internal reset is performed. Again, all internal logic and registers are cleared except for the IRQ interrupt latch and the ASSERT $\overline{RST}$ bit (bit 7) in the Initiator Command Register (port 1). The $\overline{RST}$ signal will continue to be active until the ASSERT $\overline{RST}$ bit is reset or until a hardware reset occurs.

Data Transfers

Data may be transferred between SCSI Bus devices in one of four modes: 1) Programmed I/O, 2) Normal DMA, 3) Block Mode DMA, or 4) Pseudo DMA. The following sections describe these modes in detail (Note: for all data transfer operations $\overline{DACK}$ and $\overline{CS}$ should never be active simultaneously).

Programmed I/O Transfers

Programmed I/O is the most primitive form of data transfer. The $\overline{REQ}$ and $\overline{ACK}$ handshake signals are individually monitored and asserted by readinig and writing the appropriate register bits. This type of transfer is normally used when transferring small blocks of data such as command blocks or message and status bytes.

An Initiator send operation would begin by setting the C/$\overline{D}$, I/$\overline{O}$, and $\overline{MSG}$ bits in the Target Command Register to the correct state so that a phase match exists. In addition to the phase match condition, it is necessary for the ASSERT DATA BUS bit (port 1, bit 0) to be TRUE and the received I/O signal to be FALSE for the Am5380/Am53C80N to send data.

For each transfer, the data is loaded into the Output Data Register (port 0). The CPU then waits for the $\overline{REQ}$ bit (port 4, bit 5) to become active. Once $\overline{REQ}$ goes active, the PHASE MATCH bit (port 5, bit 3) is checked and the ASSERT $\overline{ACK}$ bit (port 1, bit 4) is set. The $\overline{REQ}$ bit is sampled until it becomes FALSE and the CPU resets the ASSERT $\overline{ACK}$ bit to complete the transfer.

Normal DMA Mode

DMA transfers are normally used for large block transfers. The SCSI chip outputs a DMA request (DRQ) whenever it is ready for a byte transfer. External DMA logic uses this DRQ signal to generate $\overline{DACK}$ and an $\overline{IOR}$ or an $\overline{IOW}$ pulse to the Am5380/Am53C80N. DRQ goes inactive when $\overline{DACK}$ is asserted and $\overline{DACK}$ goes inactive some time after the minimum read or write pulse width. This process is repeated for every byte. For this mode, $\overline{DACK}$ should not be allowed to cycle unless a transfer is taking place.

Block Mode DMA

Some popular DMA controllers such as the Am9517A provide a Block mode DMA transfer. This type of transfer allows the DMA controller to transfer blocks of data without relinquishing the use of the Data Bus to the CPU after each byte is transferred; thus, faster transfer rates are achieved by eliminating the repetitive access and release of the CPU Bus.

If the BLOCK MODE DMA bit (port 2, bit 7) is active, the Am5380/Am53C80N will begin the transfer by asserting DRQ. The DMA controller then asserts $\overline{DACK}$ for the remainder of the block transfer. DRQ goes inactive for the duration of the transfer. The READY output is used to control the transfer rate.

Non-Block mode DMA transfers end when $\overline{DACK}$ goes FALSE, whereas Block mode transfers end when $\overline{IOR}$ or $\overline{IOW}$ becomes inactive. Since this is the case, DMA transfers may be started sooner in a Block mode transfer.

To obtain optimum performance in Block mode operation, the DMA logic may optionally use the normal DMA mode interlocking handshake. READY is still available to throttle the DMA transfer, but DRQ is 30 to 40 ns faster than READY and may be used to start the cycle sooner.

The methods described under 'Halting a DMA Operation' apply for all DMA operations.

Pseudo DMA Mode

To avoid the tedium of monitoring and asserting the request/acknowledge handshake signals for programmed I/O transfers, the system may be designed to implement a pseudo DMA mode. This mode is implemented by programming the Am5380/Am53C80N to operate in the DMA mode, but using the CPU to emulate the DMA handshake. DRQ may be detected by polling the DMA REQUEST bit (bit 6) in the Bus and Status Register (port 5), by sampling the signal through an external port or by using it to generate a CPU interrupt. Once DRQ is detected, the CPU can perform a read or write data transfer. This CPU read/write is externally decoded to generate the appropriate $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ signals.

Often, external decoding logic is necessary to generate the Am5380/Am53C80N $\overline{CS}$ signal. This same logic may be used to generate $\overline{DACK}$ at no extra system cost and provide an increased performance in programmed I/O transfers.

Halting a DMA Operation

The $\overline{EOP}$ signal is not the only way to halt a DMA transfer. A bus phase mismatch or a reset of the DMA MODE bit (port 2, bit 1) can also terminate a DMA cycle for the current bus phase.

Using the $\overline{EOP}$ Signal

If $\overline{EOP}$ is used, it should be asserted for at least 100 ns while $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active. Note, however, that if $\overline{IOR}$ or $\overline{IOW}$ is not active an interrupt will be generated, but the DMA activity will continue. The $\overline{EOP}$ signal does not reset the DMA MODE bit. Since the $\overline{EOP}$ signal can occur during the last byte sent to the Output Data Register (port 0), the $\overline{REQ}$ and $\overline{ACK}$ signals should be monitored to ensure that the last byte has transferred.

Bus Phase Mismatch Interrupt

A bus phase mismatch interrupt may be used to halt the transfer if operating as an Initiator. Using this method frees the host from maintaining a data length counter and frees the DMA logic from providing the $\overline{EOP}$ signal. If performing an Initiator send operation, the Am5380/Am53C80N requires $\overline{DACK}$ to cycle before $\overline{ACK}$ goes inactive. Since phase changes cannot occur if $\overline{ACK}$ is active, either $\overline{DACK}$ must be cycled after the last byte is sent or the DMA MODE bit must be reset in order to receive the phase mismatch interrupt.

Resetting the DMA MODE Bit

A DMA operation may be halted at any time simply by resetting the DMA MODE bit. It is recommended that the DMA MODE bit be reset after receiving an $\overline{EOP}$ or bus phase-mismatch interrupt. The DMA MODE bit must then be set before writing any of the start DMA registers for subsequent bus phases.

If resetting the DMA MODE bit is used instead of $\overline{EOP}$ for Target role operation, then care must be taken to reset this bit at the proper time. If receiving data as a Target device, the DMA MODE bit must be reset once the last DRQ is received and before $\overline{DACK}$ is asserted to prevent an additional $\overline{REQ}$ from occurring. Resetting this bit causes DRQ to go inactive. However, the last byte received remains in the Input Data Register and may be obtained either by performing a normal CPU read or by cycling $\overline{DACK}$ and $\overline{IOR}$. In most cases $\overline{EOP}$ is easier to use when operating as a Target device.

Flowcharts

Flowcharts are provided (see Figures 22 through 25) as a guideline to facilitate your firmware development. Firmware will vary depending on the application and the level of the SCSI protocol being supported.

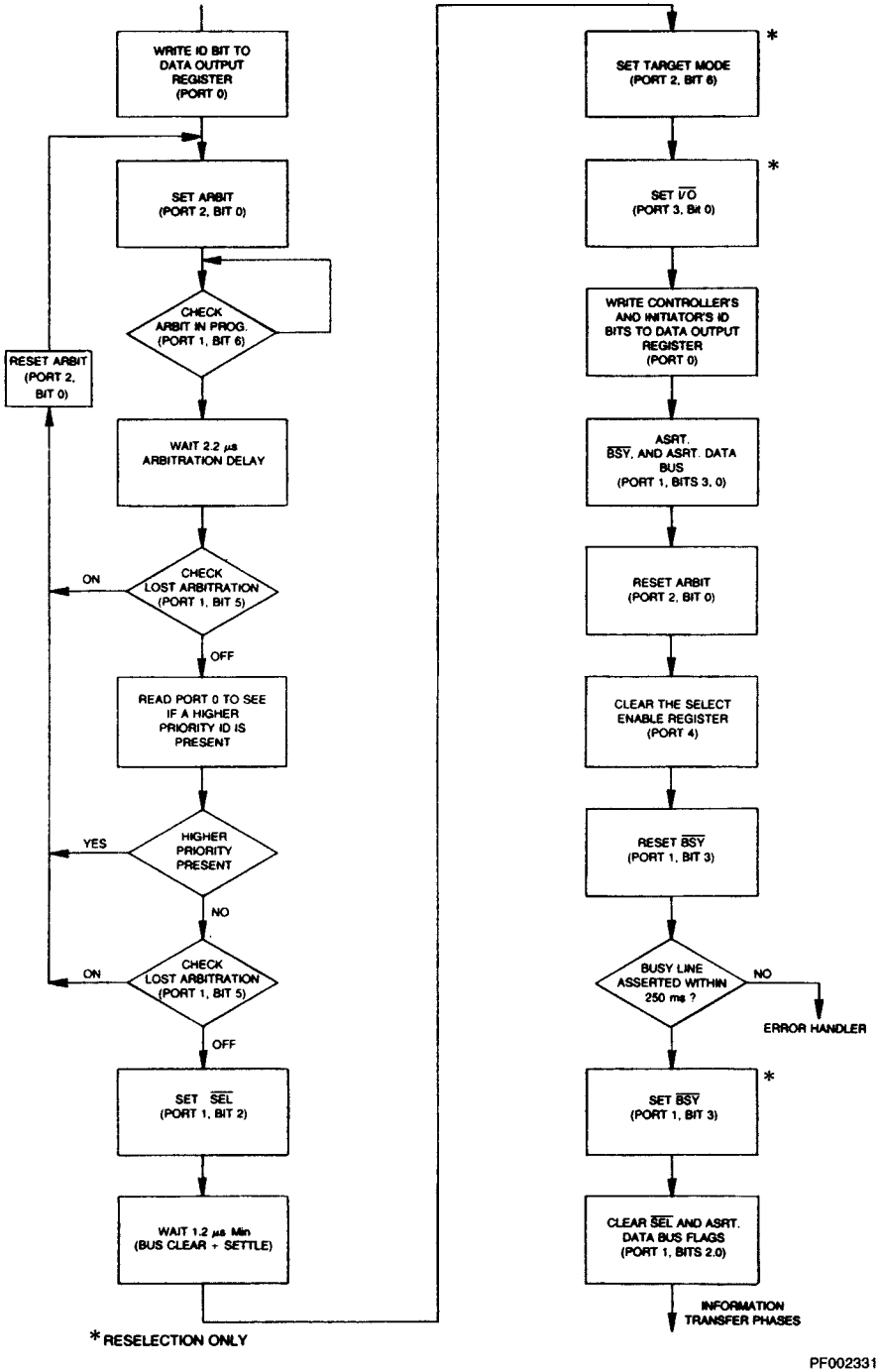


Figure 22. Arbitration and (Re) Selection

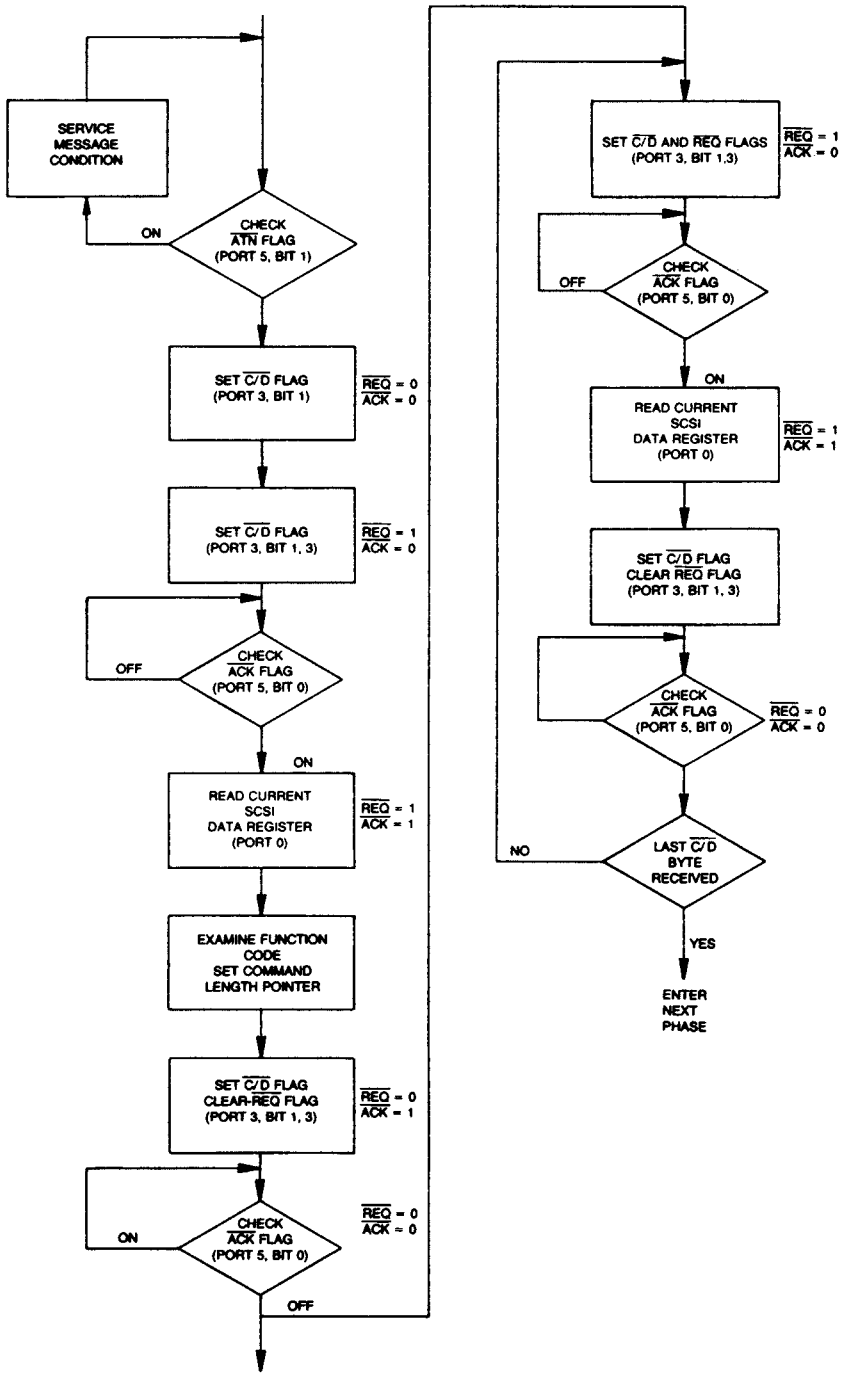
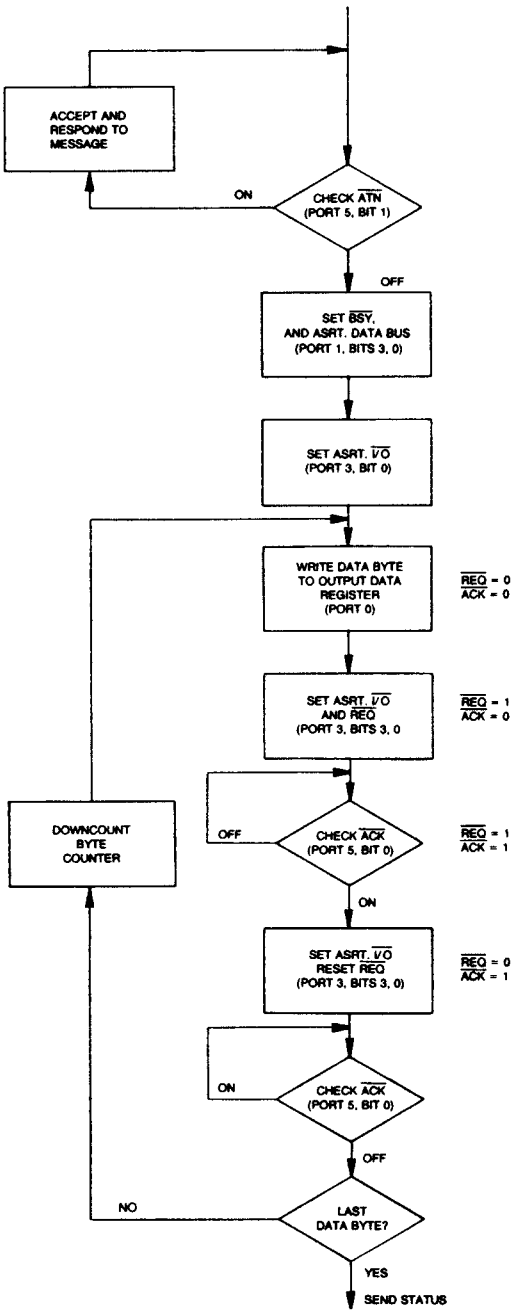


Figure 23. Command Transfer Phase (Target)



PF002351

Figure 24. Data Transfer to Host via Programmed I/O

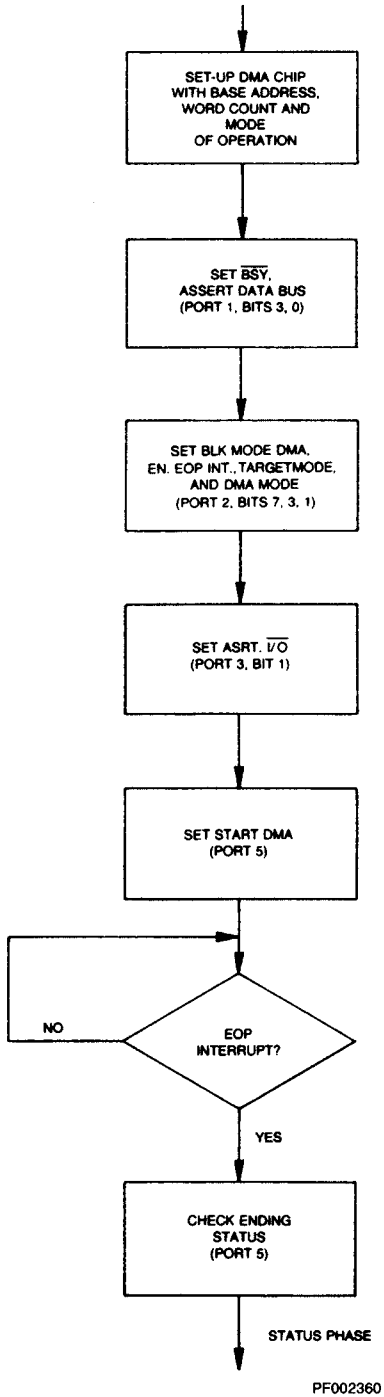


Figure 25. Data Transfer via DMA

READ **WRITE**

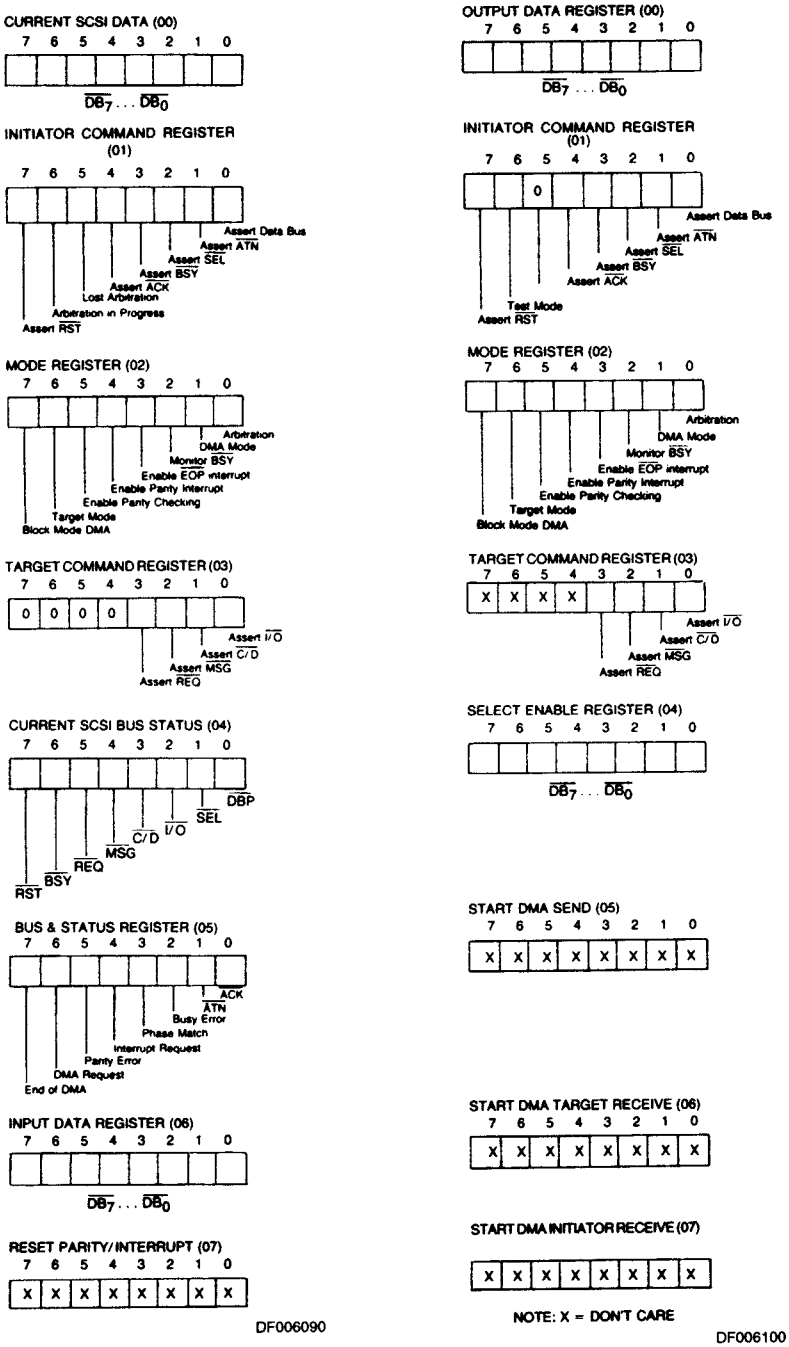


Figure 26. Register Reference Chart

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage on Any Pin
with Respect to Ground ..... −0.5 to +7.0 V
Power Dissipation:
Am5380 ..... 0.8 W
Am53C80N ..... 0.2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

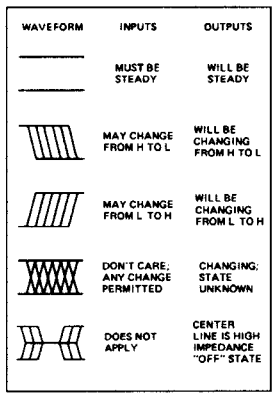
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (Note 1)

Parameter Description	Test Conditions		Min.	Max.	Unit
INPUT SIGNAL REQUIREMENTS					
HIGH-Level Input (V_{IH})			2.0	5.25	V
LOW-Level Input (V_{IL})			−0.3	0.8	V
HIGH-Level Input Current (I_{IH}):					
Am5380 = SCSI Bus Pins	V_{IH} = 5.25 V, V_{IL} = 0				μA
Am53C80N = SCSI Bus Pins except $\overline{RST}$				50	
All Other Pins				10	
LOW-Level Input Current (I_{IL}):					
Am5380 = SCSI Bus Pins	V_{IH} = 5.25 V, V_{IL} = 0				μA
Am53C80N = SCSI Bus Pins except $\overline{RST}$				−50	
All Other Pins				−10	
OUTPUT SIGNAL REQUIREMENTS					
HIGH-Level Output Voltage (V_{OH}):					
Am5380 = All Pins	V_{DD} = 4.75 V, I_{OH} = −3.0 mA		2.4		V
Am53C80N = All Pins except SCSI Bus					
LOW-Level Output Voltage (V_{OL}):					
SCSI Bus Pins	V_{DD} = 4.75 V, I_{OL} = 48.0 mA				
All Other Pins	V_{DD} = 4.75 V, I_{OL} = 7.0 mA			0.5	V
Power Supply Current (I_{DD})	V_{CC} = Max.	Am5380		145	mA
		Am53C80N		−35	

Notes: 1. Information for the Am53C80N is Preliminary and Subject to Change.

KEY TO SWITCHING WAVEFORMS



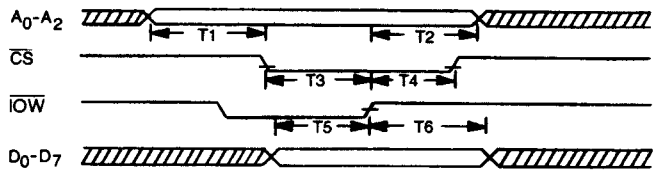
KS000010

SWITCHING CHARACTERISTICS/WAVEFORMS (Cont'd.)

CPU Write Cycle

Name	Description	Min.	Max.	Unit
T1	Address Setup to Write Enable*	10		ns
T2	Address Hold from End Write Enable*	0		ns
T3	Write Enable Width*	40		ns
T4	Chip Select Hold from End of $\overline{IOW}$	0		ns
T5	Data Setup to End of Write Enable*	20		ns
T6	Data Hold Time from End of $\overline{IOW}$	30		ns

*Write Enable is the occurrence of $\overline{IOW}$ and $\overline{CS}$

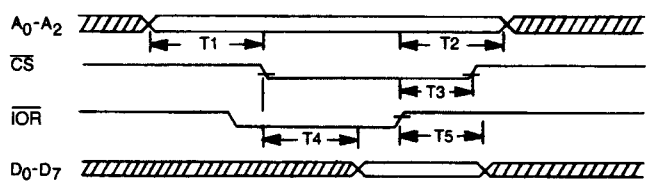


WF022360

CPU Read Cycle

Name	Description	Min.	Max.	Unit
T1	Address Setup to Read Enable*	10		ns
T2	Address Hold from End Read Enable*	0		ns
T3	Chip Select Hold from End of $\overline{IOR}$	0		ns
T4	Data Access Time from Read Enable*		100	ns
T5	Data Hold Time from End of $\overline{IOR}$	0		ns

*Read Enable is the occurrence of $\overline{IOR}$ and $\overline{CS}$



WF022370

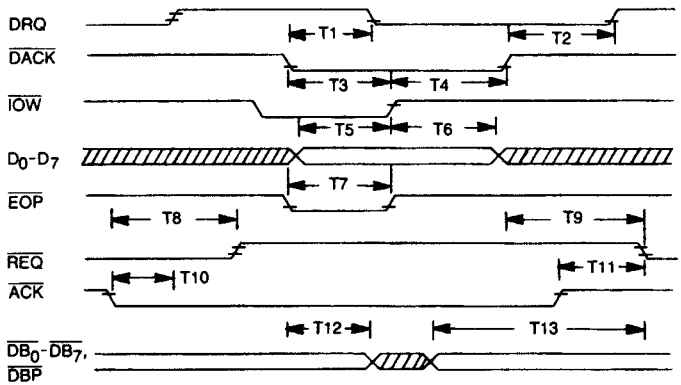
SWITCHING CHARACTERISTICS/WAVEFORMS (Cont'd.)

DMA Write (Non-Block Mode) Target Send Cycle

Name	Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		100	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	Write Enable Width*	70		ns
T4	DACK Hold from End of $\overline{IOW}$	0		ns
T5	Data Setup to End of Write Enable*	30		ns
T6	Data Hold Time from End of $\overline{IOW}$	40		ns
T7	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T8	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		125	ns
T9	$\overline{REQ}$ from End of $\overline{DACK}$ ($\overline{ACK}$ FALSE)		120	ns
T10	$\overline{ACK}$ TRUE to DRQ TRUE (Target)		110	ns
T11	$\overline{REQ}$ from End of $\overline{ACK}$ ($\overline{DACK}$ FALSE)		120	ns
T12	Data Hold from Write Enable	0		ns
T13	Data Setup to $\overline{REQ}$ TRUE (Target)	60		ns

*Write Enable is the occurrence of $\overline{IOW}$ and $\overline{DACK}$

Notes: 1. $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$ must be concurrently TRUE for at least T7 for proper recognition of the $\overline{EOP}$ pulse.



WF022380

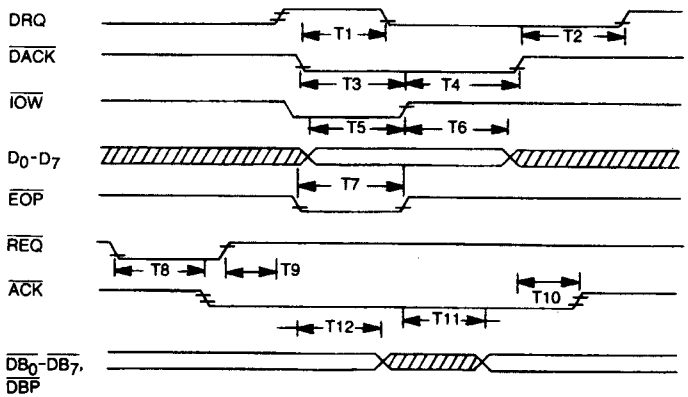
SWITCHING CHARACTERISTICS/WAVEFORMS (Cont'd.)

DMA Write (Non-Block Mode) Initiator Send Cycle

Name	Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		100	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	Write Enable Width*	70		ns
T4	$\overline{DACK}$ Hold from End of $\overline{IOW}$	0		ns
T5	Data Setup to End of Write Enable*	30		ns
T6	Data Hold Time from End of $\overline{IOW}$	40		ns
T7	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T8	$\overline{REQ}$ TRUE to $\overline{ACK}$ TRUE		110	ns
T9	$\overline{REQ}$ FALSE to DRQ TRUE		110	ns
T10	$\overline{DACK}$ FALSE to $\overline{ACK}$ FALSE		130	ns
T11	$\overline{IOW}$ FALSE to Valid SCSI Data		100	ns
T12	Data Hold from Write Enable	0		ns

*Write Enable is the occurrence of $\overline{IOW}$ and $\overline{DACK}$

Notes: 1. $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$ must be concurrently TRUE for at least T7 for proper recognition of the $\overline{EOP}$ pulse.



WF022390

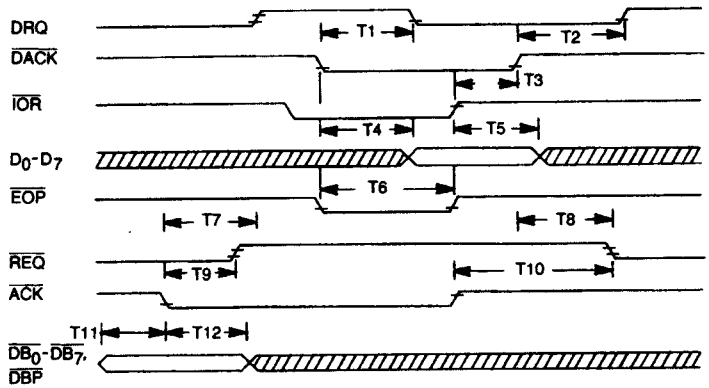
SWITCHING CHARACTERISTICS/WAVEFORMS (Cont'd.)

DMA Read (Non-Block Mode) Target Receive Cycle

Name	Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		100	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	$\overline{DACK}$ Hold Time from End of $\overline{IOR}$	0		ns
T4	Data Access Time from Read Enable*		100	ns
T5	Data Hold Time from End of $\overline{IOR}$			ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T7	$\overline{ACK}$ TRUE to DRQ TRUE		110	ns
T8	$\overline{DACK}$ FALSE to $\overline{REQ}$ TRUE ($\overline{ACK}$ FALSE)		120	ns
T9	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		125	ns
T10	$\overline{ACK}$ FALSE to $\overline{REQ}$ TRUE ($\overline{DACK}$ FALSE)		120	ns
T11	Data Setup Time to $\overline{ACK}$	20		ns
T12	Data Hold Time from $\overline{ACK}$	50		ns

*Read Enable is the occurrence of $\overline{IOR}$ and $\overline{DACK}$

Notes: 1. $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$ must be concurrently TRUE for at least T6 for proper recognition of the $\overline{EOP}$ pulse.



WF022400

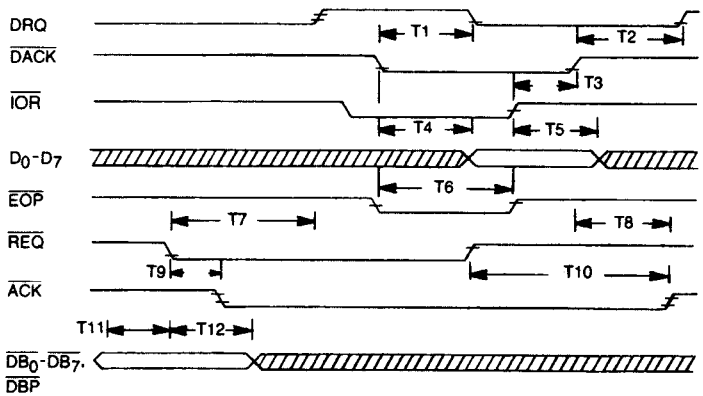
SWITCHING CHARACTERISTICS/WAVEFORMS (Cont'd.)

DMA Read (Non-Block Mode) Initiator Receive Cycle

Name	Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		100	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	$\overline{DACK}$ Hold Time from End of $\overline{IOR}$	0		ns
T4	Data Access Time from Read Enable*		100	ns
T5	Data Hold Time from End of $\overline{IOR}$	0		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T7	$\overline{REQ}$ TRUE to DRQ TRUE		140	ns
T8	$\overline{DACK}$ FALSE to $\overline{ACK}$ FALSE ($\overline{REQ}$ FALSE)		100	ns
T9	$\overline{REQ}$ TRUE to $\overline{ACK}$ TRUE		110	ns
T10	$\overline{REQ}$ FALSE to $\overline{ACK}$ FALSE ($\overline{DACK}$ FALSE)		100	ns
T11	Data Setup Time to $\overline{REQ}$	20		ns
T12	Data Hold Time from $\overline{REQ}$	50		ns

*Read Enable is the occurrence of $\overline{IOR}$ and $\overline{DACK}$

Notes: 1. $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$ must be concurrently TRUE for at least T6 for proper recognition of the $\overline{EOP}$ pulse.



WF022410

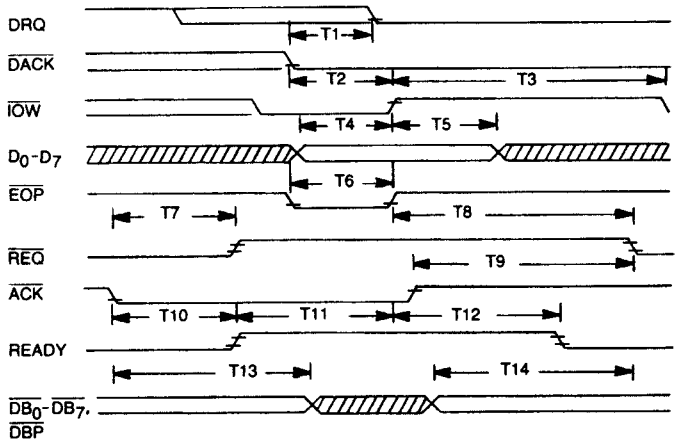
SWITCHING CHARACTERISTICS/WAVEFORMS (Cont'd.)

DMA Write (Block Mode) Target Send Cycle

Name	Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		100	ns
T2	Write Enable Width*	70		ns
T3	Write Recovery Time	120		ns
T4	Data Setup to End of Write Enable*	30		ns
T5	Data Hold Time from End of $\overline{IOW}$	40		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T7	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		120	ns
T8	$\overline{REQ}$ from End of $\overline{IOW}$ ($\overline{ACK}$ FALSE)		130	ns
T9	$\overline{REQ}$ from End of $\overline{ACK}$ ($\overline{IOW}$ FALSE)		110	ns
T10	$\overline{ACK}$ TRUE to READY TRUE		140	ns
T11	READY TRUE to $\overline{IOW}$ FALSE	70		ns
T12	$\overline{IOW}$ FALSE to READY FALSE		120	ns
T13	Data Hold from $\overline{ACK}$ TRUE	0		ns
T14	Data Setup to $\overline{REQ}$ TRUE	60		ns

*Write Enable is the occurrence of $\overline{IOW}$ and $\overline{DACK}$

Notes: 1. $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$ must be concurrently TRUE for at least T6 for proper recognition of the $\overline{EOP}$ pulse.



WF022420

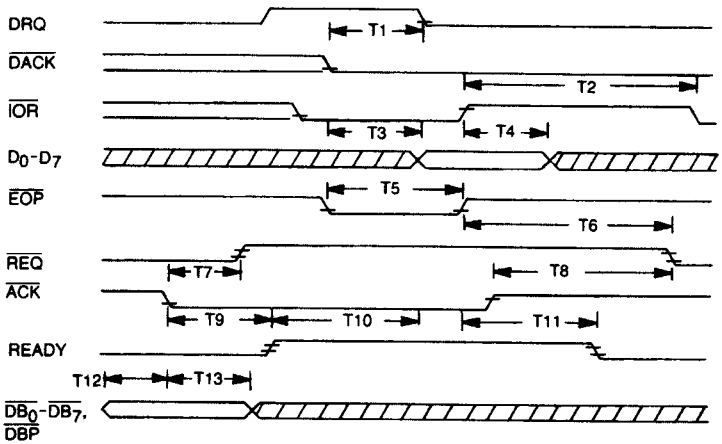
SWITCHING CHARACTERISTICS/WAVEFORMS (Cont'd.)

DMA Read (Block Mode) Target Receive Cycle

Name	Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		100	ns
T2	$\overline{IOR}$ Recovery Time	120		ns
T3	Data Access Time from Read Enable*		100	ns
T4	Data Hold Time from End of $\overline{IOR}$	0		ns
T5	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T6	$\overline{IOR}$ FALSE to $\overline{REQ}$ TRUE ($\overline{ACK}$ FALSE)		130	ns
T7	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		125	ns
T8	$\overline{ACK}$ FALSE to $\overline{REQ}$ TRUE ($\overline{IOR}$ FALSE)		110	ns
T9	$\overline{ACK}$ TRUE to READY TRUE		140	ns
T10	READY TRUE to Valid Data		50	ns
T11	$\overline{IOR}$ FALSE to READY FALSE		120	ns
T12	Data Setup Time to $\overline{ACK}$	20		ns
T13	Data Hold Time from $\overline{ACK}$	50		ns

*Read Enable is the occurrence of $\overline{IOR}$ and $\overline{DACK}$

Notes: 1. $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$ must be concurrently TRUE for at least T5 for proper recognition of the $\overline{EOP}$ pulse.

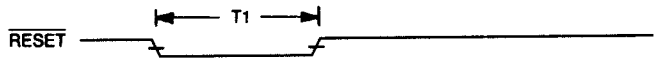


WF022430

SWITCHING CHARACTERISTICS/WAVEFORMS

Reset

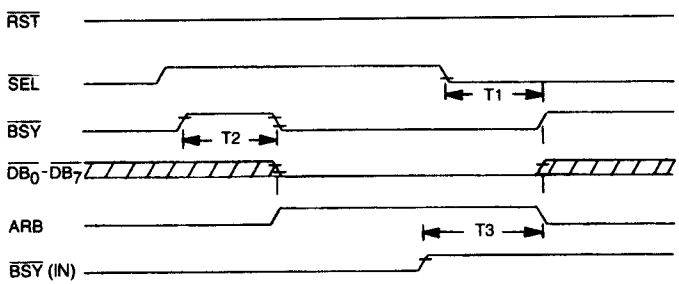
Name	Description	Min.	Max.	Unit
T1	Minimum Width of Reset	100		ns



WF022450

Arbitration

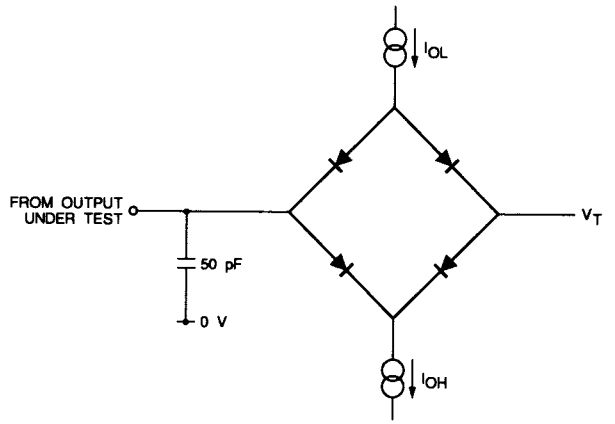
Name	Description	Min.	Max.	Unit
T1	Bus Clear from $\overline{SEL}$ TRUE		600	ns
T2	Arbitrate Start from $\overline{BSY}$ FALSE	1200	2200	ns
T3	Bus Clear from $\overline{BSY}$ FALSE		1100	ns



WF022440

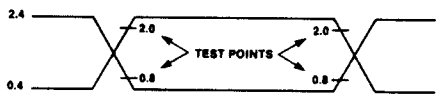
4

SWITCHING TEST CIRCUIT



TC003860

SWITCHING TEST WAVEFORM



WF009541

APPENDIX A — DESIGN MODIFICATIONS IN Am53C80N

Spurious RST Interrupts

If Am5380 is not terminated on the SCSI Interface, the floating input of the $\overline{RST}$ signal can generate spurious interrupts.

Am53C80N has 35 μA pull up on the $\overline{RST}$ signal which prevents the spurious interrupts caused by an unterminated SCSI Bus Interface.

The End of DMA for Send Operations

While sending the data to Am5380, if $\overline{EOP}$ is asserted on the last byte, the End of DMA Status Bit indicates that the last byte has been received from the DMA device; there is no indication that the last byte has been transferred to the SCSI Bus.

The Am53C80N uses Bit 7 of the Target Command Register to indicate that the last byte has been transferred to the SCSI Bus.

Faster $\overline{REQ}/\overline{ACK}$ Transition Times

The Am53C80N has faster $\overline{REQ}/\overline{ACK}$ handshake to improve overall data transfer rates.

Prevents the Possibility of an Additional $\overline{ACK}$ from Occurring

The Am5380, upon receipt of an $\overline{EOP}$ signal, sets the End of DMA Status Bit and prevents additional DMA requests; it does not reset the DMA Mode Bit. If receiving data as an initiator and the target continues to request data for the same bus phase after receiving an $\overline{EOP}$ pulse, the Am5380 will assert $\overline{ACK}$ without issuing DRQ.

The Am53C80N prevents $\overline{ACK}$ from being asserted until the device is instructed to continue by writing the Start DMA Initiator Receive Register.

Am5380/Am53C80N ERRATA

1) Edge triggered $\overline{RST}$ Interrupt — If the SCSI Bus is not terminated, the $\overline{RST}$ interrupt is continually generated.

2) TRUE End of DMA Interrupt — The Am5380/Am53C80N generates an interrupt when it receives the last byte from the DMA, not when the last byte is transferred to the SCSI Bus.

3) Return to READY after $\overline{EOP}$ Interrupt — When operating in Block mode DMA, the Am5380/Am53C80N does not return the READY signal to a Ready condition. This locks up the bus and prevents the CPU from executing.

4) SCSI handshake clean up after $\overline{EOP}$ Interrupt — Currently the $\overline{ACK}$ remains active after the $\overline{EOP}$ Interrupt is generated and must be turned off for the Send operations.

5) SCSI handshake after $\overline{EOP}$ occurs — If an $\overline{EOP}$ occurs when receiving data, a subsequent $\overline{REQ}$ will cause $\overline{ACK}$ to be asserted even though no DRQ is issued.

6) During Reselection, if the Target Command Register does not reflect the current bus phases (most likely Data Out), the Reselection interrupt may get reset.

7) A phase-mismatch interrupt is not guaranteed after a Reselection for the following reasons:

- DMA MODE bit must be set in order to receive a phase-mismatch interrupt
- DMA MODE bit cannot be set unless $\overline{BSY}$ is active
- $\overline{BSY}$ cannot be asserted until after the Reselection has occurred
- Once $\overline{BSY}$ is asserted, the Target may assert $\overline{REQ}$ in less than 500 ns
- The phase-mismatch interrupt is generated on the active edge of $\overline{REQ}$. If the DMA MODE bit is not set before the $\overline{REQ}$ goes active, the phase-mismatch interrupt will not occur