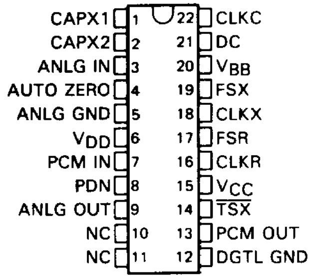
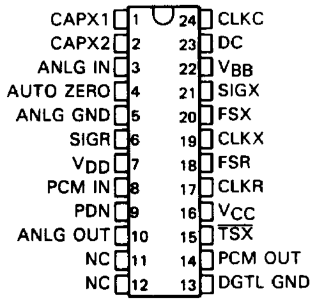
D2664, JUNE 1982—REVISED MARCH 1986

- **TCM2909 Provides μ-Law Companding In 22-Pin Package**
- **TCM2910A is Designed to be Interchangeable with Intel 2910A**
- **Compatible with CCITT Recommendations G.711 and G.712**
- **μ-255-Law Encoding and 8th-bit Signaling (TCM2910A only) Compatible with AT&T D-Type Channel Banks**
- **TTL-Compatible Digital Inputs and Outputs**
- **Optional Programmable Time-Slot Selection**
- **Low Operating Power Consumption:**
  Active . . . . 230 mW Typical
  Power-Down Mode . . . . . 33 mW Typical
- **±5% Power Supplies: +12 V, +5 V, −5 V**
- **High-Reliability, Advanced N-Channel MOS Technology**
- **Low External Component Count**
- **PEP Processing Available**

TCM2909
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM2910A
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

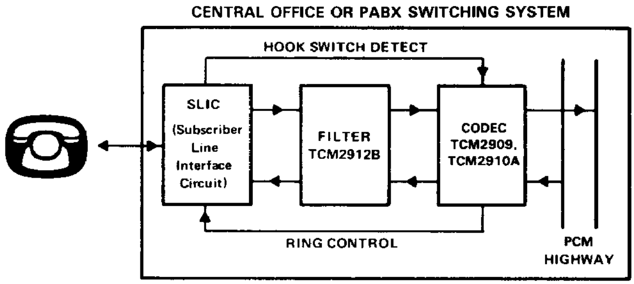
description

The TCM2909 and TCM2910A are single-chip pulse-code-modulated encoders/decoders (PCM codecs) that provide all the functions required to interface a full duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. Integrated into the codecs are circuits for signaling interface, PCM time-slot control logic, analog-to-digital (A/D) conversion, and digital-to-analog (D/A) conversion. Primary applications of the devices include:

- Line interface for digital transmission and switching of T1 Carrier, PABX, and Central Office telephone systems
- Subscriber line concentrators
- Digital encryption systems
- Digital voice-band data storage systems
- Digital signal processing

The TCM2909 and TCM2910A are characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



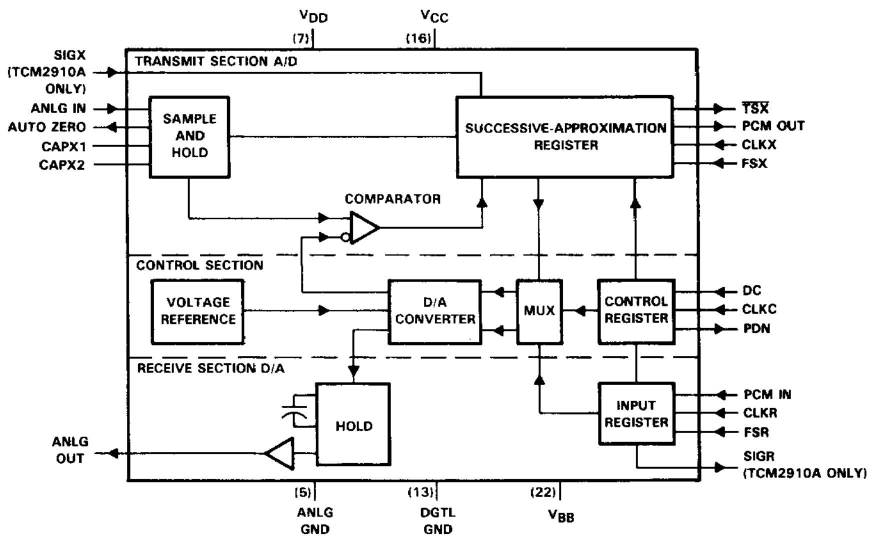
functional description

The TCM2909 and TCM2910A are designed to perform the transmit (encoding or A/D conversion) and receive (decoding or D/A) conversion) functions in a pulse-code-modulated system.

The functions of the codec are control, transmit, and receive. The control section consists of a precision voltage reference, a digital-to-analog converter, a multiplexer, and a control register. The voltage reference supplies the D/A-converter resistor ladder network with an accurate, stable reference. The analog output, in turn, is used to determine the A/D output as well as the D/A output. The control register multiplexes incoming receive and outgoing transmit data into the D/A converter.

The control section also enhances the basic codec function with programmable time-slot allocation and power-down circuits. These circuits allow dynamic allocation of both receive and transmit time slots. In small systems this feature could significantly reduce per-channel hardware for the first level of switching. In larger systems the time-slot selection circuits can be disabled, and time-slot allocation can be performed at a common system location. With either system design, the codec can be powered down during periods of inactivity, thereby significantly reducing average system power consumption.

functional block diagram



NAME	PIN TCM2909	PIN TCM2910A	DESCRIPTION
ANLG GND	5	5	Analog return common to the transmit and receive analog circuits. Not connected to DGTL GND internally.
ANLG IN	3	3	Analog input to be encoded into a PCM word. The signal on this pin is sampled at the same rate as the transmit frame synchronization pulse, FSX, and the sample value is held in the external capacitors connected at the CAPX1 and CAPX2 pins.
ANLG OUT	9	10	Analog output. The voltage present on this pin is the decoded value of the PCM word received on PCM IN and is held constant between two conversions.
AUTO ZERO	4	4	This output is the same as the most significant bit of the encoded PCM word (5 V for negative, −5 V for positive inputs).
CAPX1	1	1	Connection for the transmit holding (analog sampling) capacitor.
CAPX2	2	2	Connection for the transmit holding (analog sampling) capacitor.
CLKC	22	24	Clock input to clock in the data on the DC pin that defines the mode of operation of the codec. When CLKC is connected to V_{CC}, DC becomes an active-low chip select. TTL-compatible.
CLKR	16	17	Clock input that defines the bit rate on the receive PCM highway (1.544 megabits per second for a T1 carrier). The maximum rate is 2.1 megabits per second at 50% duty cycle. TTL-compatible.
CLKX	18	19	Transmit clock input defining the bit rate on the transmit PCM highway. It is typically 1.544 megabits per second. Maximum rate is 2.1 megabits per second at 50% cycle. TTL-compatible.
DC	21	23	Data input to program the codec for either the direct or microcomputer mode of operation. TTL-compatible.
DGTL GND	12	13	Ground return common to the logic power supply, V_{CC}.
FSR	17	18	Frame synchronization pulse for the receive PCM highway. Resets the internal time-slot counter for the receive section. Maximum frame synchronization repetition rate is 12 kHz. Also used to differentiate between nonsignaling frames and signaling frames for the receive side. TTL-compatible.
FSX	19	20	Frame synchronization pulse for the transmit PCM highway. Resets the internal time-slot counter for the transmit section. Maximum repetition rate is 12 kHz. Also used to differentiate between nonsignaling frames and signaling frames on the transmit section. TTL-compatible.
NC	10	11	No internal connection. It is recommended that this pin be connected to ANLG GND.
NC	11	12	No internal connection. It is recommended that this pin be connected to ANLG GND.
PCM IN	7	8	Receive PCM highway (serial bus) interface. The codec serially receives a PCM word (8 bits) through this pin at the time defined by FSR, CLKR, and the contents of the receive control register.
PCM OUT	13	14	Output of the encoder onto the PCM highway. The 8-bit PCM word is serially sent out as defined by FSX, CLKX, and the control register. TTL three-state output capable of driving two TTL loads (4 mA).
PDN	8	9	Power-down output is active (high) when the codec is in the power-down state. The open-drain output is capable of sinking one TTL load (1.6 mA).
SIGR		6	Signaling output SIGR is updated with the 8th bit of the receive PCM word on signaling frames, and is latched between two signaling frames. TTL-compatible.
SIGX		21	Signaling input. This digital input is transmitted as the 8th bit of the PCM word on the PCM OUT pin in signaling frames. TTL-compatible.
$\overline{TSX}$	14	15	Normally high, the transmit time-slot output goes low while the codec is transmitting a PCM word on PCM OUT. Time-slot information is used for diagnostic purposes and also to gate the data on the PCM OUT pin to the PCM transmit highway. The open-drain output is capable of sinking two TTL loads (3.2 mA).
V_{BB}	20	22	Supply voltage (−5 V ±5%) referenced to ANLG GND.
V_{CC}	15	16	Supply voltage (5 V ±5%) referenced to DGTL GND.
V_{DD}	6	7	Supply voltage (12 V ±5%) referenced to ANLG GND.

operation

The TCM2909 and TCM2910A are capable of operating as transmitters and receivers in any of the 64 channels of a PCM system. The receive and transmit sections can be assigned to the same channel (time slot) or to different channels, and assignments can be changed under microcomputer control to meet changing system needs. Table 1 shows the control options.

TABLE 1. OPERATION CONTROL CONFIGURATIONS

CONTROL SIGNALS		OPERATION
CLKC	DC	
L	X	Undefined operation
V_{CC}	H	Power-down or standby operational status
V_{CC}	L	Direct-control operation. Receive and transmit in the first time slot.
↓	X	Microcomputer-control operation. Clock in one of 8 bits of the control word at the DC input.

Bits 1 and 2		(See Figure 3)
0	0	Load bits 3 through 8 into transmit and receive time-slot counters.
0	1	Load bits 3 through 8 into transmit counter only.
1	0	Load bits 3 through 8 into receive counter only.
1	1	Power down (Bits 3 through 8 are irrelevant).

Bits 3 through 8 for time-slot assignments 1 through 64. The time-slot numbers equal one more than the decimal equivalent represented by bits 3 (MSB) through 8 (LSB) using positive logic.

Time slot	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
1	0	0	0	0	0	0
2	0	0	0	0	0	1
•	•	•	•	•	•	•
6	0	0	0	1	0	1
•	•	•	•	•	•	•
63	1	1	1	1	1	0
64	1	1	1	1	1	1

H = high level, L = low level, see digital interface table.
X = irrelevant, ↓ = V_{CC}-to-low transition.

In microcomputer control operation, the control word at DC is divided into a mode selection (bits 1 and 2) and a time-slot assignment (bits 3 through 8). In mode 00 both the receive and transmit time-slot counters are addressed, and they both receive the same subsequent 6-bit time-slot assignment. In mode 01 the transmit time-slot counter is addressed for time-slot assignment. Mode 10 assigns a time-slot only for the receive section. Mode 11 puts the device in the standby operational status and ignores the remaining 6 bits of the control word. Specific functional considerations for microcomputer-control operation are:

- All 8 negative-going transitions of CLKC must occur within 125 microseconds for the frame rate of 8 kilobits per second. The first transition of CLKC may occur anywhere within a frame. The CLKC pin should be a TTL low level after time-slot assignment is completed.
- A dead period of 250 microseconds (2 frames) must be observed between the first positive transition of CLKC in a time-slot assignment and that of any subsequent time-slot assignment.
- It is recommended that either mode 00 or mode 01 be transmitted to the control register during power-up or system initialization to ensure that a valid time-slot is always transmitted.

- The receive or the transmit section of the codec will operate only after both sections have been assigned a time-slot. Therefore, transmit-only and receive-only time-slot allocation is not allowed.
- Clocking the control register while the codec is active may cause an increase in idle-channel noise.

Direct-control operation is implemented by connecting the CLKC pin to +5 volts (V_{CC}) and using the DC pin as the chip select pin. When the DC pin is held low, the device transmits in the channel following FSX and receives in the channel following FSR. On the other hand, when the DC pin is held high, the device is in the power-down state. Operational considerations for direct time-slot allocation are:

- At least two framing pulses must occur after DC goes low to ensure that the codec is in direct-control status.
- Three frames (375 microseconds) are required to enter direct operation after power supply requirements are met and all clocks are available.
- After DC is brought high, two framing pulses are required to put the codec into the standby mode.
- The TCM2909 or TCM2910A can replace a 2910 codec even though the CLKC characteristics are not the same for the two devices.

encoding mode

The analog input signal sampled at the ANLG IN pin is held by an external capacitor on pins CAPX1 and CAPX2. This sampling is done synchronously with the transmit time-slot assigned to the device. The eight-bit digital PCM word will be transmitted on the PCM OUT pin in the frame immediately following the frame in which the analog signal was sampled. See Table 3.

decoding mode

When the assigned receive time-slot occurs, the eight-bit digital PCM word is retrieved from the PCM highway on the PCM IN pin. The word is converted from digital to analog and held with an internal capacitor until the next assigned receive time-slot update. See Table 3.

signaling

These devices are compatible with per-channel signaling and are capable of differentiating between the signaling and nonsignaling frames. A signaling frame is one in which the eighth bit of the PCM word contains signaling information while the seven most significant bits are normal information bits. The signaling frame is designated by the framing pulse (FSX or FSR) whose length is extended to two full clock periods as shown in the timing diagrams. A framing pulse of a nonsignaling frame is one full clock period in length. During a transmit signaling frame, the level present on the SIGX pin (of the TCM2910A) is substituted for the 8th bit of the PCM word. During a receive signaling frame the value of the 8th bit of the PCM word of the receive channel will be put on the SIGR pin (of the TCM2910A) and the signal level will remain unchanged until it is updated by the next signaling frame. The remaining 7 bits will be decoded according to the procedure in CCITT Recommendation G.733. See Figure 1 and Figure 2 for transmit and receive timing diagrams.

framing

These devices are compatible with the D3/D4 framing format (T1 framing), which inserts a 193rd bit after the 24th serial channel (8 bits per channel) frame. The extra bit raises the clock frequency (CLKX and CLKR) from 1.536 MHz to 1.544 MHz.

standby operation

The codec provides for powering down to standby status from both microcomputer-control and direct-control operation. The power consumption is reduced from 230 mW to 33 mW. Standby operation results in the powering down of all the codec functions except the DC, CLKC, SIGX†, SIGR†, and PDN inputs. Also, PCM OUT is forced into a high-impedance state thus helping to ensure that the PCM bus will not be driven. The SIGR† output is held low to provide a known condition until changed by a signaling frame after reactivation.

In microcomputer-control operation, the power-down state is invoked by clocking in 11 at the DC inputs as described in Table 1. In direct operation the power-down state is called by taking the DC pin high and connecting clock CLKC pin to V_{CC}. Recovery from the power-down condition is accomplished by forcing DC to the low level and allowing at least 2 frame synchronization pulses to occur.

internal reset

The TCM2909 and TCM2910A are designed to aid the user by eliminating certain system power-interruption problems. Three of the most common of these problems are:

(1) Plugging a card into a "hot" system thus causing spikes on the common power supplies
(2) Various transients such as caused by duplicated power supply faults or power feeder faults
(3) Transients and spikes that result from turning the power supplies on.

These devices are tolerant of transients in the negative power supply (V_{BB}) provided that V_{BB} remains more negative than −3.5 volts. The device will go into the power-down (standby) status if, during power up (single-card or system), V_{CC} or V_{DD} is supplied after V_{BB} or if a transient causes the positive power supplies to drop below approximately 2 volts. Since $\overline{TSX}$ is inhibited in standby operation, any codec in this status can be detected easily.

companding

The amplitude distribution of a speech message is not uniform. Moreover, the probability of occurrence for a small amplitude is greater than the probability for large amplitudes. Advantage can be taken of this fact by "compressing" digital resolution into the lower signal amplitude during transmission and "expanding" the signal upon the reception, thus increasing the overall signal-to-noise ratio. CCITT has defined this function and entitled it the μ-law.

$$f(x) = \text{sgn}(x) \frac{\ln + [1 + \mu|x|]}{\ln (1 + \mu)} \quad \text{for: } -1 \le x \le 1$$

where $\mu = 255$, x is the normalized input, and sgn(x) is the sign of x. A continuous implementation of f(x) would be impossible, therefore a piecewise continuous approximation of f(x) is used. The approximation divides the function into 16 segments, and each segment is divided into 16 equal intervals except for the first interval of the first segment. Refer to CCITT Recommendation G.711 for the segment and interval implementation details of the μ-law used for these circuits.

† TCM2910A only

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings

V_{CC}, V_{DD}, ANLG GND, and DGTL GND with respect to V_{BB} . . . . −0.3 V to 20 V
All inputs and outputs with respect to V_{BB} . . . . −0.3 V to 20 V
Temperature under bias . . . . −10°C to 80°C
Storage temperature range . . . . −65°C to 150°C

NOTE: Stresses in excess of absolute maximum ratings may permanently damage the device. Functional operation outside the recommended operating conditions is not guaranteed. Prolonged exposure to absolute maximum ratings may have an adverse effect on device characteristics.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	11.4	12	12.6	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Ground voltages (ANLG GND and DGTL GND)		0		V
Auto-zero resistor, R1 (see Figures 9 and 10)			150	kΩ
Auto-zero resistor, R2 (see Figures 9 and 10)			330	Ω
Auto-zero resistor, R3 (see Figures 9 and 10)			470	kΩ
Analog coupling capacitor, C1 (see Figures 9 and 10)			0.1	μF
Analog coupling capacitor, C2 (see Figure 10)			0.3	μF
Analog sampling capacitor, CAPX, for 8-kHz sampling rate (see Figures 9 and 10)	1600	2000	2400	pF
Operating free-air temperature, T_A	0		70	°C

NOTE 1: Voltages at the analog input, analog output, and V_{DD} terminals are with respect to the analog ground terminal. All other voltages are referenced to the digital ground terminal unless otherwise noted.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.6	V
I_{IH}	High-level input current		V_I = 5.5 V		10	μA
I_{IL}	Low-level input current		V_I = 0 V		−10	μA
V_{OH}	High-level output voltage (see Note 2)	PCM OUT	I_{OH} = 15 mA	2.4		V
		SIGR†	I_{OH} = 80 μA	2.4		
V_{OL}	Low-level output voltage	PCM OUT	I_{OL} = 4 mA		0.4	V
		SIGR†	I_{OL} = 0.5 mA		0.4	
		PDN	I_{OL} = 1.6 mA		0.4	
		$\overline{TSX}$	I_{OL} = 3.2 mA		0.4	

analog interface

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Analog-input impedance (between ANLG IN and CAPX1) in series with CAPX to ANLG GND during sampling of ANLG IN	V_I = −3.1 V to 3.1 V	125	300	500	Ω
Small-signal impedance at ANLG OUT	V_O = −3.1 V to 3.1 V	100	180	300	Ω
Decoder output offset voltage	Serial 11111111 to PCM IN	−50		50	mV
Encoder input offset voltage (see Note 3)	Serial 11111111 from PCM OUT	−5	1.5	5	mV
Peak negative output voltage at auto zero§	400 kΩ to ANLG GND	$V_{BB}+2$	V_{BB}		V
Peak positive output voltage at auto zero		$V_{CC}-2$	V_{CC}		V

power supplies

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{DD1}	V_{DD} standby current	V_{DD} = 12.6 V, V_{CC} = 5.25 V, V_{BB} = −4.75 V, f_{CLK} = 2.048 MHz, See Note 4		0.7	1.1	mA
I_{CC1}	V_{CC} standby current			4	7	mA
I_{BB1}	V_{BB} standby current			−1.4	−2.5	mA
I_{DD2}	V_{DD} operating current			11	16	mA
I_{CC2}	V_{CC} operating current			13	21	mA
I_{BB2}	V_{BB} operating current			−4	−7.5	mA

† TCM2910A only.
‡ Typical values are at V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
§ Limits are expressed as magnitudes. For example, if V_{BB} = −5 V, the typical value is −5 V and the minimum value is −3 V.

NOTES: 2. PDN and $\overline{TSX}$ outputs are open-drain n-channel transistors that only sink current to DGTL GND. External pull-up devices are required to source current.
3. External auto-zero must be used when the required input offset is less than ±4 code steps or approximately 2.7 mV. The external auto-zero circuit shown in Figure 10 will bias the codec at the zero-crossing point and reduce the input offset voltage to zero.
4. These measurements apply to the microcomputer and direct modes. All output pins are left open, the dc input (pin 23) is at 5 V for standby current and at 0 V for operating current. All other input pins are grounded with the clocks operating.

operating characteristics over recommended ranges of supply voltages and operating free-air temperature, R_L = 600 Ω (unless otherwise noted)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Digital milliwatt response	Nominal supply voltages, T_A = 25°C, See Note 5 and Figure 6	5.53	5.63	5.73	dBm
Temperature coefficient of digital milliwatt response	Nominal supply voltages, See Note 5		−0.001	−0.002	dB/°C
Change in digital milliwatt response	Supply voltages changing ±5%, T_A = 25°C, See Note 5			±0.07	dB
RMS input dynamic voltage range using dc and ac tests	Nominal supply voltages, T_A = 25°C, See Note 6 and Figure 6	2.17	2.20	2.23	V
Temperature coefficient of RMS input dynamic voltage range	Nominal supply voltages, See Note 6			−0.5	mV/°C
Change in RMS input dynamic voltage range	Supply voltages changing ±5%, T_A = 25°C, See Note 6			±18	mV
RMS output dynamic voltage range	Nominal supply voltages, T_A = 25°C	2.13	2.16	2.19	V
Temperature coefficient of RMS output dynamic voltage range	Nominal supply voltages			−0.5	mV/°C
Change in RMS output dynamic voltage range	Supply voltages changing ±5%, T_A = 25°C			±18	mV
Self-loop gain	P_I = 0 dBm0 at 1.02 kHz, See Note 7 and Figure 5		−0.2		dB

† Typical values are at V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

NOTES: 5. The input to PCM IN is a repetitive digital word sequence specified in CCITT Recommendation G.711. Measurement is made at ANLG OUT. Limits are not corrected for (six x)/x degradation and no C-message-weighted filter is used. See Table 2.

6. In the dc procedure, the positive and negative clipping levels are measured and dynamic voltage range is calculated. In the ac procedure, a sinusoidal input signal to ANLG IN is used and input dynamic voltage range is measured directly.

7. The codec acts as both encoder and decoder (PCM OUT = PCM IN) in a digital loop-back configuration. Specified gain is in addition to normal (sin x)/x insertion loss. See Note 8.

8. In the term (sin x)/x

$$x = \pi \frac{\text{measurement frequency}}{\text{sampling frequency}}$$

gain tracking error at f = 1.02 kHz

PARAMETER	TEST CONDITIONS	MOST NEG.	MOST POS.	UNIT
End-to-end gain tracking error (see Figure 4)	P_I = −37 dBm0 to 0 dBm0	−0.4	0.4	dB
	P_I = −50 dBm0 to −37 dBm0	−0.8	0.8	
	P_I = −55 dBm0 to −50 dBm0	−2.4	2.4	
Half-channel gain tracking error (encoder only with ideal decoder) See Figure 6	P_I = −37 dBm0 to 0 dBm0	−0.3	0.3	dB
	P_I = −50 dBm0 to −37 dBm0	−0.9	0.9	
	P_I = −55 dBm0 to −50 dBm0	−1.5	1.5	
Half-channel gain tracking error (decoder only with ideal encoder) See Figure 6	P_I = −37 dBm0 to 0 dBm0	−0.3	0.3	dB
	P_I = −50 dBm0 to −37 dBm0	−0.9	0.9	
	P_I = −55 dBm0 to −50 dBm0	−1.5	1.5	

operating characateristics over recommended ranges of supply voltages and operating free-air temperature, R_L = 600 Ω (unless otherwise noted) (continued)

transmission characteristics (see Figure 6), f = 1.02 kHz (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
Signal-to-total-distortion ratio, C-message weighting, end-to-end		See Figure 7			
Signal-to-total-distortion ratio, C-message weighting, (half-channel)		See Figures 6 & 7			
Harmonic distortion (2nd or 3rd overtone) measured at ANLG OUT, P_I = 0 dBm0 See Figure 6.			−48	−44	dB
Encoder idle-channel noise measured at mid-tread (no quantizing noise) C-message weighting with no signaling	No external auto zero See Figure 9		2	10	dBrnc0
	With external auto zero See Figure 10		8		dBrnc0
Encoder idle-channel noise measured at the riser (quantizing noise included) C-message weighting, no signaling				17	dBrnc0
Encoder idle-channel noise measured at mid-tread (no quantizing noise), C-message weighting, 6th and 12th frame signaling per AT&T System requirements	No external auto zero See Figure 9		10	13	dBrnc0
	With external auto zero See Figure 10		13		dBrnc0
Decoder idle-channel noise, no sign-bit toggling, no signaling, quiet code (serial 11111111 to PCM IN)			−10	7	dBrnc0
Decoder idle-channel noise with sign-bit toggling, no signaling, quiet code (serial 11111111 to PCM IN)			13	17	dBrnc0

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
SVRR1	V_{DD} supply voltage rejection ratio	Decoder alone,	See Note 9	45	55		dB
SVRR2	V_{BB} supply voltage rejection ratio	Decoder alone,	See Note 9	35	38		dB
SVRR3	V_{CC} supply voltage rejection ratio	Decoder alone,	See Note 9	50	80		dB
SVRR4	V_{DD} supply voltage rejection ratio	Encoder alone		50	75		dB
SVRR5	V_{BB} supply voltage rejection ratio	Encoder alone		45	70		dB
SVRR6	V_{CC} supply voltage rejection ratio	Encoder alone		50	85		dB
SVRR7	V_{DD} supply voltage rejection ratio	Self loop,	See Note 10	40	50		dB
SVRR8	V_{BB} supply voltage rejection ratio	Self loop,	See Note 10	35	38		dB
SVRR9	V_{CC} supply voltage rejection ratio	Self loop,	See Note 10	50	80		dB
a_x	Crosstalk attenuation	See Figure 8,	See Note 11	75	>80		dB

clock timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	485		ns
t_r, t_f	Rise and fall times for CLKX, CLKR, and CLKC	5	30	ns
$t_{w(CLK)}$	Clock pulse duration for CLKX, CLKR, and CLKC	215		ns
	Clock duty cycle $[t_{w(CLK)}/t_{c(CLK)}]$ for CLKX and CLKR	45	55	%

† Typical values are for T_A = 25 °C and nominal power supply voltages.

NOTES: 9. With the test device acting as a decoder, a 200-mV peak-to-peak, 1,02 kHz signal is applied to the appropriate supply pin and measurements are made at the remote encoder output with the decoder in idle-channel conditions.

10. With the test device acting as encoder and decoder, a 200-mV peak-to-peak, 1.02-kHz signal is applied to the appropriate supply pin and measurements are made at the decoder output with the encoder in idle-channel conditions.

11. The analog input power is 0 dBm0 at 1.02 kHz and the decoder is under idle-channel conditions. Measurement is made at ANLG OUT.

12. All timing parameters are referenced to 2 V except t_{pd3} and t_{pd5}, which reference a high-impedance state.

transmit timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{conv(X)}$	Analog input conversion time referenced to leading edge of transmit time slot (see Note 13)	20		time slots
$t_{d(FSX)}$	Frame sync delay time	20	150	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge	100		ns

receive timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{conv(R)}$	Analog output update from leading edge of the channel time slot	7 1/16		time slots
$t_{d(FSR)}$	Frame sync delay time	20	150	ns
$t_{su(PCM\ IN)}$	Receive data setup time	20		ns
$t_{h(PCM\ IN)}$	Receive data hold time	60		ns

control (microcomputer operation) timing requirements over recommended ranges of operating conditions

PARAMETER		MIN	MAX	UNIT
$t_{su(DC)}$	Control data setup time	100		ns
$t_{h(DC)}$	Control data hold time	100		ns

propagation delay times over recommended ranges of operating conditions (see Note 12 and timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock Bit 1 to Bit 1 data valid at PCM OUT (data enable time on time-slot entry)	C_L = 0 to 100 pF	50	180	ns
t_{pd2}	From falling edge of transmit clock Bit n to Bit n+1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	80	230	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time-slot exit)	C_L = 0, See Note 13	75	245	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to $\overline{TSX}$ active (low) (time-slot enable time)	C_L = 0 to 100 pF	30	220	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to $\overline{TSX}$ inactive (high) (time-slot disable time)	C_L = 0, See Note 13	70	225	ns
t_{pd6}	From falling edge of receive clock Bit 8 on signaling frames to updated signaling bit on SIGR output (receive signaling update time)			1000	ns

NOTES: 12. All timing parameters are referenced to 2 V except t_{pd3} and t_{pd5}, which reference a high-impedance state.
13. The 20-time-slot minimum ensures that the complete A/D conversion will take place under any combination of receive interrupt of asynchronous operation of the codec. If only the transmit channel is operated, the A/D conversion can be completed in a minimum of 11 time slots.

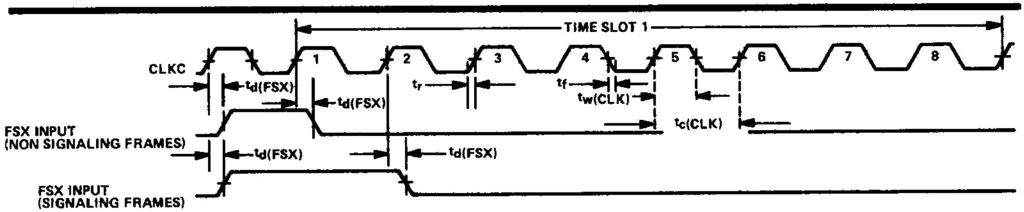


FIGURE 1a. TRANSMIT FRAME SYNCHRONIZATION TIMING

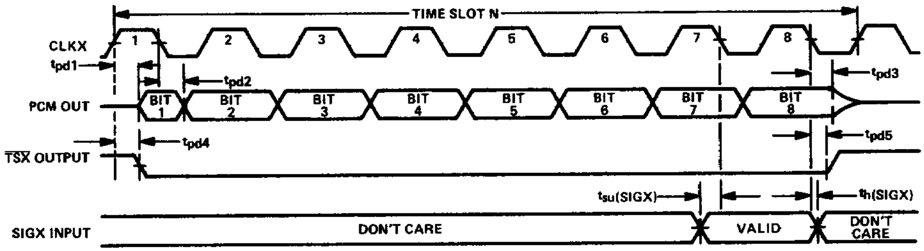


FIGURE 1b. TRANSMIT OUTPUT TIMING

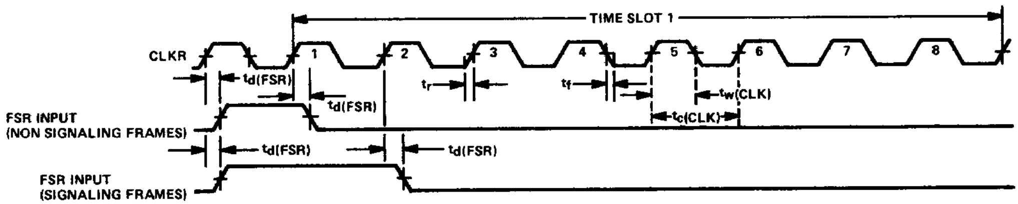


FIGURE 2a. RECEIVE FRAME SYNCHRONIZATION TIMING

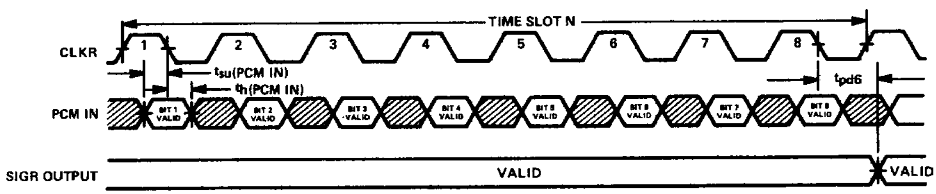


FIGURE 2b. RECEIVE INPUT TIMING

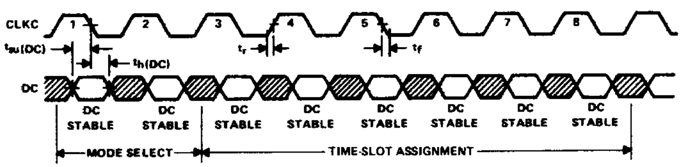


FIGURE 3. CONTROL TIMING

PARAMETER MEASUREMENT INFORMATION

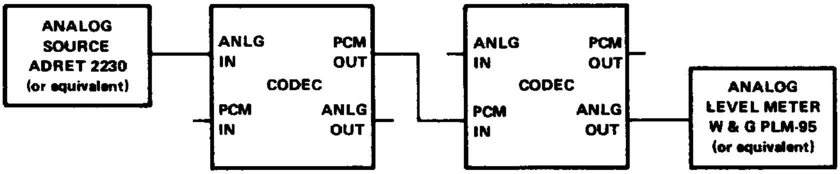


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FIGURE 4. END-TO-END GAIN TEST CIRCUIT

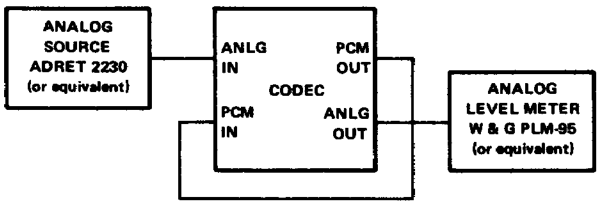

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FIGURE 5. SELF-LOOP GAIN TEST CIRCUIT

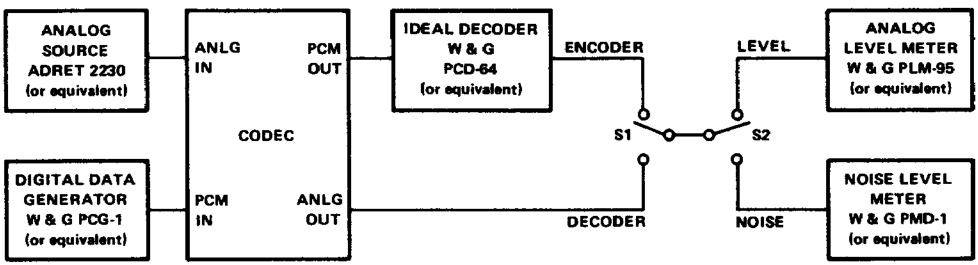

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FIGURE 6. TRANSMISSION PARAMETER TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

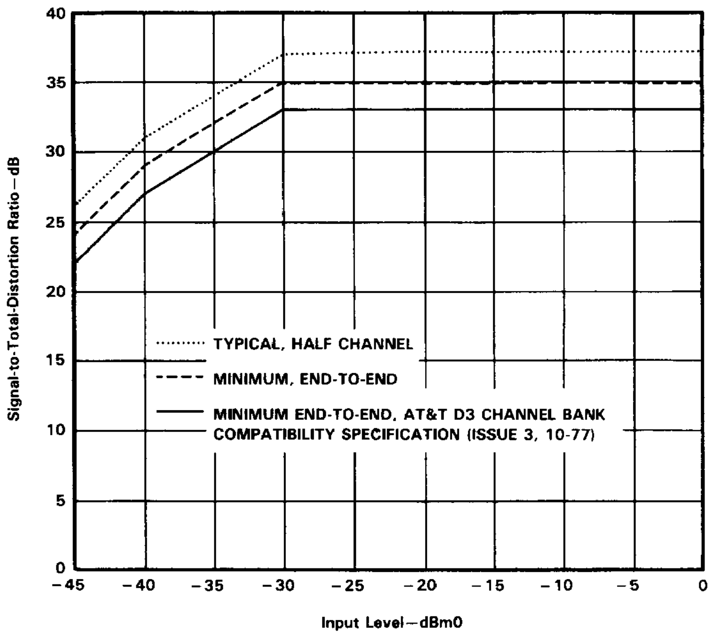

FIGURE 7. SIGNAL-TO-TOTAL DISTORTION RATIO

PARAMETER MEASUREMENT INFORMATION

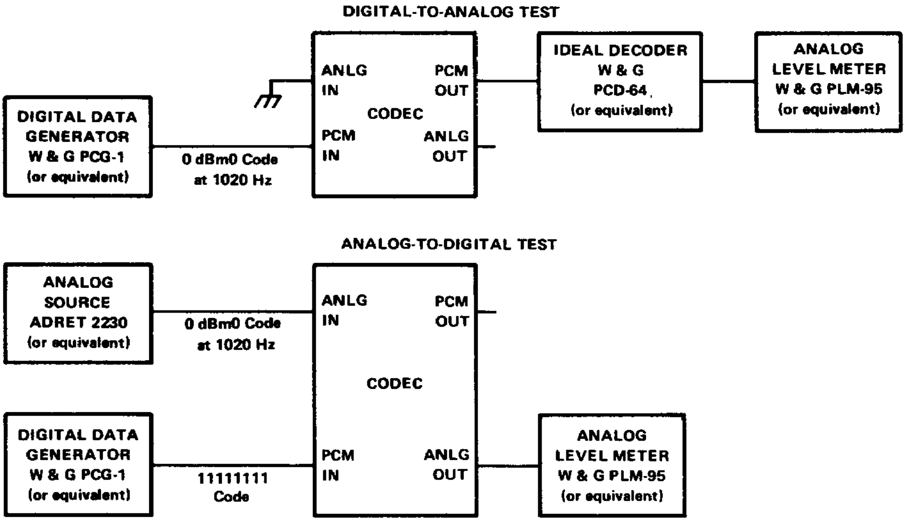

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FIGURE 8. CROSSTALK ATTENUATION TEST CIRCUIT

TABLE 2. μ-LAW DIGITAL WORD SEQUENCE FOR THE DIGITAL MILLIWATT RESPONSE PER CCITT RECOMMENDATION G.711

	Bit Number							
Word Number	1	2	3	4	5	6	7	8
1	0	0	0	1	1	1	1	0
2	0	0	0	0	1	0	1	1
3	0	0	0	0	1	0	1	1
4	0	0	0	1	1	1	1	0
5	1	0	0	1	1	1	1	0
6	1	0	0	0	1	0	1	1
7	1	0	0	0	1	0	1	1
8	1	0	0	1	1	1	1	0

TYPICAL APPLICATION INFORMATION

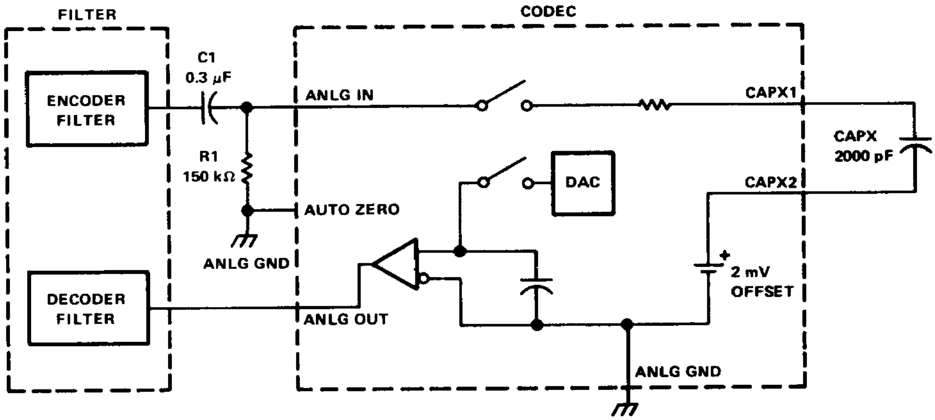

FIGURE 9. ANALOG INTERFACE WITHOUT EXTERNAL AUTO ZERO

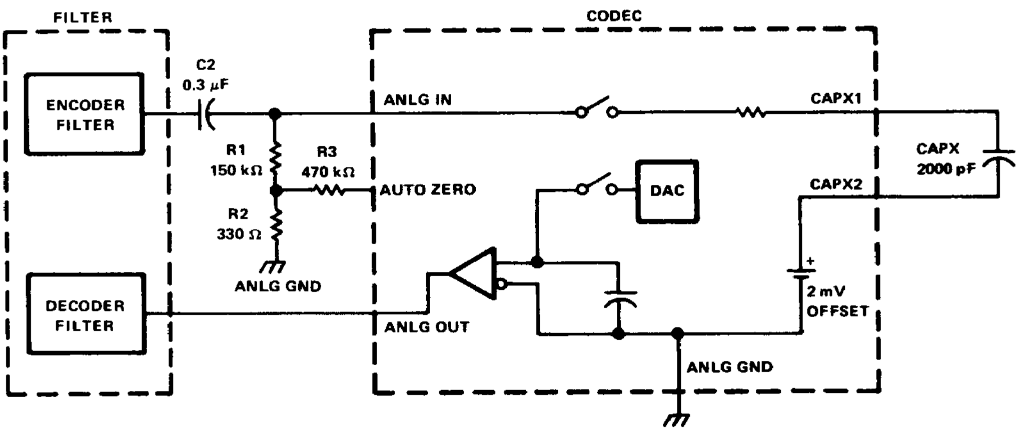

FIGURE 10. ANALOG INTERFACE WITH EXTERNAL AUTO ZERO

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TYPICAL APPLICATION INFORMATION

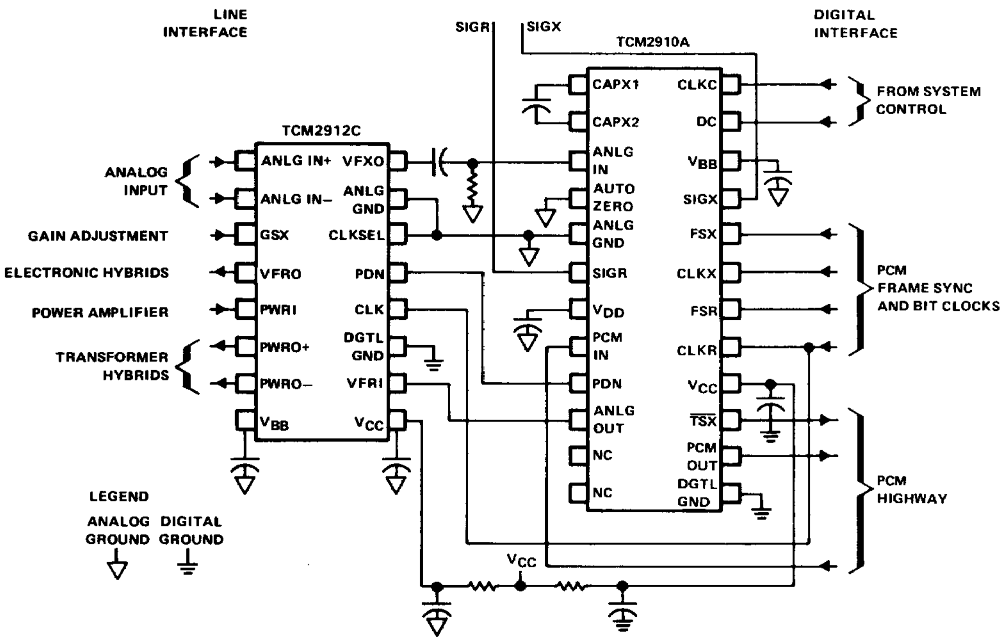

FIGURE 11. TCM2910A INTERFACE WITH TCM2912C FILTER

TABLE 3a. μ-LAW POSITIVE INPUT VALUES
Reproduced from CCITT† (Volume III — 2 on Line Transmission)
Recommendation G.711 on Pulse Code Modulation of Voice Frequencies

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note A)	Character signal (see Note B) Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (see Note C)	Decoder output value number
		8159	$(128)^D$	(8159)			
					1 0 0 0 0 0 0 0	8031	127
			127	7903			
8	16 × 256		⋮	⋮	(see Note E)	⋮	⋮
			113	4319			
					1 0 0 0 1 1 1 1	4191	112
		4063	112	4063			
7	16 × 128		⋮	⋮	(see Note E)	⋮	⋮
			97	2143			
					1 0 0 1 1 1 1 1	2079	96
		2015	96	2015			
6	16 × 64		⋮	⋮	(see Note E)	⋮	⋮
			81	1055			
					1 0 1 0 1 1 1 1	1023	80
		991	80	991			
5	16 × 32		⋮	⋮	(see Note E)	⋮	⋮
			65	511			
					1 0 1 1 1 1 1 1	495	64
		479	64	479			
4	16 × 16		⋮	⋮	(see Note E)	⋮	⋮
			49	239			
					1 1 0 0 1 1 1 1	231	48
		223	48	223			
3	16 × 8		⋮	⋮	(see Note E)	⋮	⋮
			33	103			
					1 1 0 1 1 1 1 1	99	32
		95	32	95			
2	16 × 4		⋮	⋮	(see Note E)	⋮	⋮
			17	35			
					1 1 1 0 1 1 1 1	33	16
		31	16	31			
	15 × 2		⋮	⋮	(see Note E)	⋮	⋮
			2	3			
1					1 1 1 1 1 1 1 0	2	1
			1	1			
↓	1 × 1				1 1 1 1 1 1 1 1		
			0	0		0	0

NOTES: A. 8159 normalized value units correspond to the value of the on-chip voltage reference.
B. The PCM word on the highways is the same as the one shown in column 6.
C. The voltage output on the ANLG OUT lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
D. X_{128} is a virtual decision value.
E. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.

†The International Telegraph and Telephone Consultative Committee. Published by the International Telecommunication Union, Geneva, Switzerland.

TABLE 3b. μ-LAW NEGATIVE INPUT VALUES
Reproduced from CCITT† (Volume III — 2 on Line Transmission) Recommendation G.711 on Pulse Code Modulation of Voice Frequencies

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note A)	Character signal (see Note B) Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (see Note C)	Decoder output value number
			0	0		0	0
	1 × 1				0 1 1 1 1 1 1 1		
			1	−1			
1					0 1 1 1 1 1 1 0	−2	1
			2	−3			
	15 × 2				(see Note D)		
		−31	16	−31			
					0 1 1 0 1 1 1 1	−33	16
			17	−35			
2	16 × 4				(see Note D)		
		−95	32	−95			
					0 1 0 1 1 1 1 1	−99	32
			33	−103			
3	16 × 8				(see Note D)		
		−223	48	−223			
					0 1 0 0 1 1 1 1	−231	48
			49	−239			
4	16 × 16				(see Note D)		
		−479	64	−479			
					0 0 1 1 1 1 1 1	−495	64
			65	−511			
5	16 × 32				(see Note D)		
		−991	80	−991			
					0 0 1 0 1 1 1 1	−1023	80
			81	−1055			
6	16 × 64				(see Note D)		
		−2015	96	−2015			
					0 0 0 1 1 1 1 1	−2079	96
			97	−2143			
7	16 × 128				(see Note D)		
		−4063	112	−4063			
					0 0 0 0 1 1 1 1	−4191	112
			113	−4319			
8	16 × 256				(see Note D)		
			126	−7647			
					0 0 0 0 0 0 0 1	−7775	126
			127	−7903			
					0 0 0 0 0 0 0 0	−8031	127
		−8159	(128)[E]	(−8159)			

NOTES:
- A. 8159 normalized value units correspond to the value of the on-chip voltage reference.
- B. The PCM word on the highways is the same as the one shown in column 6.
- C. The voltage output on the ANLG OUT lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
- D. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.
- E. X_{128} is a virtual decision value.

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