

TC541000P/F-15, TC541000P/F-20 TC541001P/F-15, TC541001P/F-20

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC541000P/F and TC541001P/F are a 131,072 word x 8 bit one time programmable read only memory and molded in a 32 pin plastic package.

The TC541000P/F and TC541001P/F's access time are 150ns/200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC571000D/TC571001D's. Once programmed, the TC541000P/F and TC541001P/F cannot be erased because of using plastic package without transparent window.

FEATURES

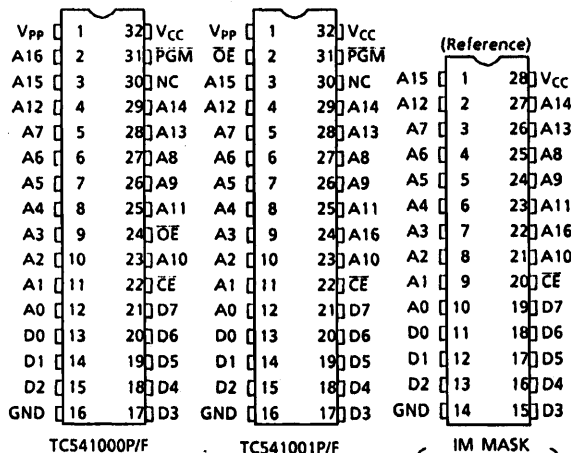
- Peripheral circuit : CMOS
- Single 5V power supply
- Memory cell : N-MOS
- Full static operation
- Access Time
- High speed programming operation : t_{pw} 0.1ms

	- 15	- 20
Temp	0~70°C	-40~85°C
t _{acc}	150ns	200ns

- Input and output TTL compatible
- JEDEC standard 32 pin : TC541000P/F
- 1M MROM compatible : TC541001P/F
- Standard 32 pin DIP plastic package: TC541000P/TC541001P
- S32Pin Plastic Flat Package : TC541000F/TC541001F

- Low power dissipation
- Active : 30mA/6.7MHz
- Standby : 100µA

PIN CONNECTION (TOP VIEW)

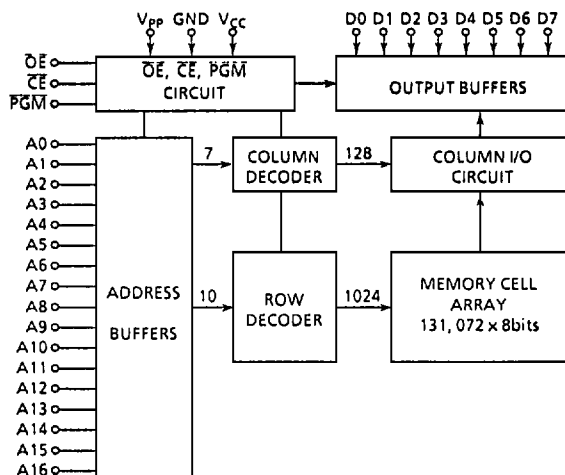


PIN NAMES

Pin Name	Function
A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

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BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	P _{GM}	C _E	O _E	V _{PP}	V _{CC}	D0~D7	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6~7.0	V
V _{PP}	Program Supply Voltage	-0.6~14.0	V
V _{IN}	Input Voltage	-0.6~7.0	V
V _{IO}	Input/Output Voltage	-0.6~V _{CC} +0.5	V
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature Time	260·10	°C·sec
T _{STRG}	Storage Temperature	-65~125	°C
T _{OPR}	Operating Temperature	-40~85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	$V_{CC} - 0.6V$	V_{CC}	$V_{CC} - 0.6$	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	-	-	± 10	μA
I_{CCO1}	Operating Current	$\bar{C}\bar{E} = 0V$ $f = 6.7\text{MHz}$	-	-	30	mA
I_{CCO2}		$I_{OUT} = 0\text{mA}$ $f = 1\text{MHz}$	-	-	10	mA
I_{CCS1}	Standby Current	$\bar{C}\bar{E} = V_{IH}$	-	-	1	mA
I_{CCS2}		$\bar{C}\bar{E} = V_{CC} - 0.2V$	-	-	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	-	-	~ 0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$	-	-	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	-	-	± 10	μA

$T_a = 0 \sim 70^\circ\text{C}$ for TC541000P/F/TC541001P/F - 15

A.C. CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TC541000P - 15 / TC541001P - 15		TC541000P - 20 / TC541001P - 20		UNIT
		TC541000F - 15 / TC541001F - 15		TC541000F - 20 / TC541001F - 20		
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\bar{C}\bar{E}$ to Output Valid	-	150	-	200	ns
t_{OE}	$\bar{O}\bar{E}$ to Output Valid	-	70	-	70	ns
t_{PGM}	$\bar{P}\bar{G}\bar{M}$ to Output Valid	-	70	-	70	ns
t_{DF1}	$\bar{C}\bar{E}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\bar{O}\bar{E}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	PGM to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	-	0	-	ns

$T_a = 0 \sim 70^\circ\text{C}$ for TC541000P/F/TC541001P/F - 15

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

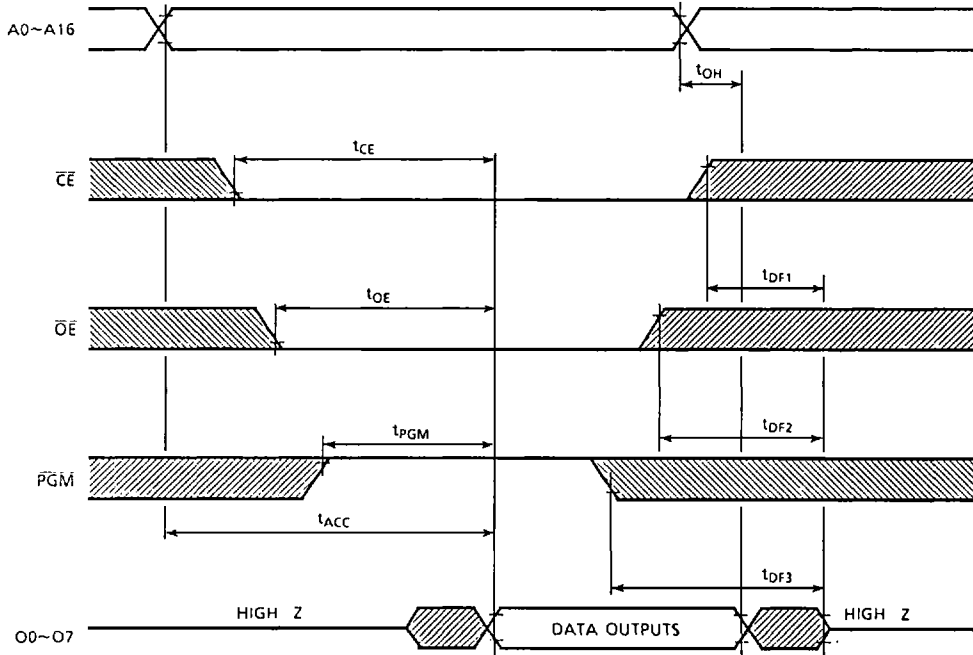
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CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	-	4	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	-	10	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



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HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.75 \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	-	-	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0\text{V}$	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25 \pm 0.25\text{V}$, $V_{PP} = 12.75 \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\bar{C}\bar{E}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\bar{C}\bar{E}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OL}	$\bar{O}\bar{E}$ to Output Valid	-	-	-	100	ns
$t_{DR?}$	$\bar{O}\bar{E}$ to Output in High-Z	$\bar{C}\bar{E} = V_{IL}$	-	-	90	ns

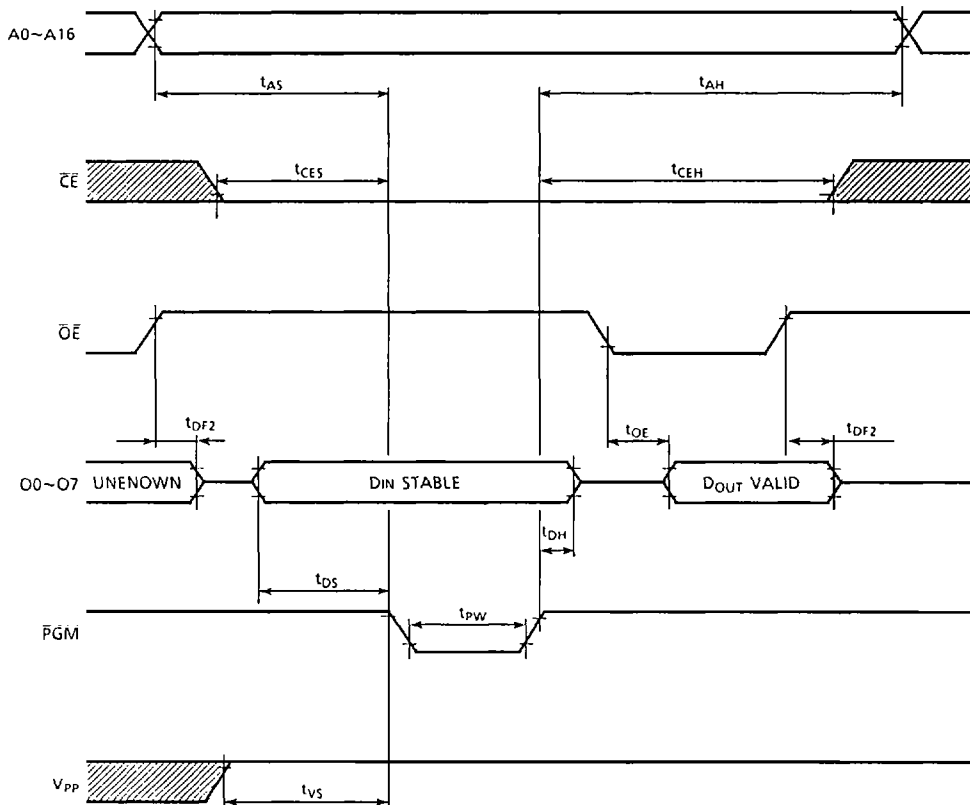
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

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HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note :
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=12.75V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC541000P/F/TC541001P/F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{\text{PGM}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{CC}	O0~O7	Power
READ OPERATION	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION ($T_a = 25 \pm 5^\circ\text{C}$)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note : H; V_{IH} , L; V_{IL} , *; V_{IH} or V_{IL}

READ MODE

The TC541000P/F/TC541001P/F has three control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable ($\overline{\text{OE}}$) and the program control ($\overline{\text{PGM}}$) control the output buffers independent of device selection.

Assuming in that $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$, and $\overline{\text{PGM}} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}} = V_{IL}$, $\overline{\text{PGM}} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

And assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$, and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{\text{PGM}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$, the outputs will be in a high impedance state.

So two or more ROMs can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

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STANDBY MODE

The TC541000P/F/TC541001P/F has a low power standby mode controlled by the \overline{CE} signal. By applying a high level to the \overline{CE} input, the TC541000P/F/TC541001P/F is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the \overline{OE} inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC541000P/F/TC541001P/F are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC541000P/F/TC541001P/F can be programmed any location at anytime - either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{II} , and \overline{PGM} at V_{III} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TC541000P/F/TC541001P/F from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{III}$.

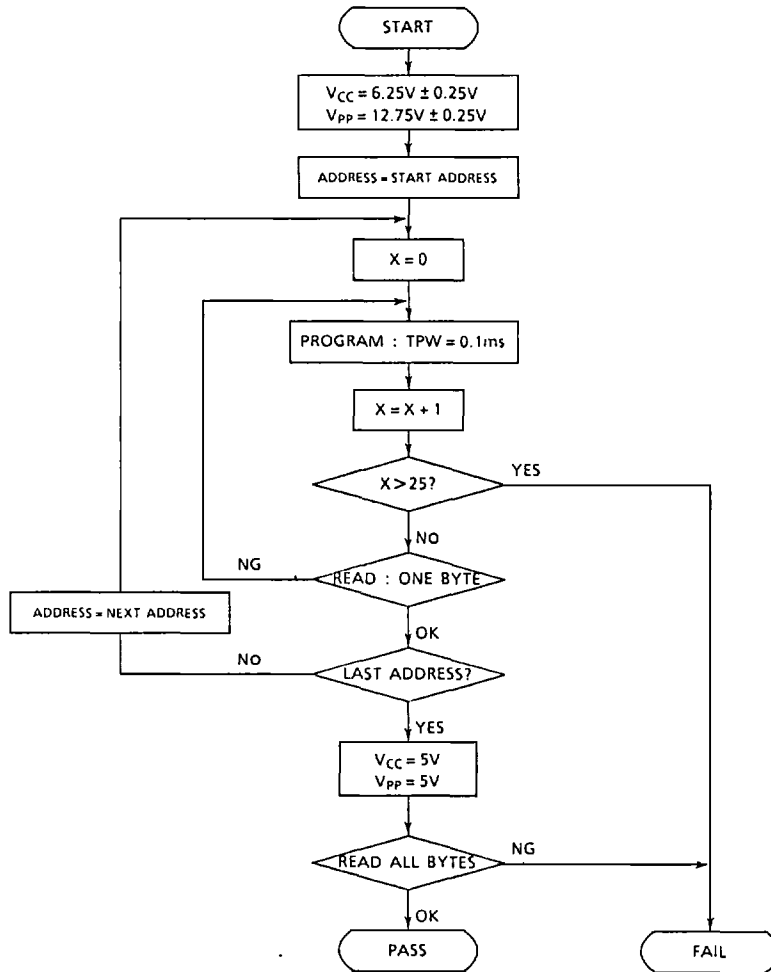
The programming is achieved by applying a single TTL low level 0.1ms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



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ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC541000P / F / TC541001P / F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC541000P / F / TC541001P / F by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC541000P / F / TC541001P / F.

SIGNATURE		PINS									HEX. DATA
		A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC541000P / F	V_{IH}	1	0	0	0	0	1	1	0	86
	TC541001P / F		0	0	0	0	0	1	1	1	07

Notes : A9 = 12V ± 0.5V

A1 ~ A8, A10 ~ A16, \overline{CE} , \overline{OE} = V_{IL}

\overline{PGM} = V_{IH}

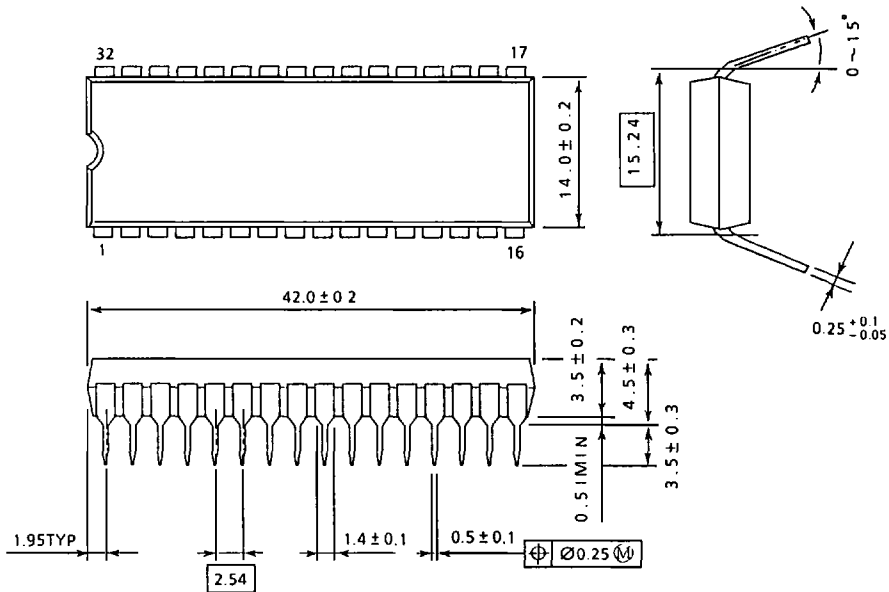
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OUTLINE DRAWINGS

• Plastic DIP

DIP32-P-600

Unit : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

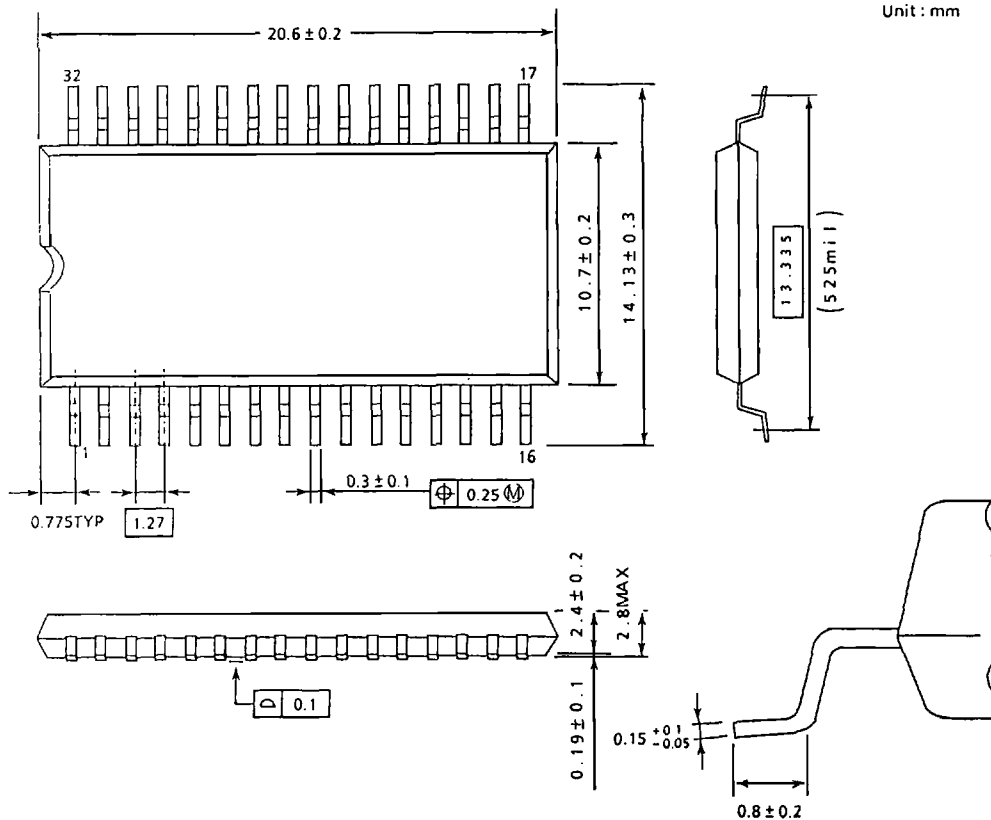
TC541000P/F-15, TC541000P/F-20 TC541001P/F-15, TC541001P/F-20

OUTLINE DRAWINGS

- Plastic SOP

SOP32-P-525

Unit: mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm