

LH53V2R00

Low-Voltage • High-Speed
2M-bit Mask-Programmable ROM

■ Description

The LH53V2R00N/T (User's No. : LH5V2RXX) is a CMOS 2M-bit mask-programmable ROM organized as 262 144 × 8 bits.

It provides a high-speed access time of 120 ns with low voltage operation (2.7 to 3.6 V).

■ Features

1. 262 144 × 8 bit organization
2. Maximum access time 120 ns
3. Maximum supply current

Operating	35 mA
Standby	30 μA
4. Static operation (Internal sync. system)
5. Three-state outputs
6. Supply voltage 2.7 to 3.6 V
7. Package

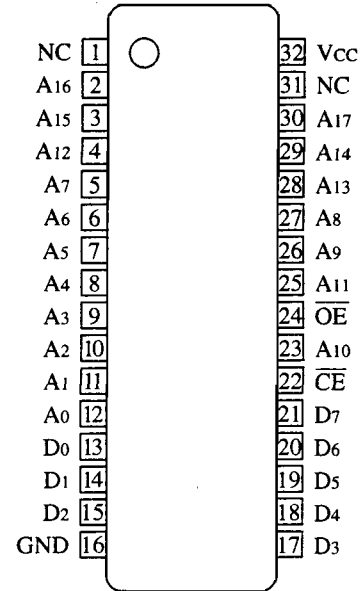
LH53V2R00N	32-pin SOP (SOP032-P-0525)
LH53V2R00T	32-pin TSOP (I) forward bend (TSOP032-P-0820)

■ Pin Description

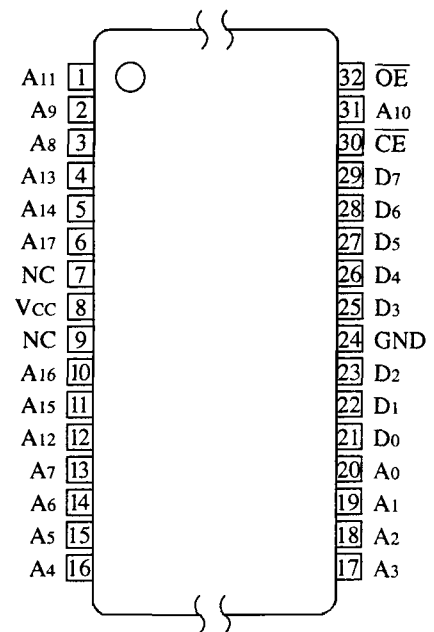
Signal	Pin name
A ₀ -A ₁₇	Address input
D ₀ -D ₇	Data output
\overline{CE}	Chip enable input
\overline{OE}	Output enable input
V _{CC}	Power supply
GND	Ground
NC	Non connection

■ Pin Connection

32-pin SOP

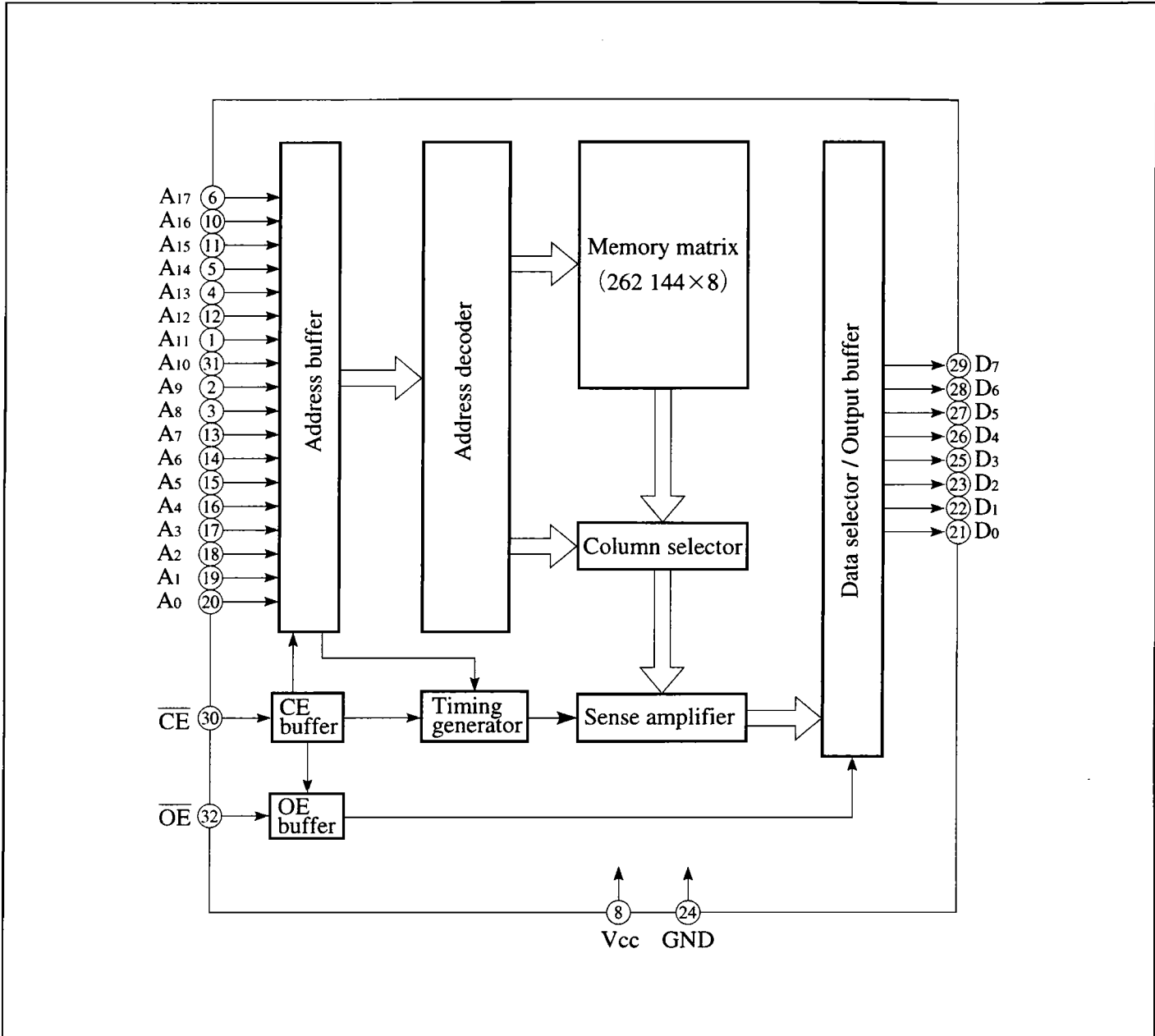


32-pin TSOP (I) forward bend



Top View

■ Block Diagram



■ Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	Data output	Supply current
High	X	High-impedance	Standby
Low	High	High-impedance	Operating
Low	Low	D ₀ -D ₇	Operating

X : Don't Care

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.3 to +4.6	V
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC} +0.3	V
Operating temperature	T _{opr}	-20 to +70	°C
Storage temperature	T _{stg}	-65 to +150	°C

■ Recommended Operating Conditions

(T_a = -20 to +70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}	2.7		3.6	V

DC Characteristics

(V_{CC}=2.7 to 3.6 V, T_a=-20 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V _{IH}		0.7V _{CC}		V _{CC} +0.3	V	
Input "Low" voltage	V _{IL}		-0.3		0.2V _{CC}	V	
Output "High" voltage	V _{OH}	I _{OH} =-100 μA	V _{CC} -0.4			V	
Output "Low" voltage	V _{OL}	I _{OL} =400 μA			0.4	V	
Input leakage current	I _{LI}	V _{IN} =0 V to V _{CC}			5	μA	
Output leakage current	I _{LO}	V _{OUT} =0 V to V _{CC}			5	μA	1
Supply current (Operating)	I _{CC1}	t _{RC} =120 ns			35	mA	2
	I _{CC2}	t _{RC} =1 μs			25	mA	
Supply current (Standby)	I _{SB1}	$\overline{CE}=V_{IH}$			1	mA	
	I _{SB2}	$\overline{CE}=V_{CC}-0.2 V$			30	μA	
Input capacitance	C _{IN}	f=1 MHz, T _a =25 °C			10	pF	
Output capacitance	C _{OUT}				10	pF	

Note 1. $\overline{CE}=V_{IH}$, $\overline{OE}=V_{IH}$ Note 2. V_{IN}=V_{IH}/V_{IL}, $\overline{CE}=V_{IL}$ (Output is open)

AC Characteristics

(V_{CC}=2.7 to 3.6 V, T_a=-20 to +70 °C)

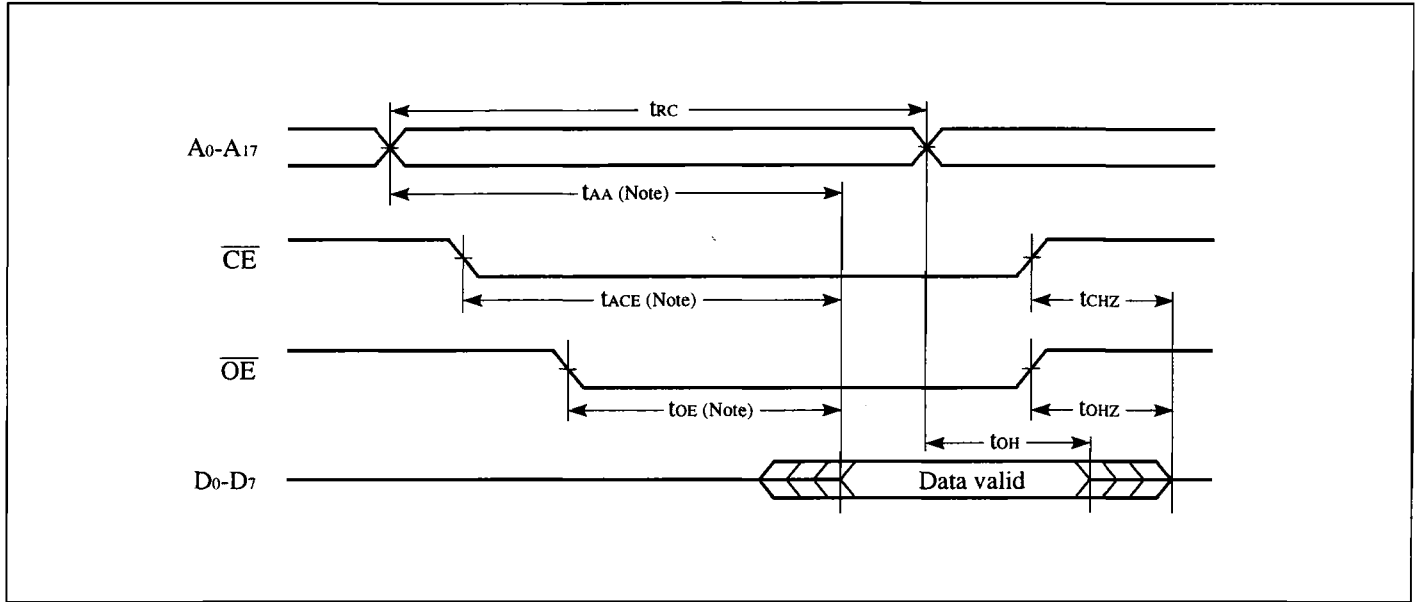
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Read cycle time	t _{RC}	120			ns	
Address access time	t _{AA}			120		
Chip enable access time	t _{ACE}			120		
Output enable delay time	t _{OE}			55		
Output hold time	t _{OH}	0				
Output floating time	t _{CHZ}			55		3
	t _{OHZ}			55		

Note 3. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC Test Conditions

- Input voltage amplitude : 0.2 V_{CC} to 0.7 V_{CC}
- Input signal rise / fall time : 10 ns
- Input / Output reference level : 1.4 V
- Output load condition : 1TTL + 100 pF

■ Timing Diagram



Note. The output data becomes valid when the last interval t_{AA} , t_{ACE} or t_{OE} have concluded.

Sharp's Product Line-up (2M-bit Mask ROM)

Configuration (Word × bits)	*1 Pinout	Model No.	User's No.	Access time (ns) MAX. Cycle time (ns) MAX.	Supply current (mA) MAX.	Supply voltage (V)	Package
256k × 8	J	LH532100BD/BN/BT/BS/BSR/BU-1	LH532KXX	120	50	5 ± 10%	32DIP/32SOP/32TSOP (I) forward bend/ 32TSOP (II) forward bend/ 32TSOP (II) reverse bend/32QFJ
256k × 8	J	LH53V2R00N/T	LH5V2RXX	120	35	2.7 to 3.6	32SOP/32TSOP (I) forward bend
256k × 8	J	LH532100BD/BN/BT/BS/BSR/BU	LH532KXX	150	50	5 ± 10%	32DIP/32SOP/32TSOP (I) forward bend/ 32TSOP (II) forward bend/ 32TSOP (II) reverse bend/32QFJ
128k × 16	J	LH532048D/N/U	LH532CXX	100	75	5 ± 10%	40DIP/40SOP/44QFJ
256k × 8 128k × 16	M	LH532600D/N/T/TR	LH5326XX	100	75	5 ± 10%	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend
256k × 8 128k × 16	M	LH53V2P00N/T	LH5V2PXX	120	35	2.7 to 3.6	40SOP/48TSOP (I) forward bend
256k × 8 128k × 16	M	LH532000BD/BN/BT/BTR-1	LH532GXX	120	50	5 ± 10%	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend
256k × 8 128k × 16	M	LH532000BD/BN/BT/BTR	LH532GXX	150	50	5 ± 10%	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend
256k × 8 128k × 16	M	LH532000BD/BN/BT/BTR-S	LH532SXX	500 (*3) 150 (*2)	15 (*4)	2.6 to 5.5	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend

*1 J : JEDEC standard EPROM pinout, M : Mask ROM specific pinout.

*2 $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$

*3 $2.6 \text{ V} \leq V_{CC} < 4.5 \text{ V}$

*4 $2.6 \text{ V} \leq V_{CC} \leq 3.4 \text{ V}$

MROM Flash Pin Compatible Flash MROM LH53V2R00 Low-Voltage High Speed 2M-bit