FEATURES

- 300-MHz MAXIMUM CLOCK FREQUENCY
- 28-BIT FREQUENCY RESOLUTION
- 8-BIT PARALLEL SINE OUTPUT
- ECL 100K OUTPUT LEVELS
- TTL INPUT LEVELS
- ECL 100K TECHNOLOGY
- CASCADABLE FOR ULTRA-HIGH FREQUENCY RESOLUTION
- 156 PIN CERAMIC PGA PACKAGE WITH INTEGRAL HEAT SINK MOUNTING STUDS

APPLICATIONS

- HIGH FREQUENCY SYNTHESIZERS
- HIGH-SPEED FREQUENCY HOPPED SOURCES
- DIGITAL SIGNAL PROCESSORS

CIRCUIT DESCRIPTION

The STEL-2172 Number Controlled Oscillator (NCO) generates a digital sine waveform of very precise frequency and can be used in conjunction with a D/A converter to provide high resolution frequency synthesis with virtually instantaneous frequency switching. The device is implemented in ECL technology and can operate at clock frequencies as high as 300 MHz. The frequency control inputs are TTL compatible to facilitate interface with conventional control circuits. The sine outputs are ECL-100K compatible to facilitate interfacing with available video DACs.

The NCO phase accumulator maintains a record of phase which is accurate to 28 bits of resolution. During each clock cycle, Δ-phase (the number stored in the 28-bit D-phase register) is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine function, and D-phase represents the change of phase at each cycle of the clock. This number is directly related to the output frequency by the following equation:

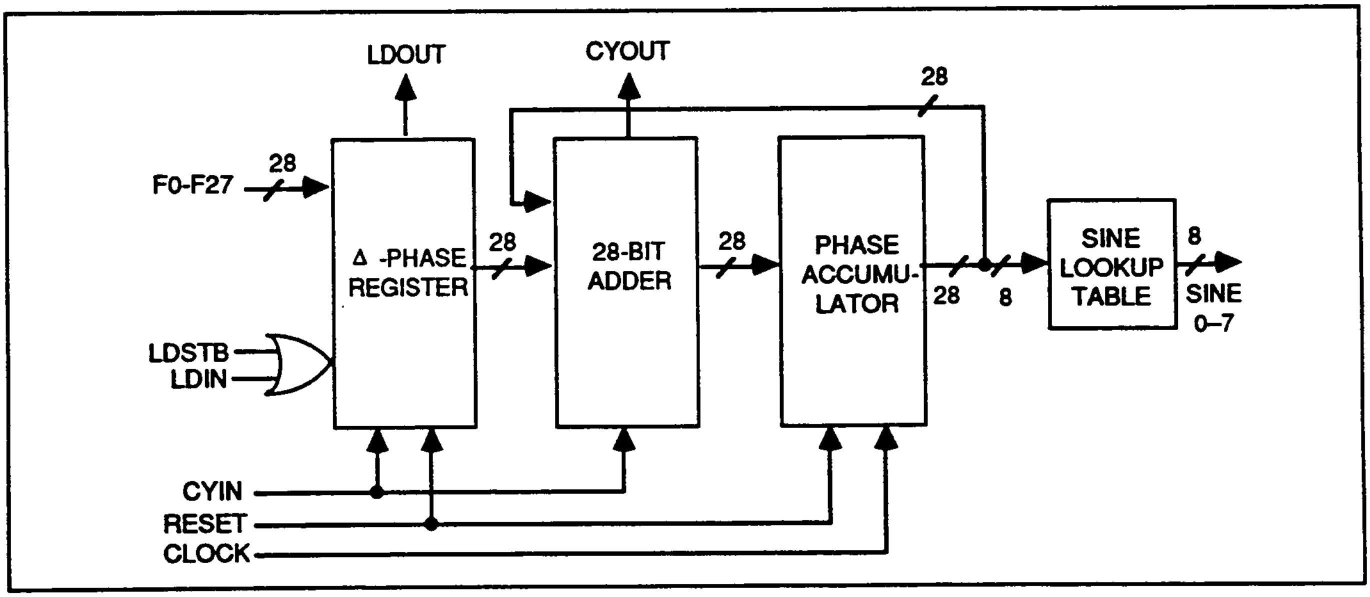
$$f_o = \frac{f_c \times \Delta\text{-phase}}{2^{28}}$$

where f_o = output frequency

f_c = clock frequency

and $0 \le \Delta\text{-phase} \le 2^{28} - 1$

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The sine function is generated from the eight most significant bits of the phase accumulator. The frequency of the ECL-NCO is determined by the number stored in the Δ-phase register which may be programmed by a microprocessor (with a few discrete logic circuits) or hardwired to full parallel control logic.

The output signal of the ECL-NCO is a sampled sine wave where the sampling function is the clock. If the output frequency is very low with respect to the clock, then the ECL-NCO output will sequence through each of the 256 states of the sine function. As the output frequency is increased with respect to the clock, the sine function appears more discontinuous. At the Nyquist limit, when the output frequency is exactly half the clock frequency, the output waveform is reduced to a square wave. The practical upper limit of the ECL-NCO output frequency is about 40% of the clock frequency. This is because spurious components at frequencies greater than half the clock frequency become difficult to remove by filtering (see Page 5).

The phase noise of the ECL-NCO output signal may be determined by knowing the phase noise of the clock signal input and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

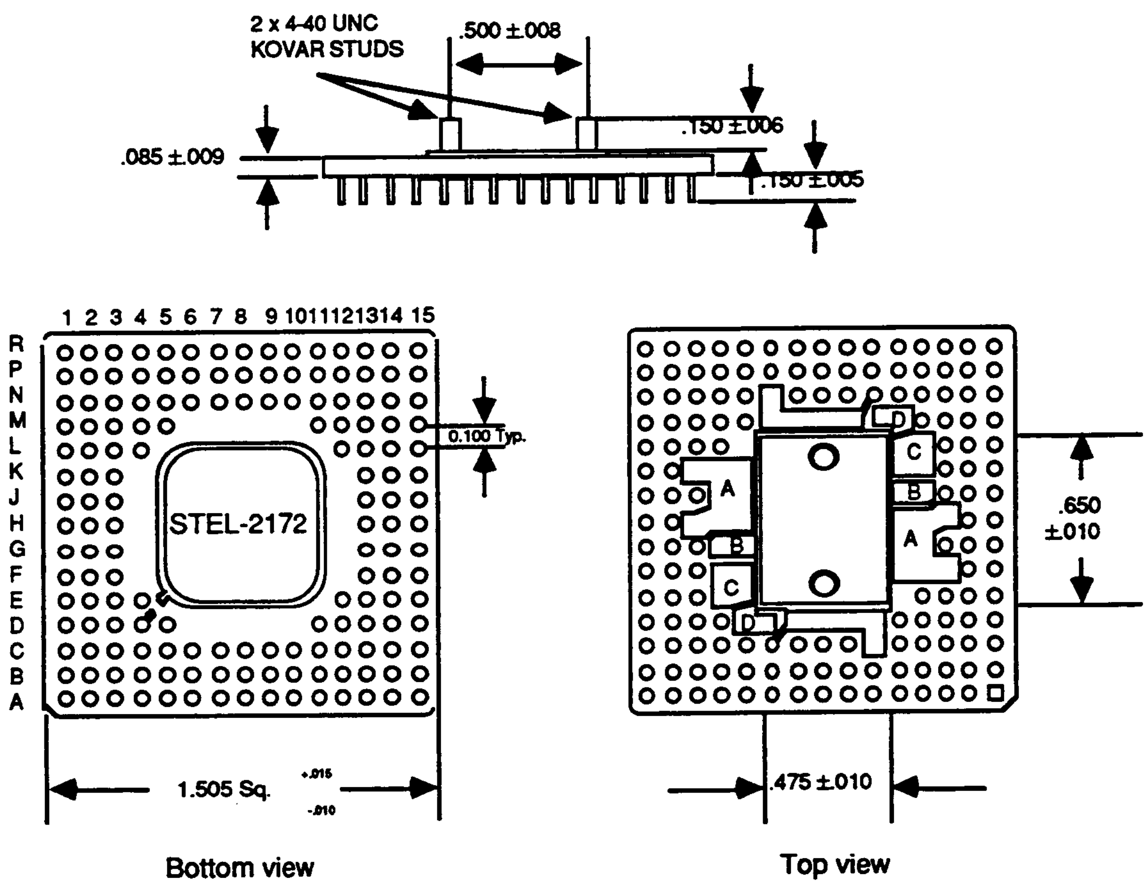
The ECL-NCO achieves its high operating frequency by making extensive use of pipelined architecture. The pipelining delay within the ECL-NCO takes 33 clock periods. This effectively limits the rate at which the NCO frequency can be changed. After new frequency data is entered, the load command is given, and the pipelining delay commences. After that time, the output frequency instantaneously switches maintaining phase coherence. After this, the next frequency may be entered. If a 300-MHz clock is used, the NCO could be continuously switched between programmed frequencies with a minimum average switching time of about 110 nanoseconds.

STEL-2172 PIN ASSIGNMENTS (See Page 4 for package information.)

PIN NAME	PIN #	PIN NAME	PIN #	PIN NAME	PIN #
F_0	R14	F_{14}	R7	LDSTB	R15
F_1	N12	F_{15}	P7	RESET	N11
F_2	R13	F_{16}	R6	CLOCK	P15
F_3	P13	F_{17}	P6	CYIN	N15
F_4	R12	F_{18}	R5	LDIN	M15
F_5	P12	F_{19}	P5	CYOUT	A14
F_6	R11	F_{20}	R4	LDOUT	A15
F_7	P11	F_{21}	P4	SIN_0	A1
F_8	R10	F_{22}	R3	SIN_1	A2
F_9	P10	F_{23}	P3	SIN_2	A3
F_{10}	R9	F_{24}	R2	SIN_3	A4
F_{11}	P9	F_{25}	N4	SIN_4	A5
F_{12}	R8	F_{26}	R1	SIN_5	A6
F_{13}	P8	F_{27}	N3	SIN_6	A7
				SIN_7	A8

POWER CONNECTIONS:
V_{EE}: F3, H3, H13, K13
V_{CC}: C6, C10, D4, D12, G3, G13, J3, M4, M12, N6, N10, J13
TTL_{GND}: C7, C8, C9, D5, D11, M5, M11, N7, N8, N9
V_{TTL}: E4, E12, L4, L12

PACKAGE DIMENSIONS



Bottom view

Top view

Notes:
1. All dimensions in inches.
2. Pads marked A are connected to V_{EE}
3. Pads marked B are connected to V_{CC}
4. Pads marked C are connected to V_{TTL}
5. Pads marked D are connected to TTL_{GND}
6. Maximum torque on heat sink mounting studs: 100 oz.-inches (7 Kgm-cm.)

POWER DECOUPLING

The 8 pads A through D (2 of each) on the top surface of the package are connected to the power supply pins and provide means to decouple the supply lines very close to the chip itself. It is recommended that 1000pF NPO chip capacitors be mounted directly on these pads to decouple V_{EE} to V_{CC} and V_{TTL} to TTL_{GND}; i.e, between both sets of pads A and B and between both sets of pads C and D (4 capacitors total).

INPUT SIGNALS

RESET
The **RESET** input is asynchronous with respect to the **CLOCK** input. When **RESET** goes to a logic high, all registers are cleared within 4 nanoseconds. After the **RESET** is returned to logic low, the **SIN** output corresponding to zero phase (81_H) will appear at the output 10 clock pulses later and remain there until a new frequency is loaded. The signal is TTL compatible.

CLOCK
All synchronous functions performed within the ECL-NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** input should nominally be a square wave with a maximum frequency of 300 MHz. The signal is ECL-100K compatible. A non-repetitive clock waveform is permissible as long as the minimum period between edges is always greater than 1.5 nanoseconds. On each rising edge of the **CLOCK** signal, the number stored in the D-phase register is added to the current contents of the phase accumulator.

F_0 through F_{27}
The 28-bit F_0 through F_{27} bus is used to program the 28-bit D-phase register. F_0 is the least significant bit of the bus. These inputs are TTL compatible and must be stable for at least 28 clock periods after the rising of the **LDSTB** input (See Page 7).

LDSTB
The **LDSTB** (Load Strobe) input is TTL compatible and is active on its rising edge. The minimum high pulse width is 1.5 nanoseconds. The rising edge of **LDSTB** starts the sequential loading of F_0 through F_{27}, one input at each clock pulse, starting with F_0. It takes 28 clock periods to load the 28 frequency input bits. The frequency of the NCO output will change 33 clock cycles after the rising edge of **LDSTB** due to the pipelining delays.

CYIN
In normal operation of the NCO, the **CYIN** (Carry In) input may be left open. This ECL-100K compatible input is internally connected to V_{EE} via a 50K ohm resistor . When **CYIN** is logic high, the effective value of the D-phase register is increased by one. If two ECL-NCO's are cascaded to obtain 56 bits of resolution, the **CYOUT** of the lower order ECL-NCO is connected to the **CYIN** of the higher order ECL-NCO.

LDIN
During normal operation of the ECL-NCO, the **LDIN** (Load In) input may be left open. This ECL-100K level input is internally connected to V_{EE} via a 50K ohm resistor. When two ECL-NCO's are cascaded, the **LDOUT** of the lower order ECL-NCO is connected to the **LDIN** of the higher order ECL-NCO. **LDIN** is logically ORed with **LDSTB** and, when not being used for cascading purposes, may be used in place of **LDSTB** if an ECL compatible input is required.

OUTPUT SIGNALS

SIN_0 through SIN_7
The output of the ECL-NCO is an 8-bit digitized sinewave and appears on the parallel **SIN_0-SIN_7** bus. This signal is derived from the 8 MSBs of the phase accumulator by means of a sine look-up table. The signal is in offset binary code, a value of 01_{hex} representing the most negative value, 80_{hex} representing a value of zero, and FF_{hex} representing the most positive value. Note that the output value 80_{hex} is never actually generated since the phase value of zero is not the start point of the sine wave stored in the ROM.

CYOUT
The **CYOUT** (Carry Out) signal represents the overflow bit of the phase accumulator. Each time the contents of the phase accumulator exceeds the maximum value that can be represented in a 28 bit field, the **CYOUT** (Carry Out) signal goes logic high for one clock cycle. If two ECL-NCO's are cascaded to obtain 58 bit frequency resolution, then the **CYOUT** of the lower order ECL-NCO must be connected to the **CYIN** of the higher order ECL-NCO. This effectively cascades the phase accumulators for true multiple precision.

LDOUT
Each time a new frequency is loaded, **LDSTB** initiates loading of each frequency bit into D-phase register starting with F_0. After the 28th bit is loaded, the **LDOUT** signal goes true for one clock cycle. If two ECL-NCO's are cascaded to obtain 56 bit frequency resolution, then the **LDOUT** of the lower order ECL-NCO must be connected to the **LDIN** of the higher order ECL-NCO, and the LDSTB input of this device must be held at a logic low level or left open. This ensures that the loading sequence of the new 56 bit number into the Δ-phase registers is correct allowing phase coherence to be maintained in this mode of operation.

SPECTRAL PURITY

In many applications, the ECL-NCO is used with a digital-to-analog converter to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including phase quantization, amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the D/A converter.

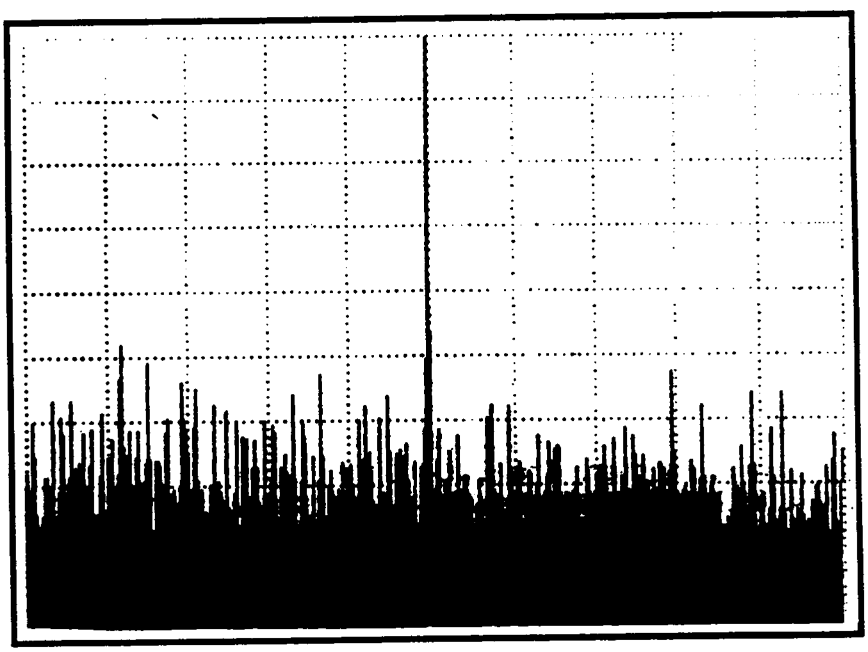
The sine function produced by the STEL-2172 has eight bit amplitude quantization and eight bit phase quantization which result in spurious levels which are theoretically about -48dBc (dB below the carrier, or primary component). The highest output frequency the ECL-NCO can generate is half the clock frequency ($f_c/2$), so spurious components which occur at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency of the ECL-NCO approaches $f_c/2$, an "image" spurious component also approaches $f_c/2$ from above. If the programmed output frequency is only slightly below $f_c/2$, it is virtually impossible to remove the "image" spurious component just above $f_c/2$ by filtering. For this reason, the maximum practical output frequency of the ECL-NCO should be limited to about 40% of the clock frequency.

Probably the most significant contribution to spectral purity is the dynamic performance of the D/A converter. To minimize these effects, connections between the D/A converter and ECL-NCO should be kept equal length using transmission line techniques. The analog output of the D/A converter should be isolated from the clock signal and other digital signals as much as possible. Grounding and decoupling should be done with the objective of optimizing the step response of the DAC.

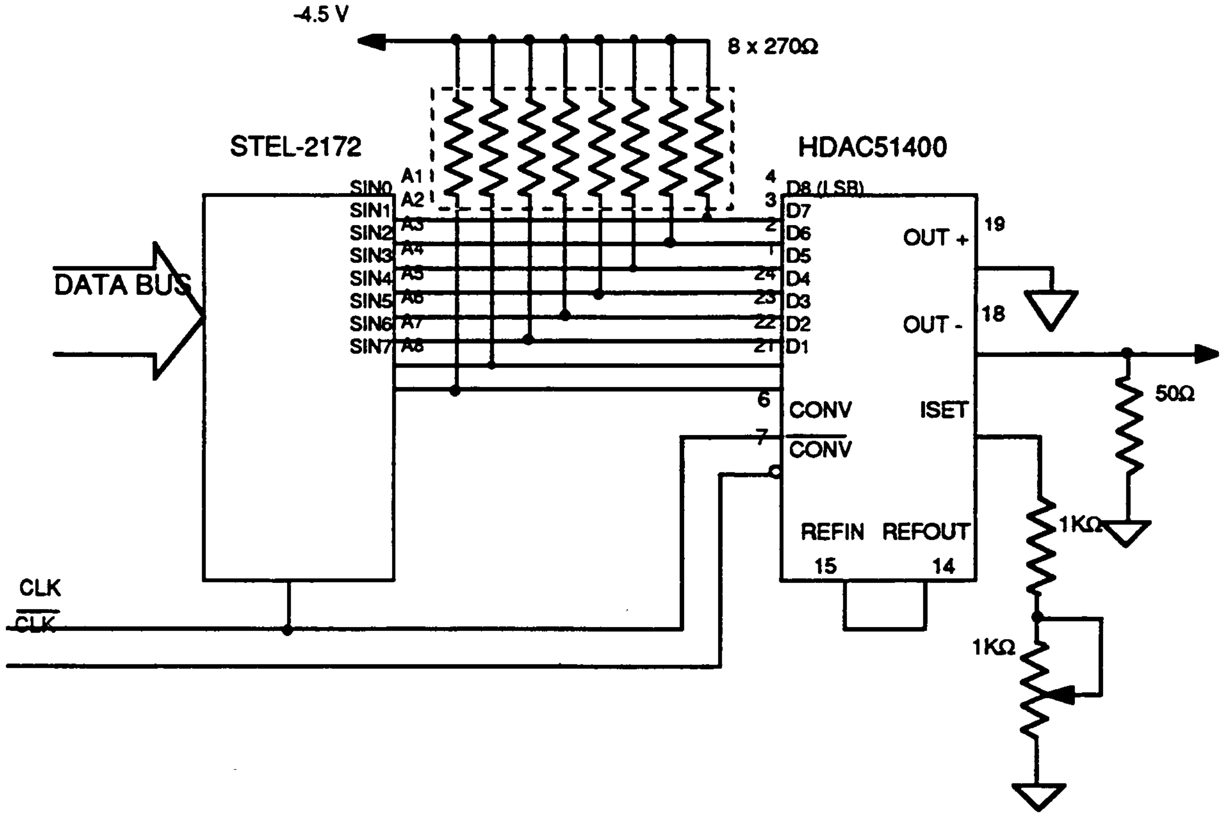
TYPICAL SPECTRUM OF STEL-2172 OUTPUT

TYPICAL SPECTRUM

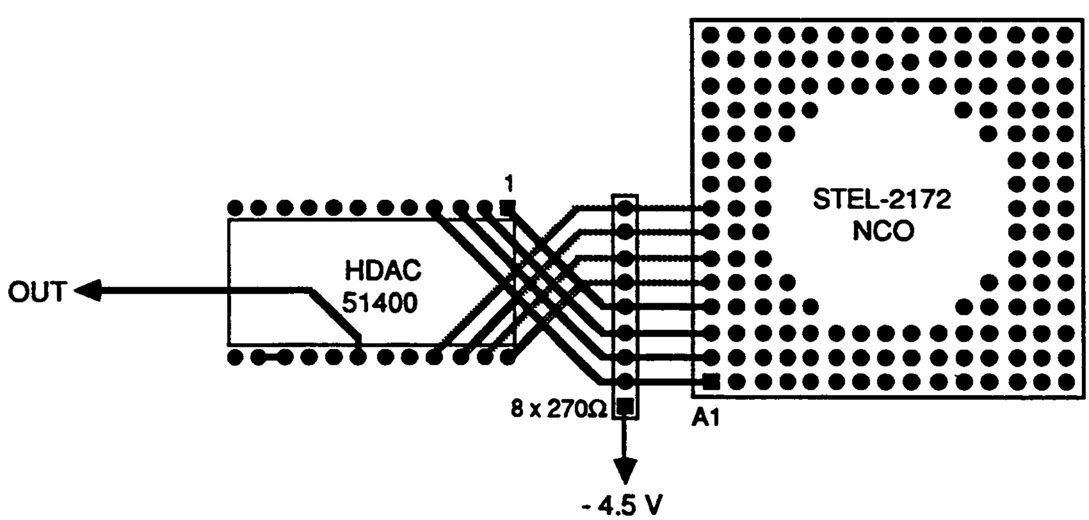
Center Frequency:	67.89 MHz
Frequency Span:	100 MHz
Reference Level:	+6 dBm
Resolution Bandwidth:	3 KHz
Scale:	Log, 10 dB/div
Output frequency:	67.89 MHz
Clock frequency:	300.0 MHz



INTERFACING THE STEL-2172 TO THE HDAC51400



Care must be taken when using the STEL-2172 with a Digital to Analog converter because of the high frequencies involved. Great care must be taken to ensure that the power supplies are properly decoupled, especially the -4.5 volt supply. The preferred practice is to use a 4 layer printed circuit board, using one layer as a ground plane and another as a -4.5 volt supply plane. In this way the transients in the ground plane can be minimized, and the analog output purity maximized. It is recommended that four 1000pF chip capacitors be connected between the supply lines and ground on the body of the ECL-NCO as shown on page 8. The pinout of the HDAC51400 requires that the SIN0-3 and SIN4-7 output lines from the STEL-2172 must cross over each other. In addition, it is recommended that 270Ω pullup resistors be connected from these lines to the -4.5 volt supply rail. A suggested layout for the connections is shown below.



D.C. CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Max. Junction Temperature	+150	°C
T_c	Case Temperature in Operation	-55 to +125	°C
V_{max}	Max. Voltage between V_{EE} and V_{CC}	-7.0 to +0.5	Volts
V_{in}	Input Voltage (D.C.)	V_{EE} to (V_{CC}+0.5)	Volts
I_{out}	Output Current at Vo=V_{OH}	-50	mA
V_{EE}	ECL Operating Range	-5.7 to -4.2	Volts
V_{TTL}	TTL Interface Operating Range	+4.5 to +5.5	Volts

D.C. CHARACTERISTICS

Operating Conditions: V_{EE} = -4.5 V, V_{CC} = GND, V_{TTL} = +5.0 V, TTL_{GND} = GND, T_{case} = -10 to +85 °C

(a) ECL CHARACTERISTICS

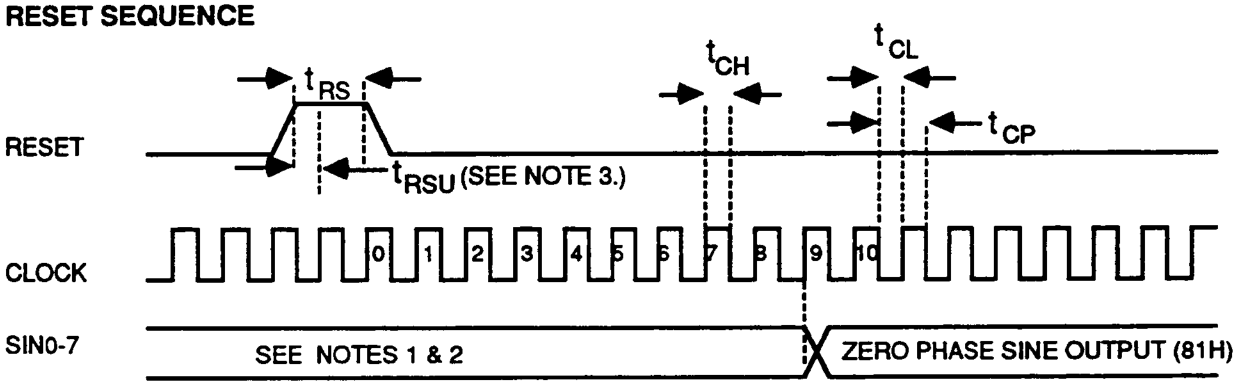
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Voltage	-1125		-880	mV	
V_{IL}	Input LOW Voltage	-1810		-1520	mV	
V_{OH}	Output HIGH Voltage	-1025	-955	-880	mV	Loaded with
V_{OL}	Output LOW Voltage	-1810	-1705	-1620	mV	50Ω to -2 V
I_{EE}	V_{EE} Supply Current		1.45		A	

(b) TTL INTERFACE CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Voltage	2.0			Volts	
V_{IL}	Input LOW Voltage			0.8	Volts	
I_{IH}	Input HIGH Current			40	µA	V_{CC}=Max, V_{IN}=2.4 V
I_{IL}	Input LOW Current			-400	µA	V_{CC}=Max, V_{IN}=0.4 V
I_{TTL}	VTTL Supply Current		100		mA	

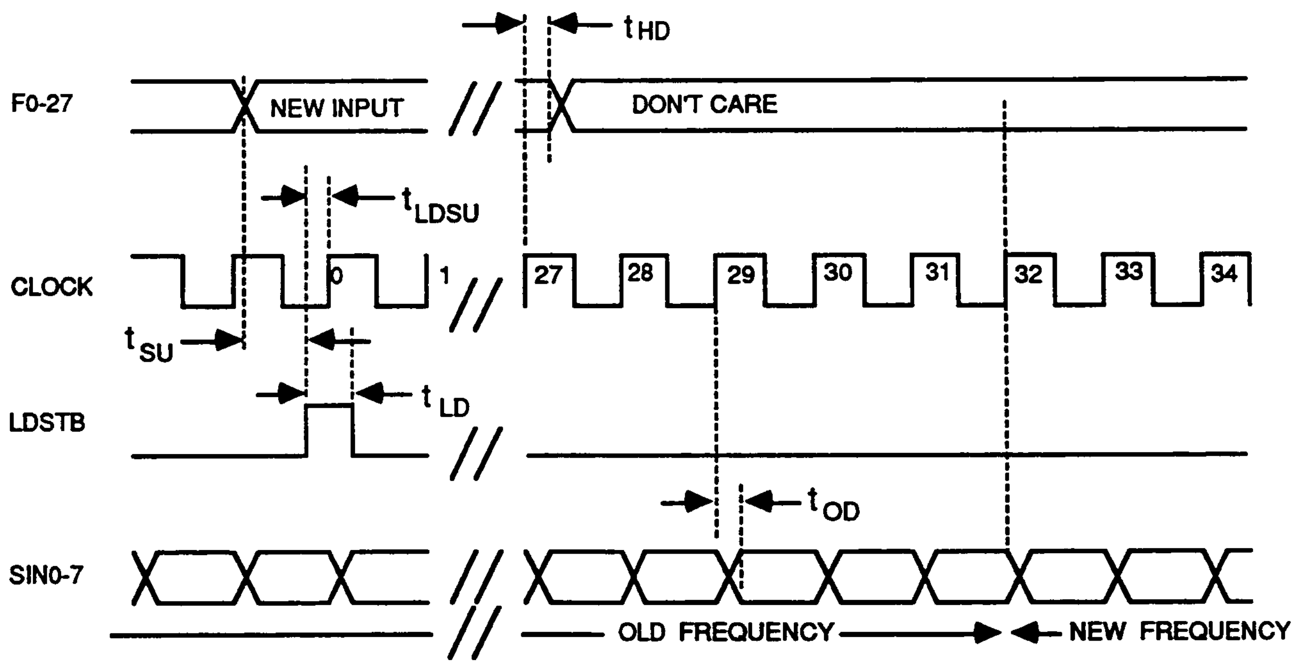
A.C. CHARACTERISTICS

RESET SEQUENCE



NOTES:
1. DATA IS INVALID DURING INITIAL RESET.
2. IF RESET OCCURS DURING NCO OPERATION, THE OUTPUT REMAINS AT THE FREQUENCY PREVIOUSLY SET FOR A PERIOD OF 10 CLOCK CYCLE THE PHASE THEN STAYS AT ZERO UNTIL A NEW FREQUENCY IS SET.
3. RESET IS ASYNCHRONOUS WITH RESPECT TO THE CLOCK.

FREQUENCY CHANGE

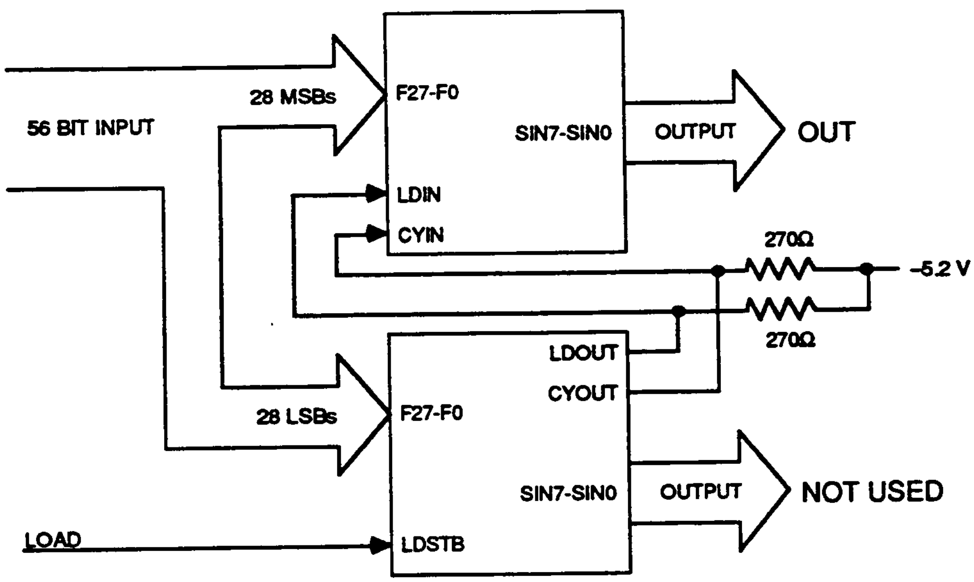


A.C. CHARACTERISTICS

TEST CONDITIONS: V_{EE} =–4.2 to –4.8 V. V_{CC} = TTL $_{GND}$ = 0 V.
V_{TTL} =4.75 to 5.25 V. Case Temp. = –55° to +125° C

Parameter	Symbol	Min.	Max.	Units
RESET duration	t_{RS}	1.5		nsec.
CLOCK high duration	t_{CH}	1.5		nsec.
CLOCK low duration	t_{CL}	1.5		nsec.
LDSTB duration	t_{LD}	1.5		nsec.
FREQUENCY setup	t_{SU}	0	nsec.	
FREQUENCY hold	t_{HD}	1.5		nsec.
OUTPUT delay	t_{OD}	1.9	3.8	nsec.
CLOCK period	t_{CP}	4.0		nsec.
LDSTB setup	t_{LDSU}	3.0	t_{CP}+1	nsec.
RESET setup	t_{RSU}	2.5	t_{CP}+0.5	nsec.
Max. CLOCK frequency	f_C	250	300	MHz

CASCADING STEL-2172s FOR HIGHER FREQUENCY RESOLUTION

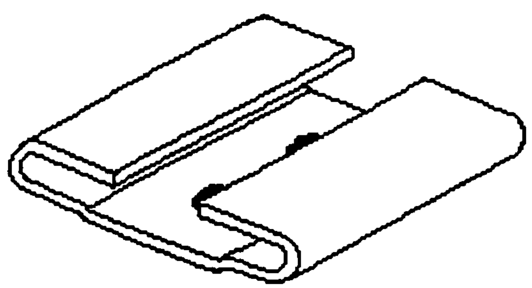


Two or more devices can be cascaded to increase the frequency resolution as shown in the diagram above. Only the LDSTB input of the lower order device is connected to the LOAD control line; the higher order device is automatically loaded at the right instant by connecting the higher order LDIN to the lower order LDOUT. Note that the F0-F27 lines must now be held stable for at least 56 clock cycles after the rising edge of the LOAD pulse. If this is a problem, the two devices may be loaded simultaneously by connecting both LDSTB inputs to the LOAD line, at the expense of sacrificing phase continuity whenever the frequency is changed. Because of the delay incurred in carrying the phase accumulator overflow signal (CYOUT) from the lower order device to the phase accumulator of the higher order device, the system will not operate at the rated maximum clock frequency of the STEL-2172 chip. The device has not yet been characterized in this mode.

HEAT SINKING

Since the STEL-2172 dissipates approximately 7 watts, it is essential that it be fitted with a suitable heat sink whenever the power is on. Detailed specifications of the heat sink will depend on the operating environment, and the main consideration is to keep the junction temperature below 150° C at all times. The temperature coefficient of the chip itself to the heat sink mounting pad on the package (q_{jc}) is approximately 2.0° C/watt which means that the package temperature must be kept below 135° C. A suitable heat sink for room temperature operation in free air conditions and higher temperatures with forced air cooling is shown below. This heat sink, part # 27004941, has a thermal resistance of approximately 15°/W in free air, falling to approximately 4°/W with 1000 ft/min. of airflow. It is available from:

O'Neal International
126 Yolo St.
Corte Madera,
CA 94925
(415) 924-1691



Approximate dimensions: 1.4" x 1.4" x 0.3"
Material: Black anodized aluminum, thickness 0.07"
Mounting holes: 0.125" dia. countersunk to 0.160" on underneath. Separation: 0.5"

Great care must be exercised when tightening the nuts on the Kovar studs since the studs will shear off very easily. The maximum torque used should be less than 50 oz-ins.

SOCKETS

Sockets for the STEL-2172 are available from a number of sources, some of which are listed below, with part numbers where known:

Advanced Interconnections Inc.
5 Energy Way,
W. Warwick, RI 02893
(401) 823-5200
Part # CS156-01TG
(for solder tail, others also available)

Augat Interconnection Components Inc.
33 Perry Ave.
Attleboro, MA 02703
(617) 222-2202
Part # PPS176-1A1513L
(for solder tail, others also available)

Aries Electronics Inc.
PO Box 130, 62A Trenton Ave.
Frenchtown, NJ 08825
(201) 996-6841

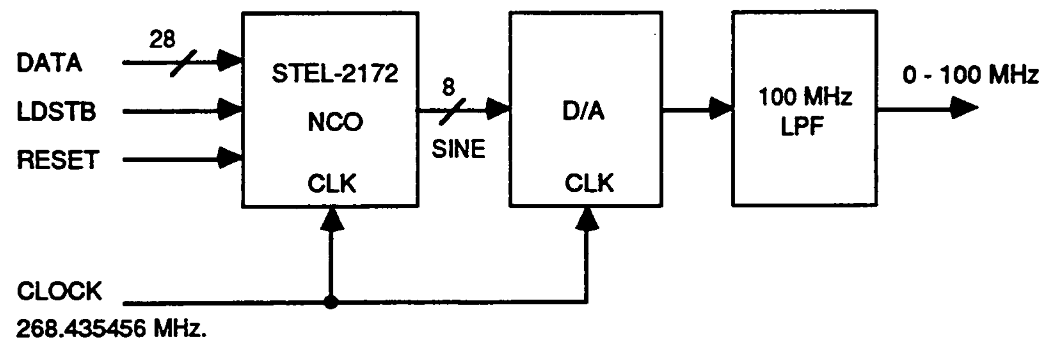
Elco Corp.
Huntingdon Ind. Park,
Huntingdon, PA 16652
(814) 643-0700
Part # 00-9085-06-000-0026

Note that PGA sockets are invariably made to order, due to the profusion of types available. Lead times of 4-10 weeks are common.

HEAT SINK AND SOCKET KIT

A kit consisting of a heat sink and socket is available from Stanford Telecommunications, Inc. for the convenience of the user of the STEL-2172 during prototyping. The part number of this kit is STEL-2172HSS.

TYPICAL APPLICATION:
A FAST SWITCHING DC TO 100 MHz SYNTHESIZER
WITH 1 Hz STEPS



If the output of the ECL-NCO is fed into a high-speed D-to-A converter, such as the Honeywell HDAC51400, a phase coherent, fast switching frequency synthesizer may be realized. The spurious components at the output of the low-pass filter will be 45-50 dB below the primary ouput component. If the clock frequency is set to 268.435456 MHz (2^{28} Hz), the frequency steps obtainable will be exactly 1 Hz.

The output frequency may be programmed from DC to over 100 MHz, the limit depending on the sharpness of the low-pass filter. In order to keep the spurious components at a level compatible with the other spurious components, the low-pass filter will need to have at least 45-50 dB of attenuation above f_c- f_o, where f_c is the clock frequency and f_o is the highest output frequency desired.

FOR FURTHER INFORMATION
CALL OR WRITE
STANFORD TELECOMMUNICATIONS
ASIC & Custom Products Division
Tel: (408) 980-5684 Fax: (408) 727-1482
2421 Mission College Blvd. • Santa Clara, CA 95056-0968