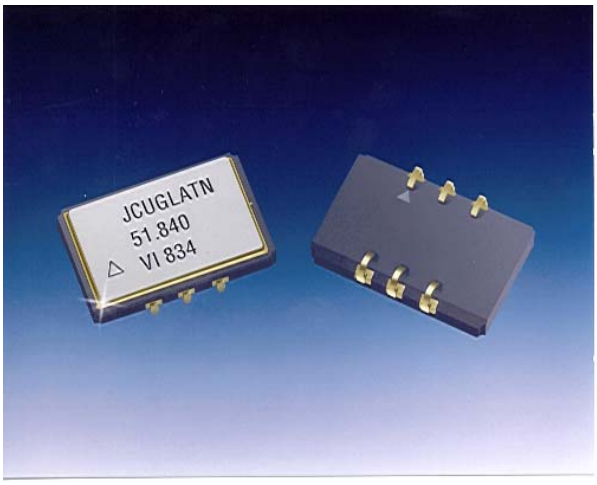
J-Type

Voltage Controlled Crystal Oscillator

Product is compliant to RoHS directive
and fully compatible with lead free assembly



The J-type Voltage Controlled Crystal Oscillator

Features

- Output Frequencies from 1.024 MHz to 170.000 MHz
- +3.3 or +5.0 volt options
- Small 14mm x 9mm J-type Package
- CMOS or PECL Outputs
- Low phase noise and custom options
- 0/70° C or –40/85° C operating temperature
- Tri-State output (CMOS) Enable/Disable (PECL)

Applications

- Clock Smoothing
- Frequency Translation
- SONET, SDH, ATM, DSLAM, ADM

Description

The J-type voltage controlled crystal oscillator expands VI's advanced VCXO performance capabilities while adhering to a package footprint compatible with the industry-common J-lead package.

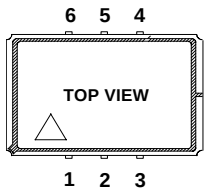
The J-type VCXO is a quartz stabilized square wave generator with either a CMOS output for driving CMOS/TTL loads or a PECL output. The device is packaged in a 6 pin J-lead ceramic package and is hermetically sealed with a grounded conductive lid.

The first section of this data sheet covers the performance/packaging/tape and reel/ordering information for the CMOS version and then the information for the PECL option follows.

Table of Contents

Table 1. Pin Out Information for the CMOS output Option

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	Tri-State[1]	TTL logic low disables output. TTL logic high, or no connect, enables output.
3	GND	Case and Electrical Ground
4	Output	VCXO Output
5	CMOS/TTL select[1,2]	TTL logic low optimizes symmetry for CMOS. TTL logic high, or NC, optimizes symmetry for TTL
6	V_{CC}	Power Supply Voltage (5.0 V or 3.3 V ±10%)



1. Standard option. Tri-State can be connected to pin 5 and CMOS/TTL select would be on pin 2.
2. Output is HCMOS. For frequencies >12MHz, this option optimizes symmetry for either CMOS or TTL thresholds. Ground this pin for frequencies < 12MHz.

Table 2. Electrical Performance @ 25°C for the CMOS output option

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage [1], +5 volt option +3.3 volt option		4.5 3.0	5.0 3.3	5.5 3.6	V V
Supply Current		10mA + 0.25mA per MHz, typical			
Center Frequency, *see ordering information*	F_N	1.024		77.760	MHz
Operating Temperature, *see ordering info*	T_{OP}	0/70, -40/85			°C
Absolute Pull Range over the operating temperature range, aging and power supply Vc= 0.5 to 4.5 or 0.3 to 3.0 V *see ordering information for options*	APR	±50 to ±100			ppm
Gain Transfer (Frequency vs. Control Voltage)	K_V	Positive			
Output Level High[2]	V_{OH}	0.8*Vcc	-		V
Output Level Low[2]	V_{OL}		-	0.1*Vcc	V
Output Rise/Fall Time[2]	$t_{R/}\ t_F$			5	ns
Duty Cycle[3], *see ordering info*	SYM	45/55 or 40/60			%
Input Leakage	I_L			±1	uA
Control Voltage Modulation Bandwidth	BW	-	10	-	kHz
RMS Jitter, 77.760MHz			3		ps
RMS Jitter, 77.760MHz, 12kHz to 20MHz			<0.5		ps
Maximum Control Voltage		0		V_{DD}	
Maximum Supply Voltage				7	V
Storage Temperature	T_S	-55	-	125	°C
Soldering Temp./Time	T_{LS}	-	-	240/10	°C/s

1. Power supply bypass is required and a 0.1uF in parallel with a 0.01uF high frequency capacitor is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the load used to test devices.
3. Duty cycle is defined as on-time versus period at 1.4 V for TTL, and 2.5 V for CMOS (5volt supply) and at 1.65 V for CMOS (3.3 volt operation)

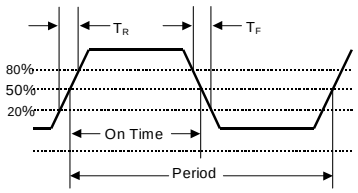


Figure 1. Output Waveform

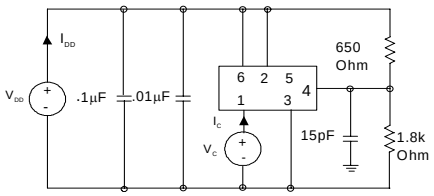


Figure 2. Output Test Conditions (25±5°C) for 5 volt devices, 15pF cap only for 3.3V.

Qualification Conformance

The CMOS J-type family has undergone the following Mil-Std qualification:

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015

Handling Precautions

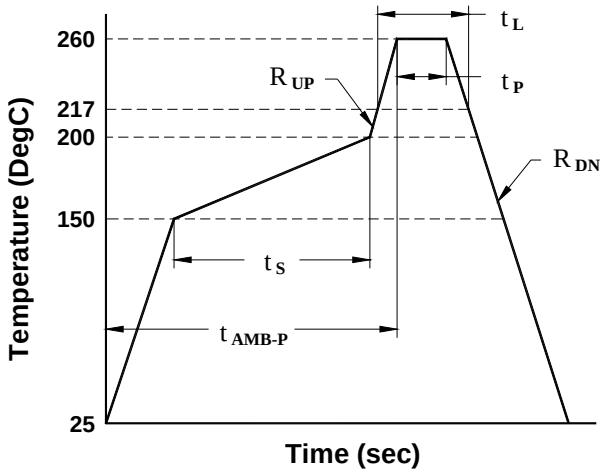
Although ESD protection circuitry has been designed into the the J-type, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5Kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

Table 4. ESD Ratings

Model	Minimum
Human Body Model (HBM)	1500 V
Charged Device Model (CDM)	1500 V

Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max



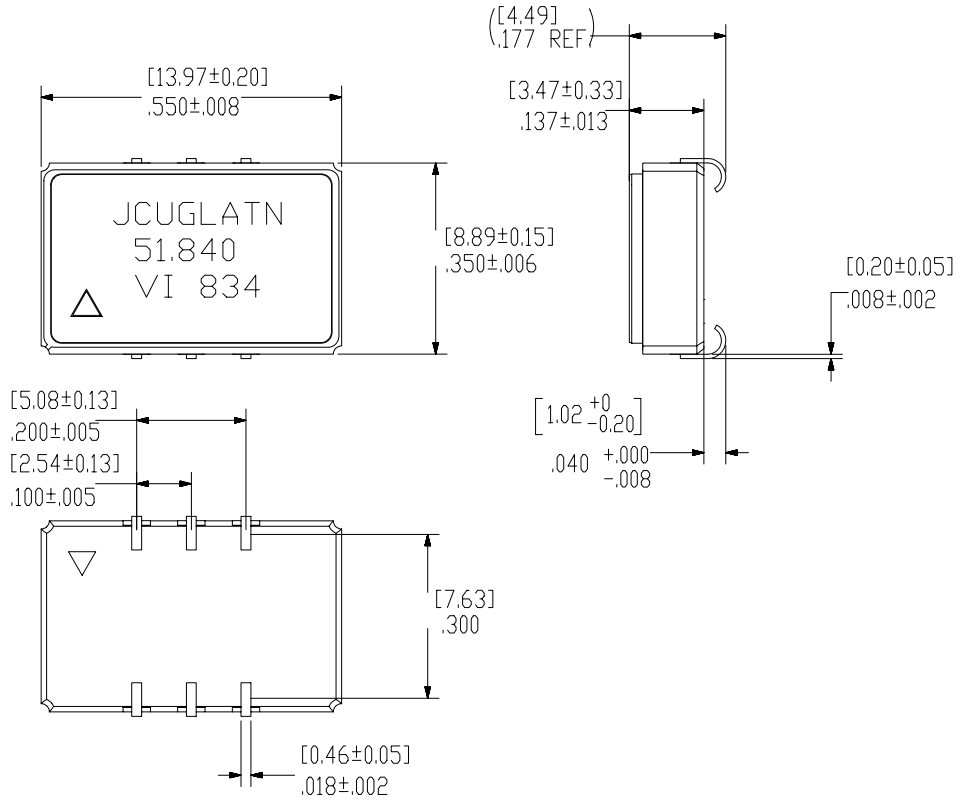


Figure 4. Outline Diagram

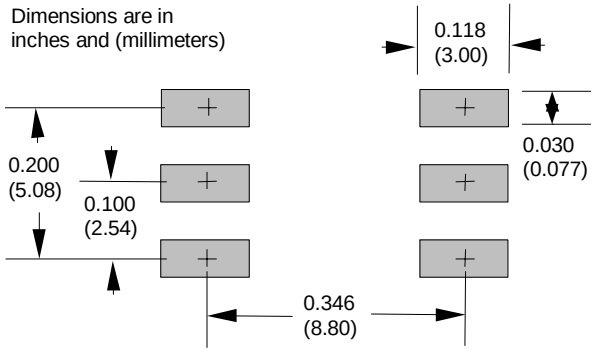


Figure 5. Suggested Pad Layout

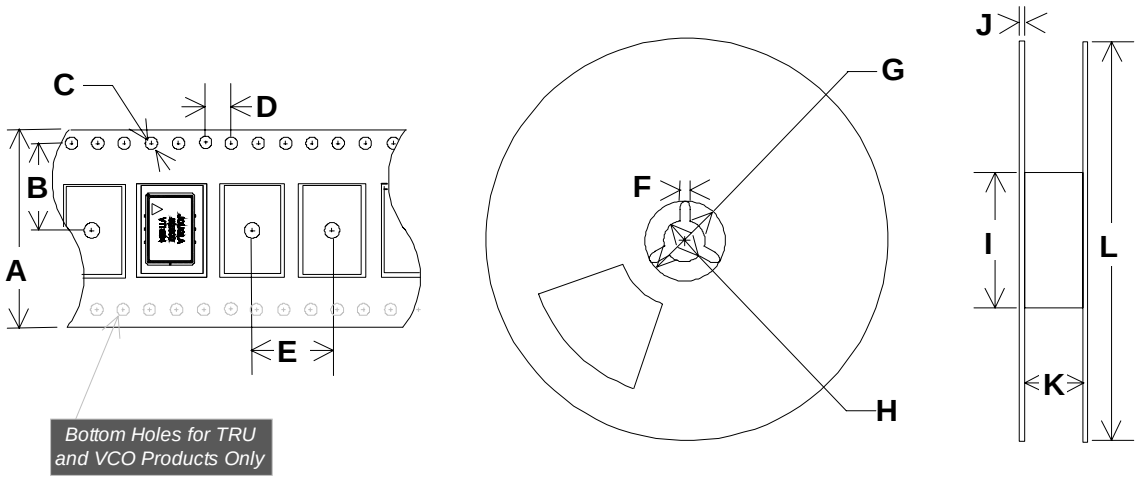


Figure 6. Tape Reel Drawing for CMOS and PECL output option

Table 5. Tape and Reel Dimensions (mm)

Tape Dimensions						Reel Dimensions							# Per
Product	A	B	C	D	E	F	G	H	I	J	K	L	Reel
J-Type	24	11.5	1.5	4	12	1.78	21	13	100	5	25	330	200

Table 6. Ordering Information for the CMOS output version (add frequency)

Package		Supply Voltage (V)		VCXO Type		APR (ppm)		Operating Temp. (°C)		Output/ Duty Cycle Min/Max		Tri-State		Specials	
J	6 pin Ceramic SOJ	**C**	5V±10%	**U**	VCXO	**G**	±50	**C**	0/70	**A**	TTL/ CMOS 45/55%[1]	**T**	Tri State on pin 2	**N**	Standard
		D	3.3±10%	**L**	±10% linear VCXO	**N**	±80	**L**	-40/ 85	**J**	CMOS 45/55%[2]				
						H	±100			**K**	CMOS 40/60%[3]				

1. Output is CMOS and symmetry is tested at TTL and CMOS thresholds.
2. Output is CMOS and symmetry is tested at CMOS threshold. This option is used for 3.3 V operation.
3. Output is CMOS and symmetry is tested at CMOS thresholds. This option is required for 3.3V, frequencies >51.840MHz.
4. Note: Not all combinations are possible.

Example: JDUGCKTN 77.76 = 3.3 volt, VCXO@77.760, ±50 ppm APR, 0/70°C, 40/60% Symmetry, CMOS, Tri-State on pin 2.

Table 7. Standard Frequencies, in MHz, for CMOS output option

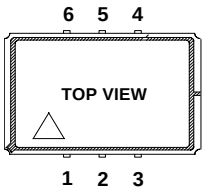
1.024	1.544	2.000	2.048	3.088	3.580
3.686	4.000	4.032	4.096	4.434	5.000
6.144	6.176	6.312	6.400	8.000	8.192
8.448	10.000	12.000	12.288	12.352	13.000
14.318	15.360	15.440	16.000	16.384	18.432
19.440	20.000	20.480	24.000	24.576	24.704
27.000	30.000	32.000	32.768	34.368	35.328
38.880	40.000	40.960	44.736	50.000	51.840
52.000	62.208	65.536	77.760	155.520[1]	

1. Uses a PLL multiplier, jitter is 25ps rms typical vs 3ps typical for a HFF design

Other frequencies available upon request.

Table 8. Pin Out Information for the PECL output option

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	N/C or E/D[2]	No Connect or Output Disable
3	GND	Case and Electrical Ground
4	Output	VCXO Output
5	COutput	VCXO Complementary Output
6	V_{CC}	Power Supply Voltage (5.0 V or 3.3 V ±10%)



. By setting OD high, the outputs are disabled and OUT is held low while Complementary OUT is held high. Output is enabled if E/D < VCC-1.6V,

2. See ordering information for enable/disable option.

Table 9. Electrical Performance @ 25°C for the PECL output option

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage [1], +5 volt option +3.3 volt option		4.5 3.0	5.0 3.3	5.5 3.6	V V
Supply Current		frequency dependent			
Center Frequency, *see ordering information*	F_N	15		170	MHz
Operating Temperature, *see ordering info*	T_{OP}	0/70, -40/85			°C
Absolute Pull Range over the operating temperature range, aging and power supply. Vc= 0.5 to 4.5 or 0.3 to 3.0 *see ordering information for options*	APR	±32, ±50			ppm
Gain Transfer (Frequency vs. Control Voltage)	K_V	Positive			
Output Level High[2]	V_{OH}	Vcc-1.025	-	Vcc-0.880	V
Output Level Low[2]	V_{OL}	Vcc-1.810	-	Vcc-1.620	V
	Output Logic Levels for -40 to 85°C Operation				
Output Level High[2]	V_{OH}	Vcc-1.085		Vcc-0.880	V
Output Level Low[2]	V_{OL}	Vcc-1.830		Vcc-1.555	V
Output Rise and Fall Time[2]	t_R/t_f			1	ns
Duty Cycle[3], *see ordering info*	SYM			45/55	%
Input Leakage	I_L			0.1	mA
RMS Jitter, 12kHz to 20 MHz, **P option** (HFF)				<1	pS
Control Voltage Modulation Bandwidth	BW	10			kHz
Maximum Control Voltage		0		V_{DD}	
Maximum Supply Voltage				7	V
Storage Temperature	T_S	-55	-	125	°C
Soldering Temp./Time	T_{LS}	-	-	240/10	°C/s

1. Power supply bypass is required and a 0.1uF in parallel with a 0.01uF high frequency capacitor is recommended.
2. Transition times are measured from 20% to 80% of a full 10K ECL level swing.

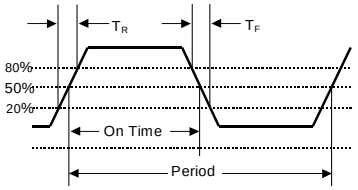


Figure 7. Output Waveform

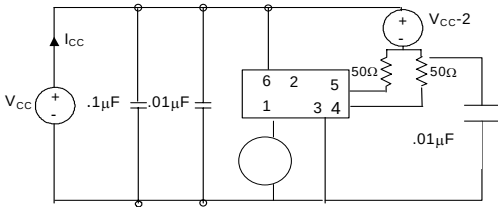


Figure 8. Output Test Conditions (25±5°C)

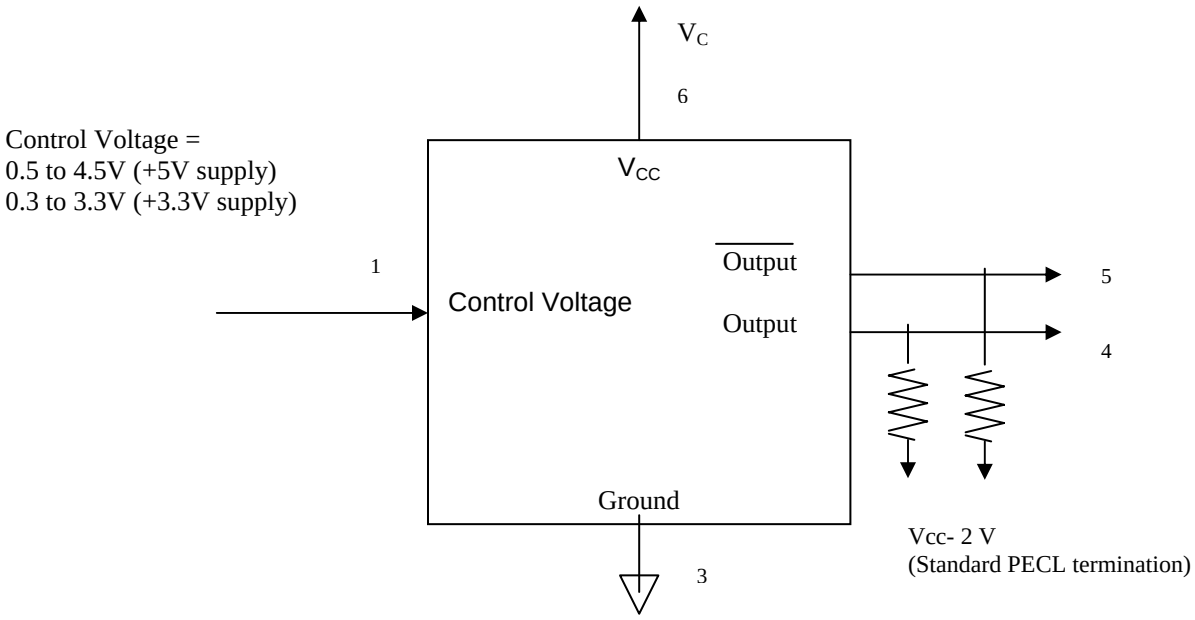


Figure 9. PECL Operation

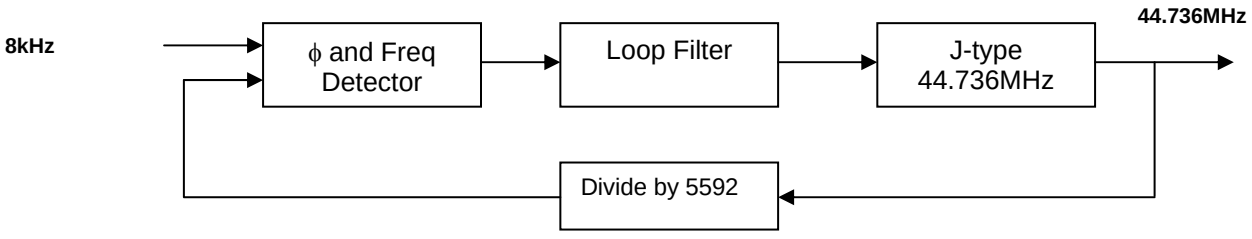


Figure 10. Typical Frequency Translation Diagram

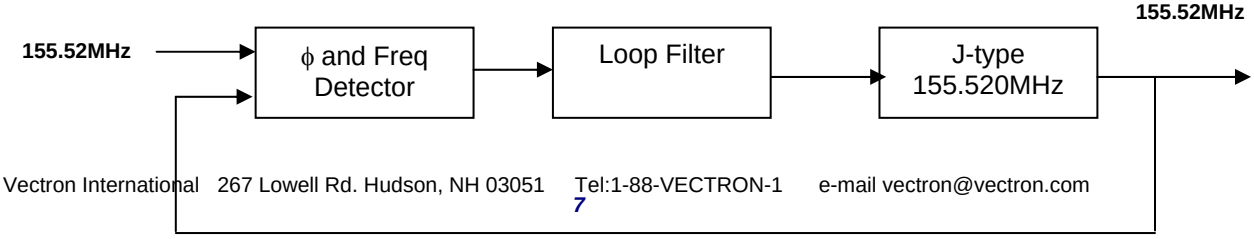


Figure 11. Typical Clock Smoothing Diagram

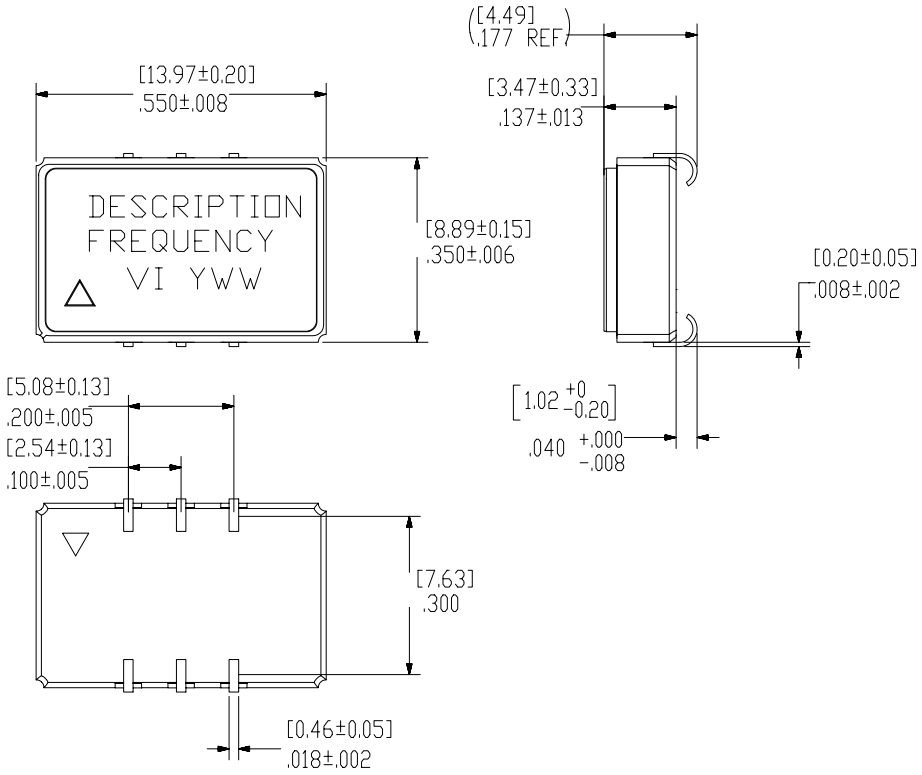


Figure 12. Outline Diagram

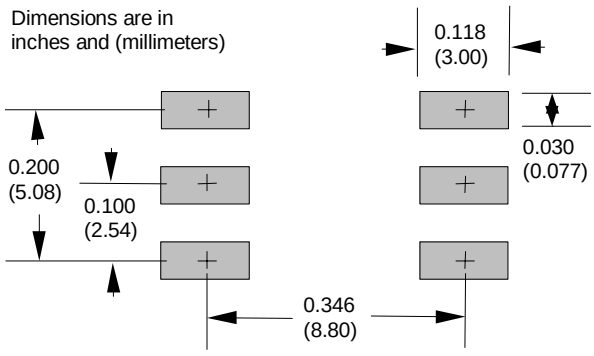


Figure 13. Suggested Pad Layout

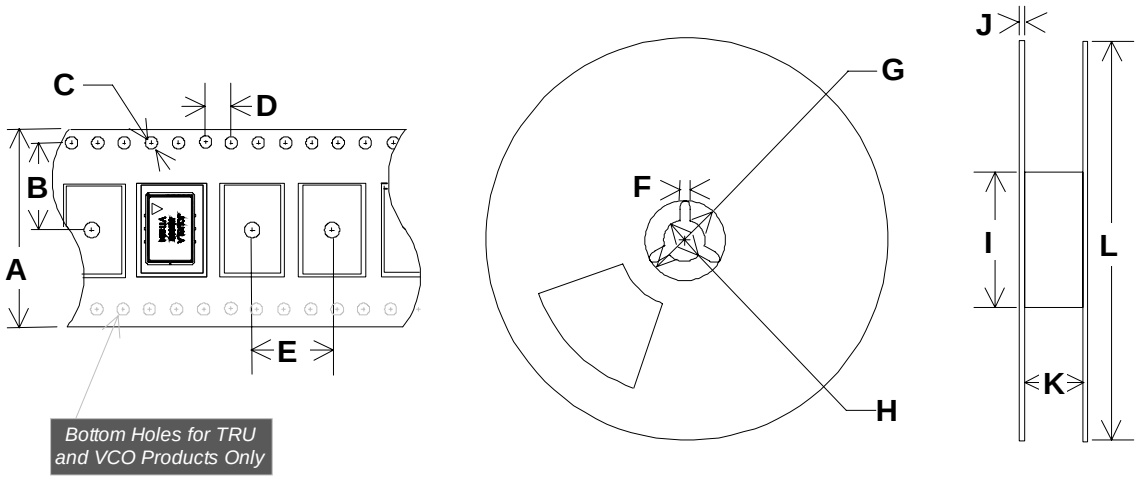


Figure 14. Tape Reel Drawing for CMOS and PECL output option

Table 10. Tape and Reel Dimensions (mm)

Tape Dimensions						Reel Dimensions							# Per
Product	A	B	C	D	E	F	G	H	I	J	K	L	Reel
J-Type	24	11.5	1.5	4	12	1.78	21	13	100	5	25	330	200

Table 11. Ordering Information for PECL output option (add frequency)															
Package		**Supply Voltage (V)**		**VCXO Type**		**APR (ppm)**		**Operating Temp. (°C)**		**Output/ Duty Cycle Min/Max**		**Enable/ Disable**		**Specials**	
J	6 pin Ceramic SOJ	**C**	5V±10%	**U**	VCXO	**F**	±32	**C**	0/70	**M**	PECL 45/55%	**U**	None	**N**	Standard
		D	3.3±10%	**L**	±10% linear VCXO	**G**	±50	**L**	-40/ 85			**E**	Enable/ Disable on pin 2	**P**	6pS rms jitter
				M	±20ppm stability VCXO									**R**	12ps rms jitter
														T	20ps rms jitter

1. Note: Not all combinations are possible.

Example: JDUGLMEP 77.76 = 3.3 volt, VCXO @ 77.760MHz, ±50 ppm, APR, -40/85°C, PECL, Enable/Disable on pin 2, 6ps rms jitter.

Table 12. Standard Frequencies, in MHz					
77.760	82.944	155.52			

Other frequencies available upon request.

For Additional Information, Please Contact:

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